Error-Correcting Codes for TLC Flash

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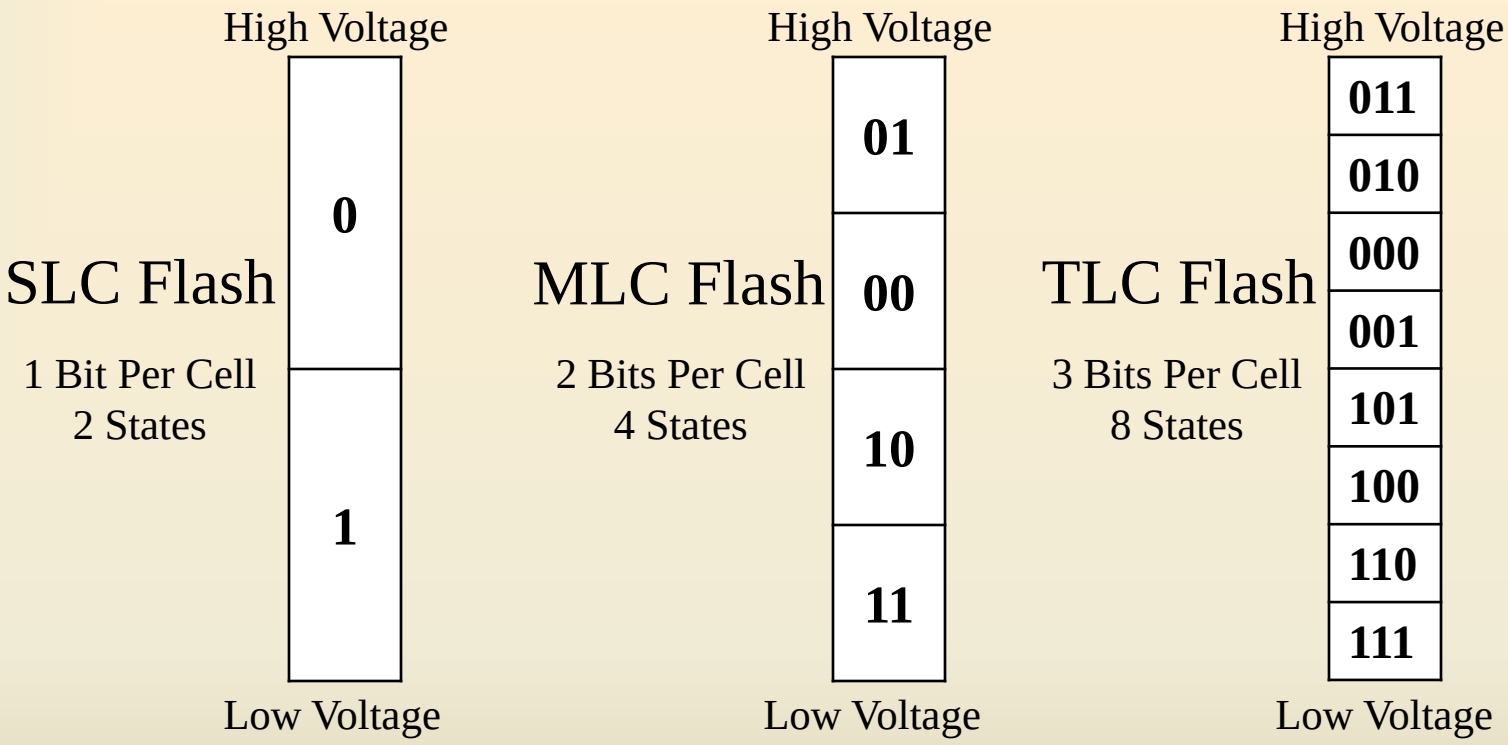
Outline

- Flash Memory Structure
- Partial Cell Usage in TLC Flash
- ECC Comparison for TLC Flash
- New ECC Scheme for TLC Flash

SLC, MLC and TLC Flash



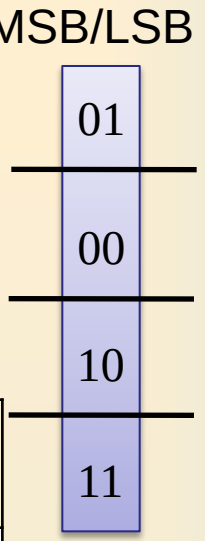
Flash Memory Structure

- A group of cells constitute a page
- A group of pages constitute a block
  - In SLC flash, a typical block layout is as follows

page 0	page 1
page 2	page 3
page 4	page 5
. . .	. . .
page 62	page 63

Flash Memory Structure

- In MLC flash the two bits within a cell **DO NOT** belong to the same page – **MSB page** and **LSB page**
- Given a group of cells, all the MSB's constitute one page and all the LSB's constitute another page



Row index	**MSB** of **first** 2^{14} cells	**LSB** of **first** 2^{14} cells	**MSB** of **last** 2^{14} cells	**LSB** of **last** 2^{14} cells
0	page 0	page 4	page 1	page 5
1	page 2	page 8	page 3	page 9
2	page 6	page 12	page 7	page 13
3	page 10	page 16	page 11	page 17
⋮	⋮	⋮	⋮	⋮
30	page 118	page 124	page 119	page 125
31	page 122	page 126	page 123	page 127

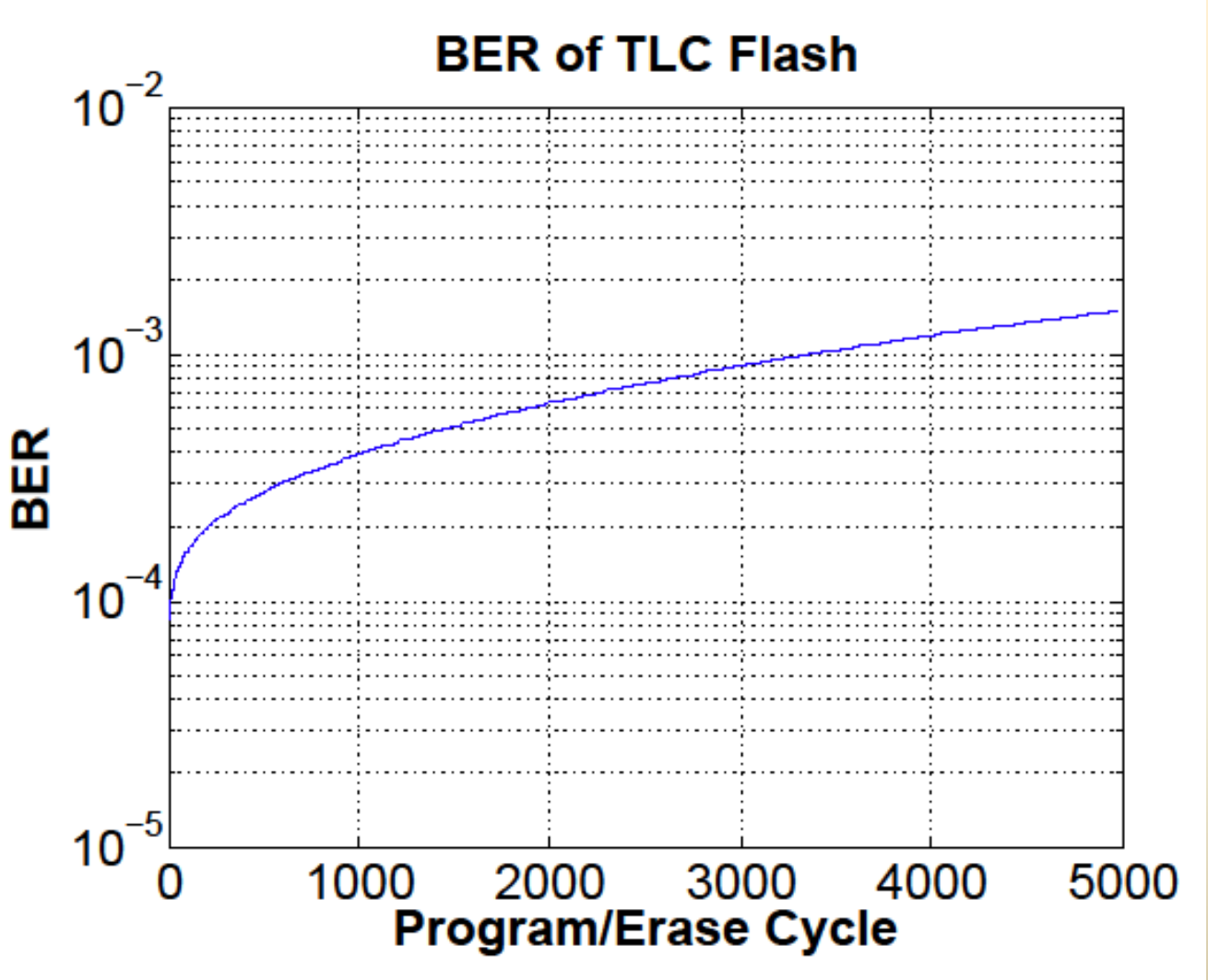
Flash Memory Structure - TLC

	MSB Page	CSB Page	LSB Page	MSB Page	CSB Page	LSB Page
Row index	**MSB** of **first** 2^{16} cells	**CSB** of **first** 2^{16} cells	**LSB** of **first** 2^{16} cells	**MSB** of **last** 2^{16} cells	**CSB** of **last** 2^{16} cells	**LSB** of **last** 2^{16} cells
0	page 0			page 1		
1	page 2	page 6	page 12	page 3	page 7	page 13
2	page 4	page 10	page 18	page 5	page 11	page 19
3	page 8	page 16	page 24	page 9	page 17	page 25
4	page 14	page 22	page 30	page 15	page 23	page 31
⋮	⋮		⋮	⋮		⋮
62	page 362	page 370	page 378	page 363	page 371	page 379
63	page 368	page 376		page 369	page 377	
64	page 374	page 382		page 375	page 383	
65	page 380			page 381		

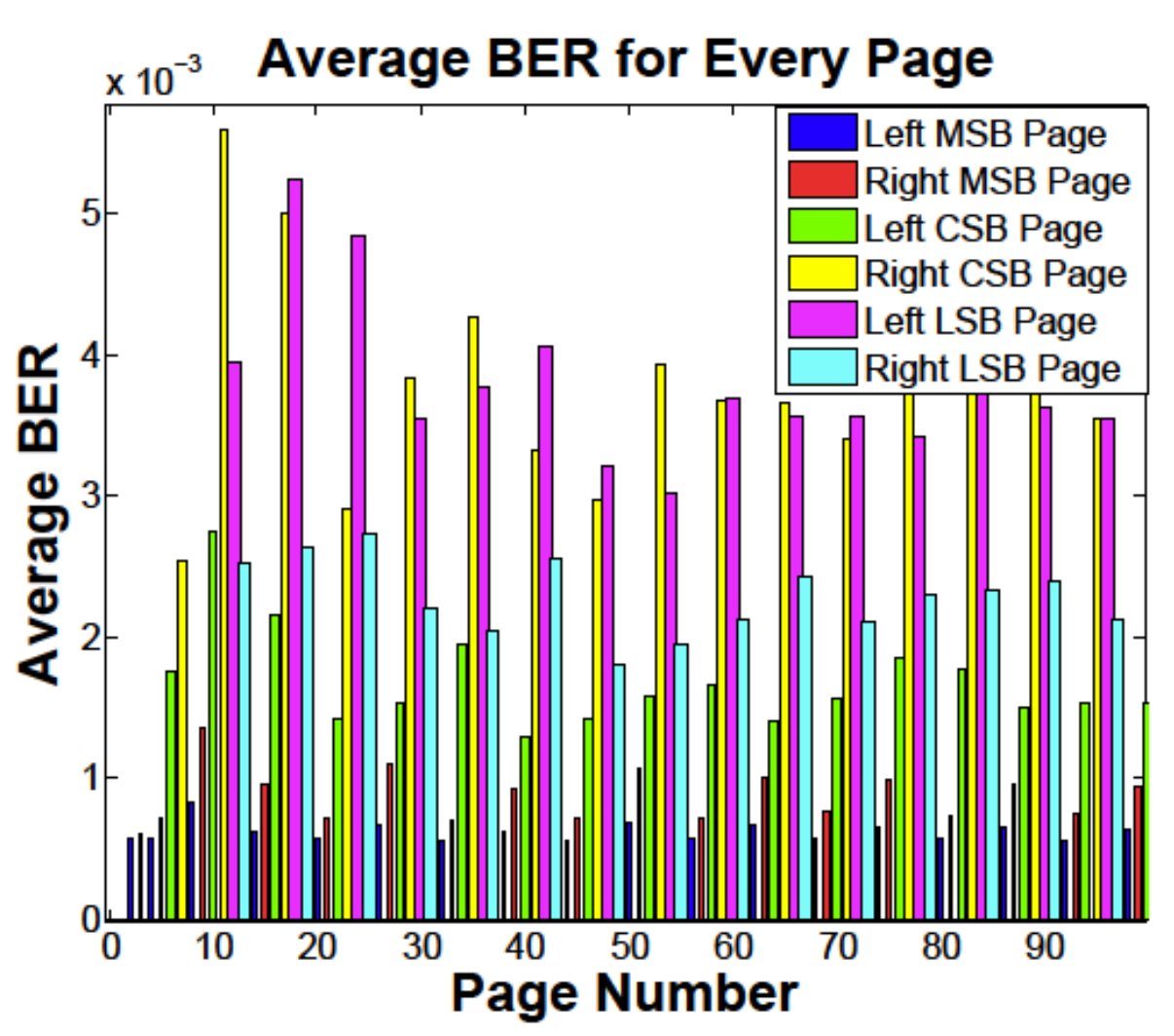
Experiment Description

- We checked several flash memory **TLC** blocks
- For each block the following steps are repeated
  - The block is **erased**
  - A pseudo-random data is **written** to the block
  - The data is **read** and **compared** to find errors
- **Remarks**:
  - We measured many more iterations than the manufacturer's guaranteed number of erasures
  - The experiment was done in laboratory conditions and related factors such as temperature change, intervals between erasures, or multiple readings before erasures were not considered

Raw BER Results



Raw BER Results



High Voltage

011
010
000
001
101
100
110
111

Low Voltage

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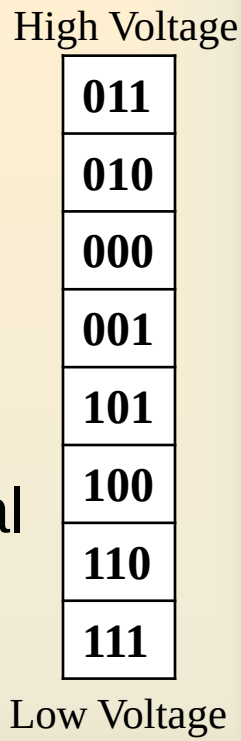
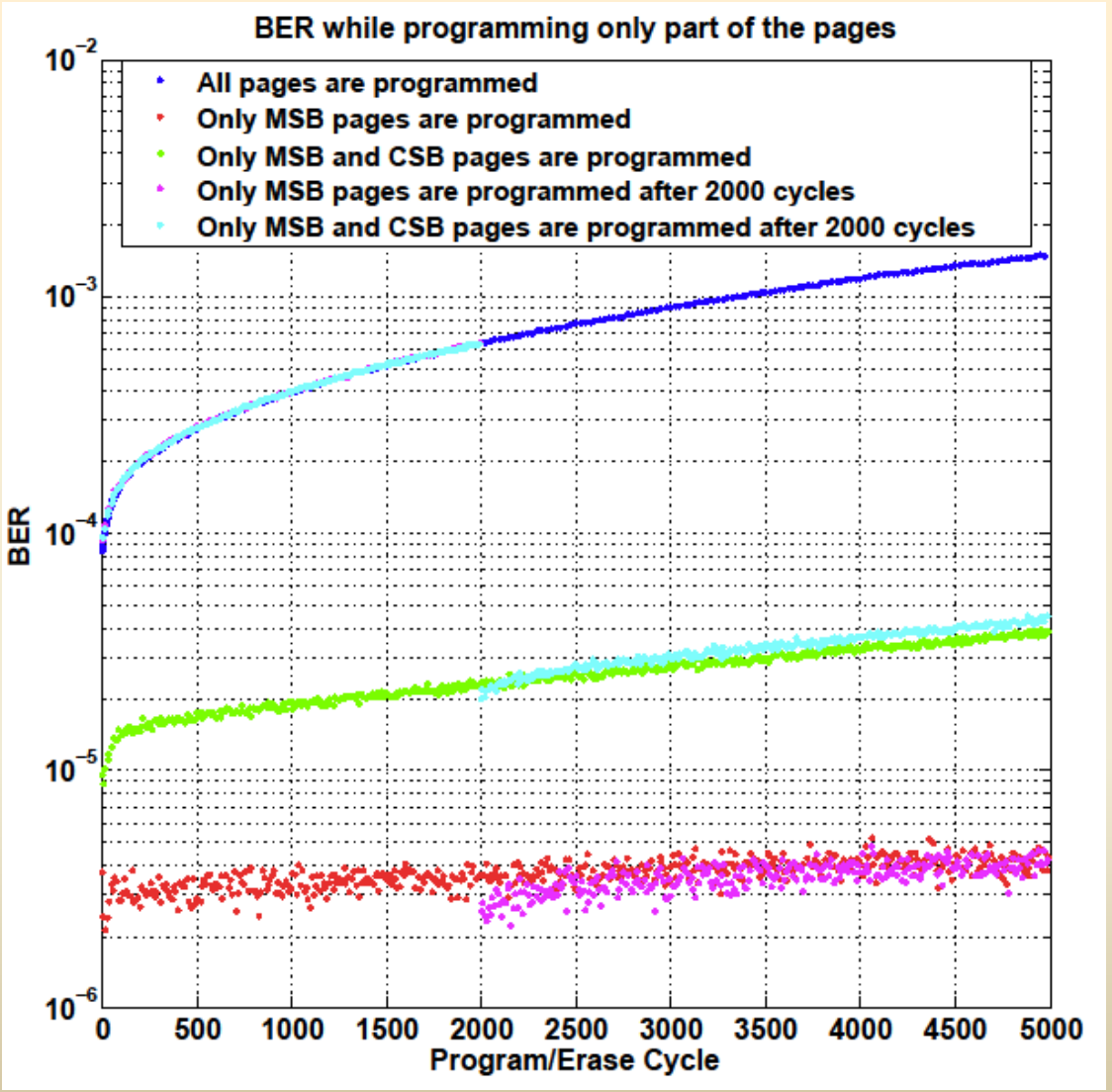
Partial Cell State Usage

- Store either one or two bits in every cell
  - For one bit, only the MSB pages
  - For two bits, only the MSB and CSB pages
- Two cases:
  - The partial storage is introduced at the beginning
  - The partial storage is introduced after 2000 normal program/erase cycles



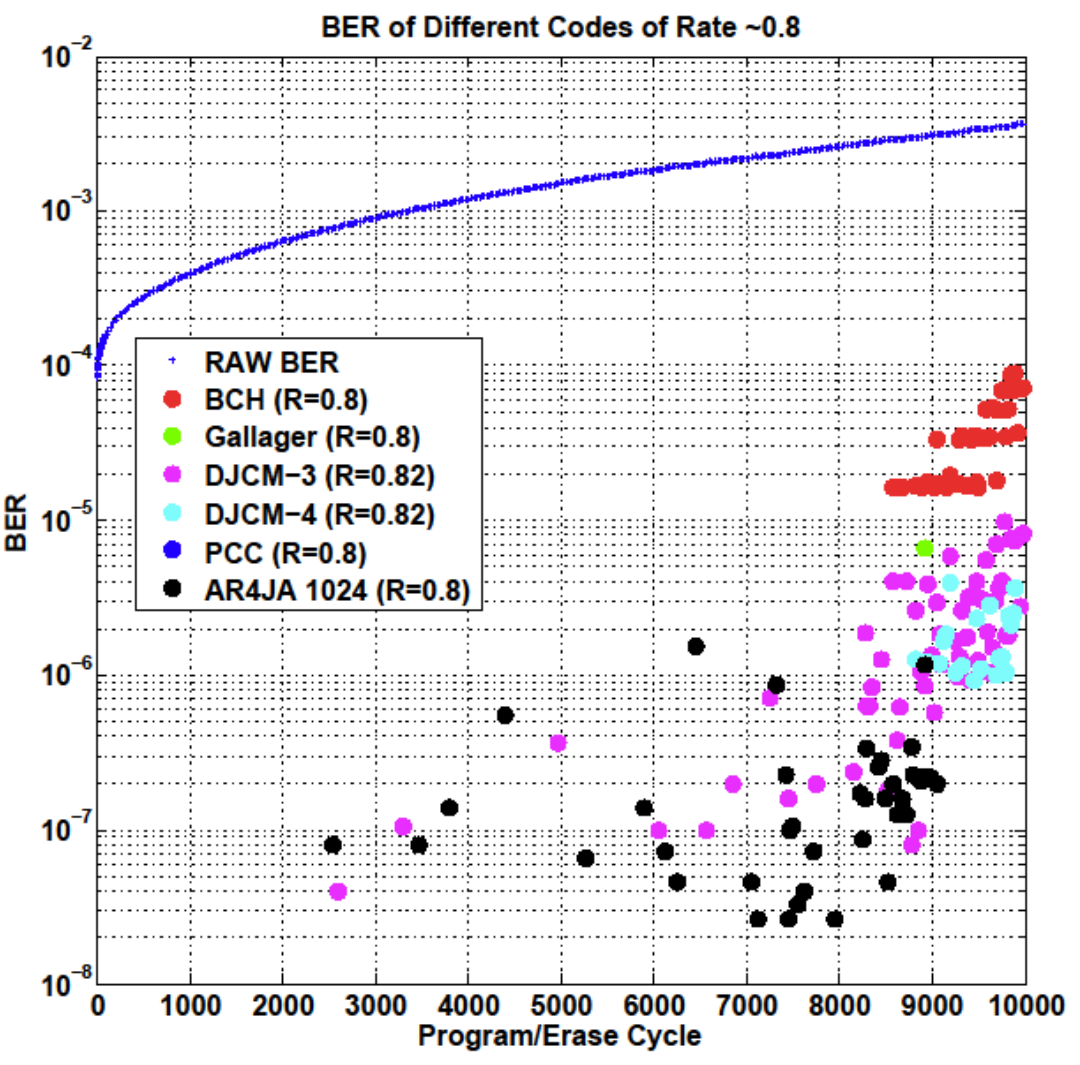
Partial Cell State Usage - BER



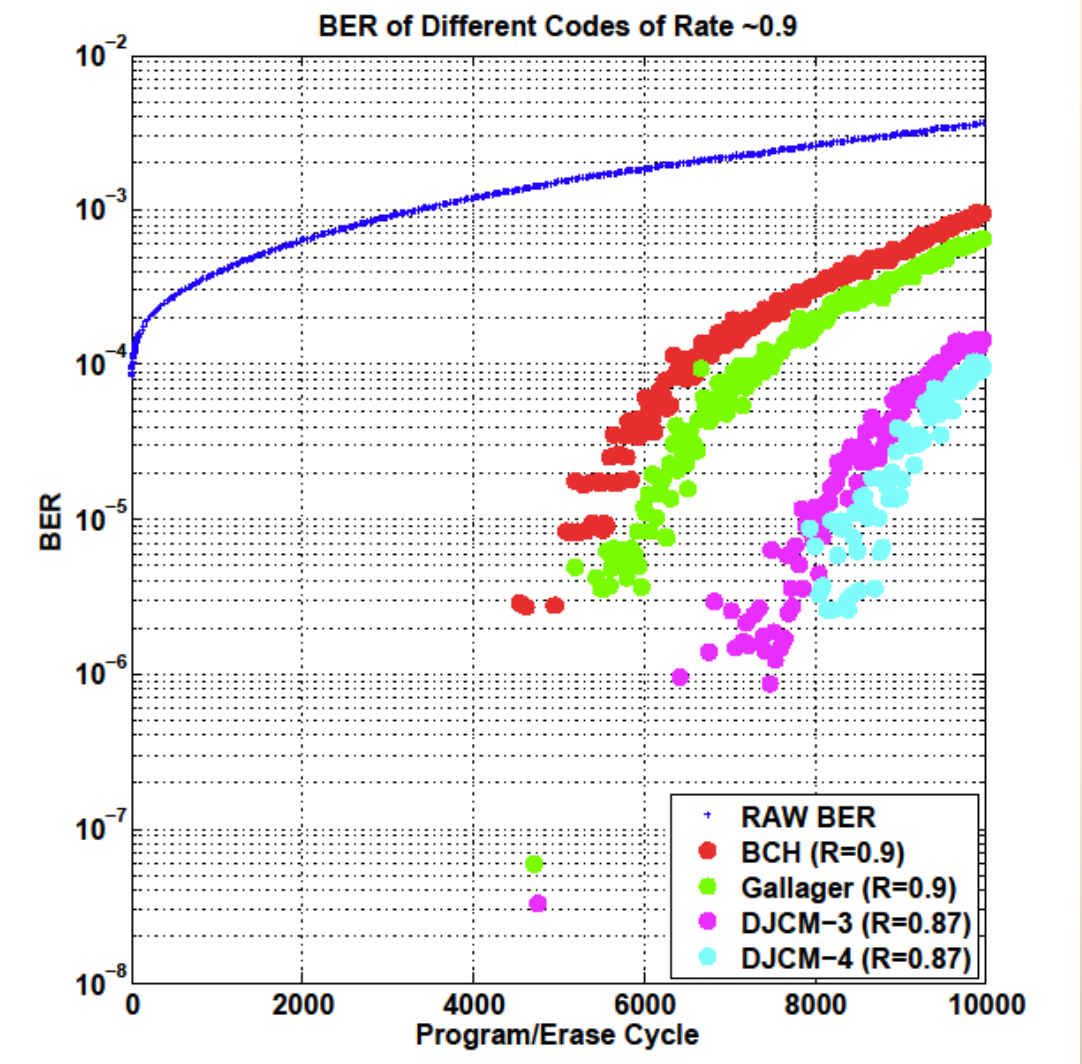
ECC Comparison

- We evaluated different ECC schemes
- BCH Codes
- LDPC Codes
  - Gallager Codes
  - Protograph-based low-density convolutional codes
  - AR4JA protograph-based LDPC codes
  - LDPC codes taken from MacKay's database of sparse graph codes

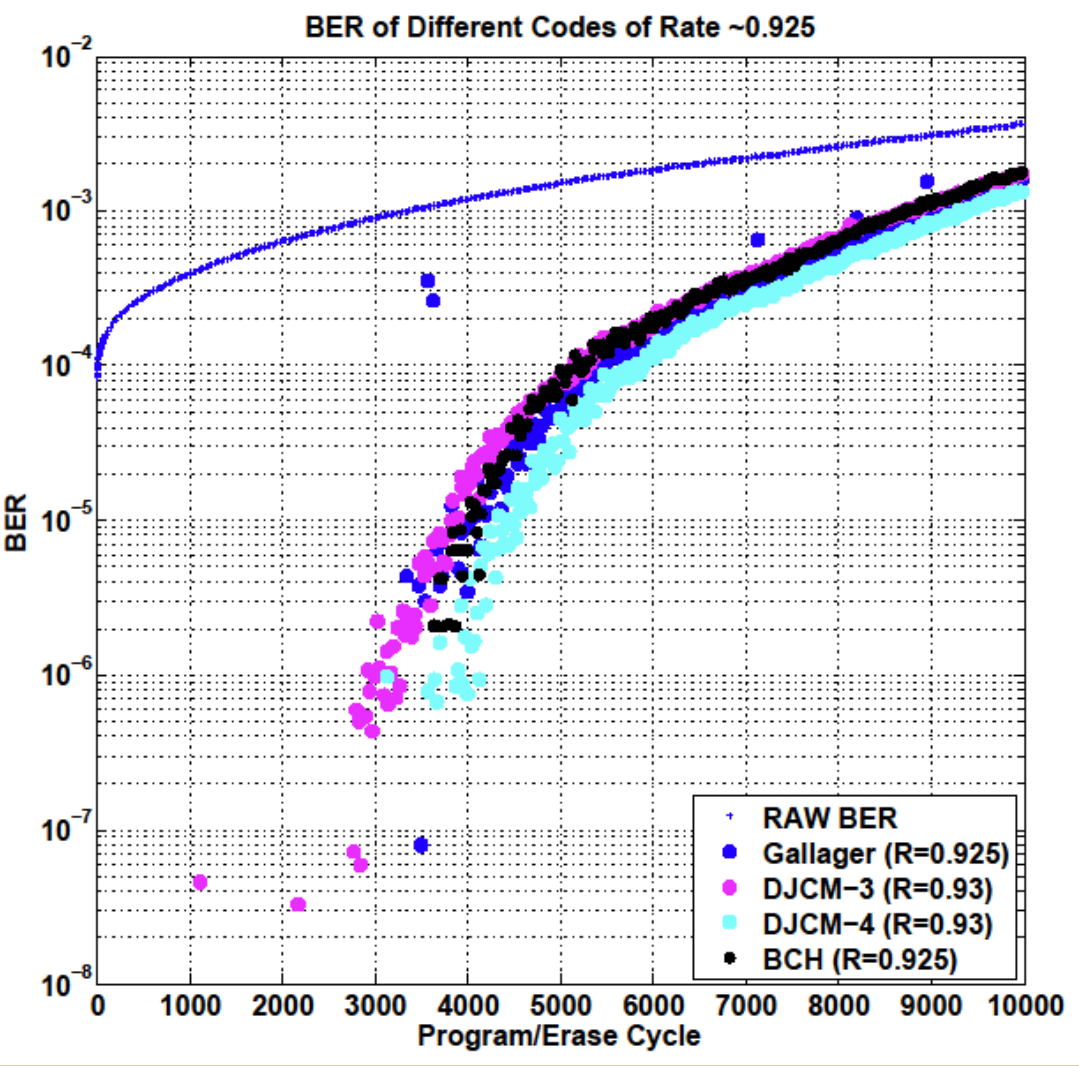
ECC Comparison $R \approx 0.8$



ECC Comparison $R \approx 0.9$



ECC Comparison $R \approx 0.925$

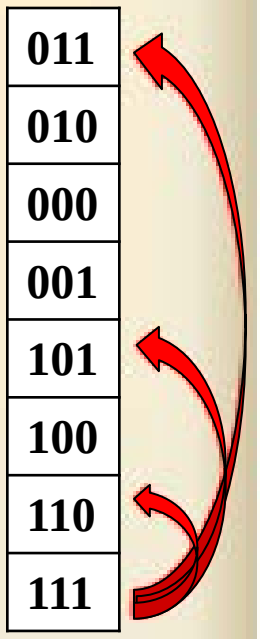


New ECC Scheme for TLC Flash

- Errors are corrected in each page **independently**
- In particular, in a group of MSB, CSB, and LSB pages sharing the same group of cells, errors are still corrected independently

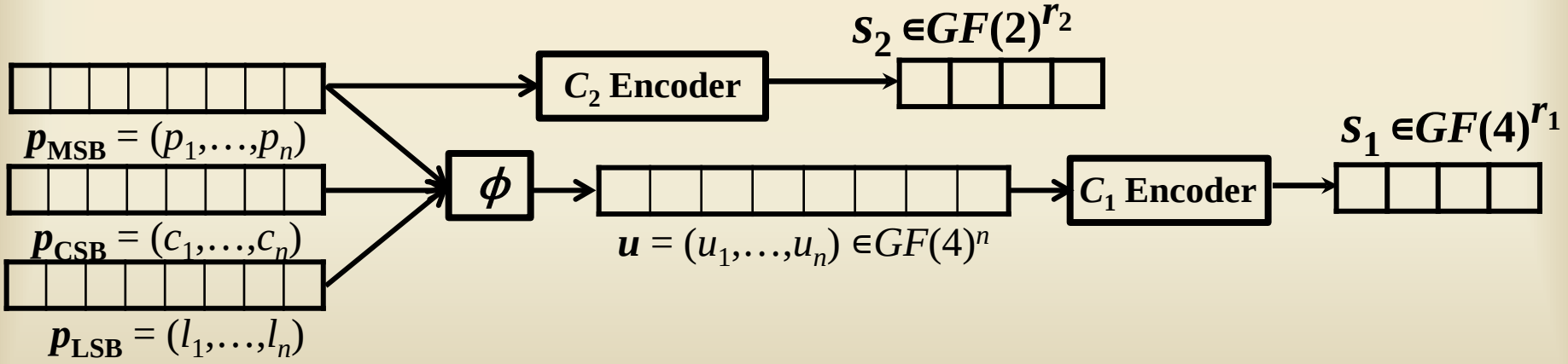
- **Goal**: to correct errors in a group of pages **together**

- If a cell is in error, then with high probability one of the bits in the cell is in error



New ECC – Encoder

- From every group of three pages we generate one page over $GF(4)$
- Use two codes
  - A code over $GF(4)$ – encodes the new page over $\mathrm{GF}(4)$
  - A binary code – encodes the MSB pages



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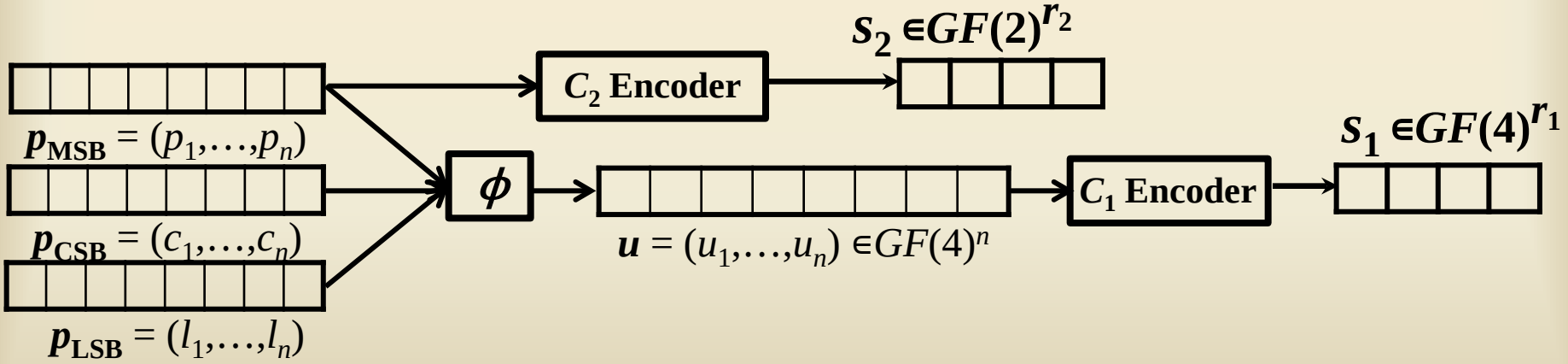
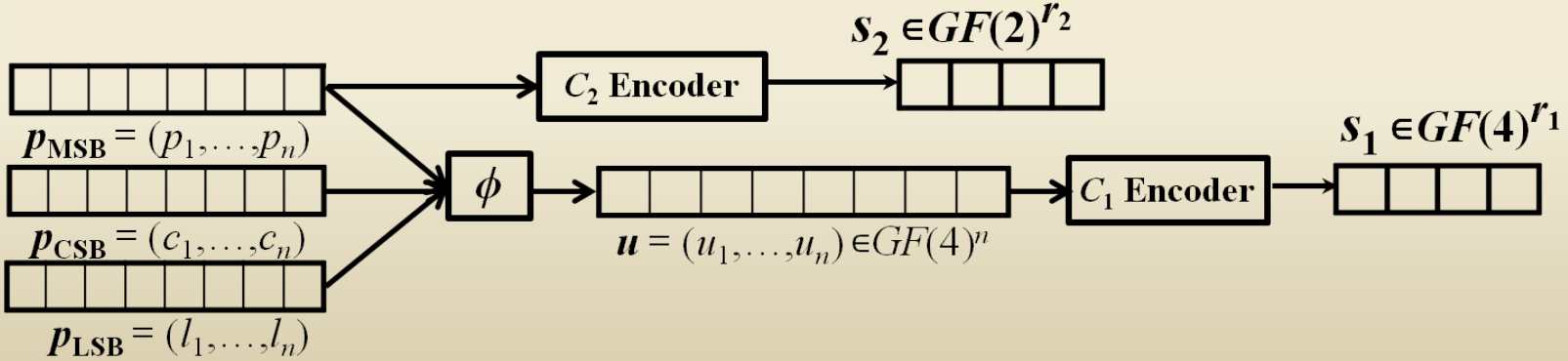
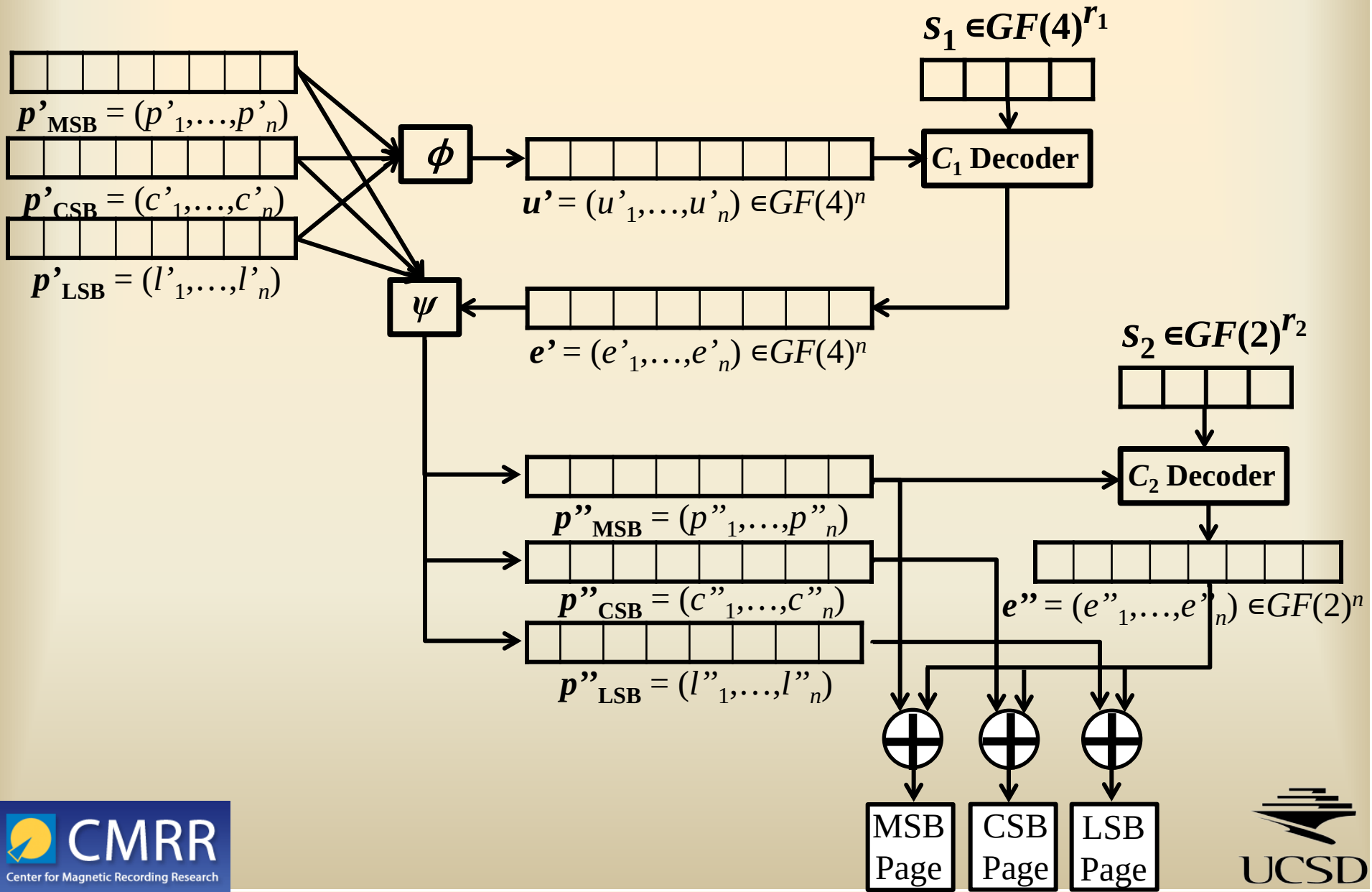


New ECC - Insights

- If there is a cell error, then with high probability **at most one** of the bits in the cell is in error
- The code over $GF(4)$ find these one-bit cell-errors
- However, it is still possible to see 2-bit and 3-bit cell errors
- After the first stage, if a cell has 2- or 3-bit cel-errors, then all the bits are in error
- The second code, working on the MSB bits, finds these errors



New ECC – Decoder



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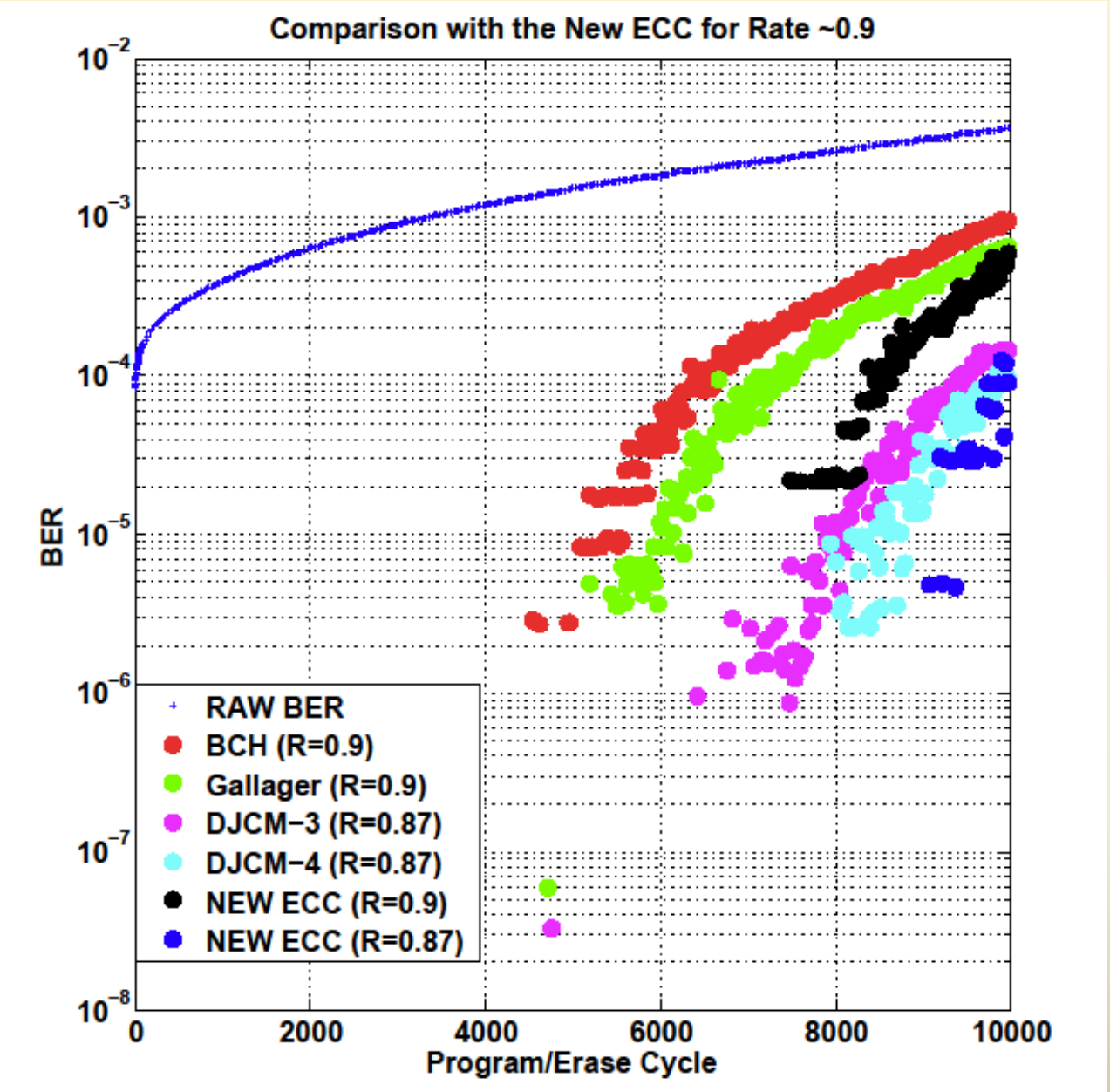
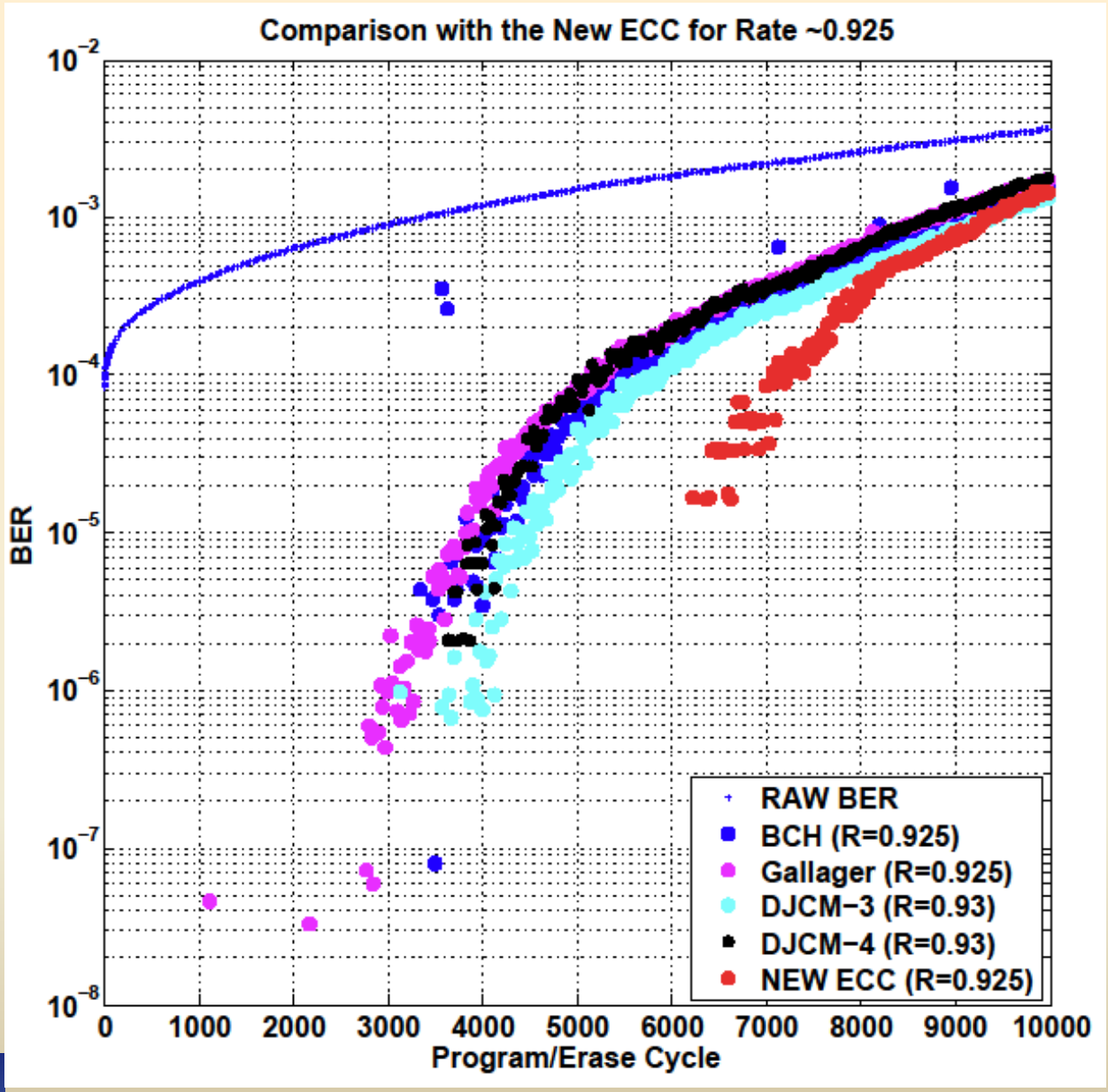

Comparison with the New ECC for Rate ~0.9
BER
Program/Erase Cycle
RAW BER
BCH (R=0.9)
Gallager (R=0.9)
DJCM−3 (R=0.87)
DJCM−4 (R=0.87)
NEW ECC (R=0.9)
NEW ECC (R=0.87)


Comparison with the New ECC for Rate ~0.925
BER
Program/Erase Cycle
RAW BER
BCH (R=0.925)
Gallager (R=0.925)
DJCM−3 (R=0.93)
DJCM−4 (R=0.93)
NEW ECC (R=0.925)

Summary

- Partial Cell Usage in TLC Flash
- ECC Comparison for TLC Flash
- New ECC Scheme for TLC Flash
- More analysis of codes and error behavior -

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Acknowledgements

- Aman Bhatia, Brian K. Butler, Aravind Iyengar, and Minghai Qin for their help in processing the error measurement results and, in particular, for the LDPC code performance simulations
- Jeff Ohshima and Hironori Uchikawa for their collaboration and support from Toshiba