Architecture Customized Constrained Coding for Mitigating FGFG coupling in Flash

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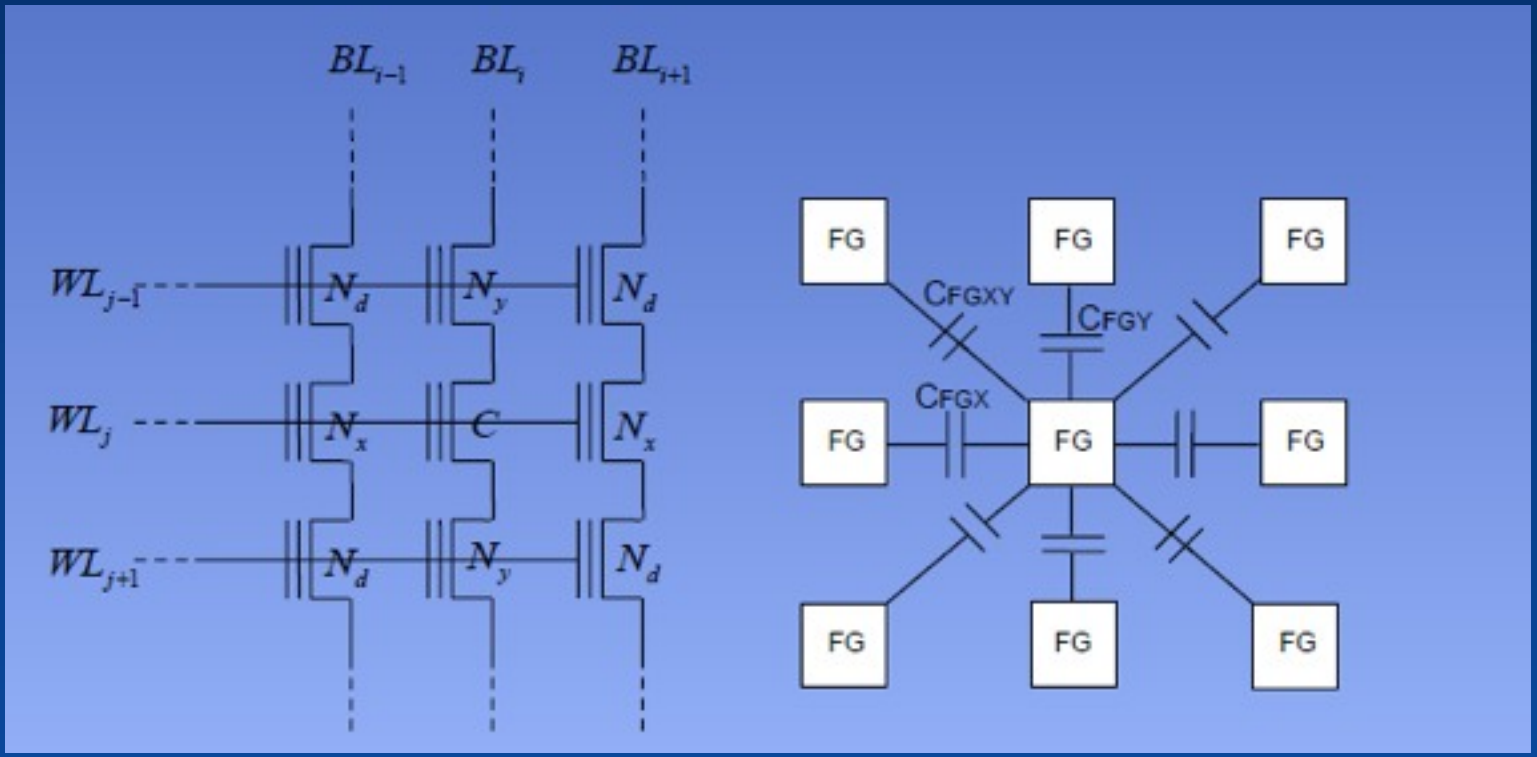
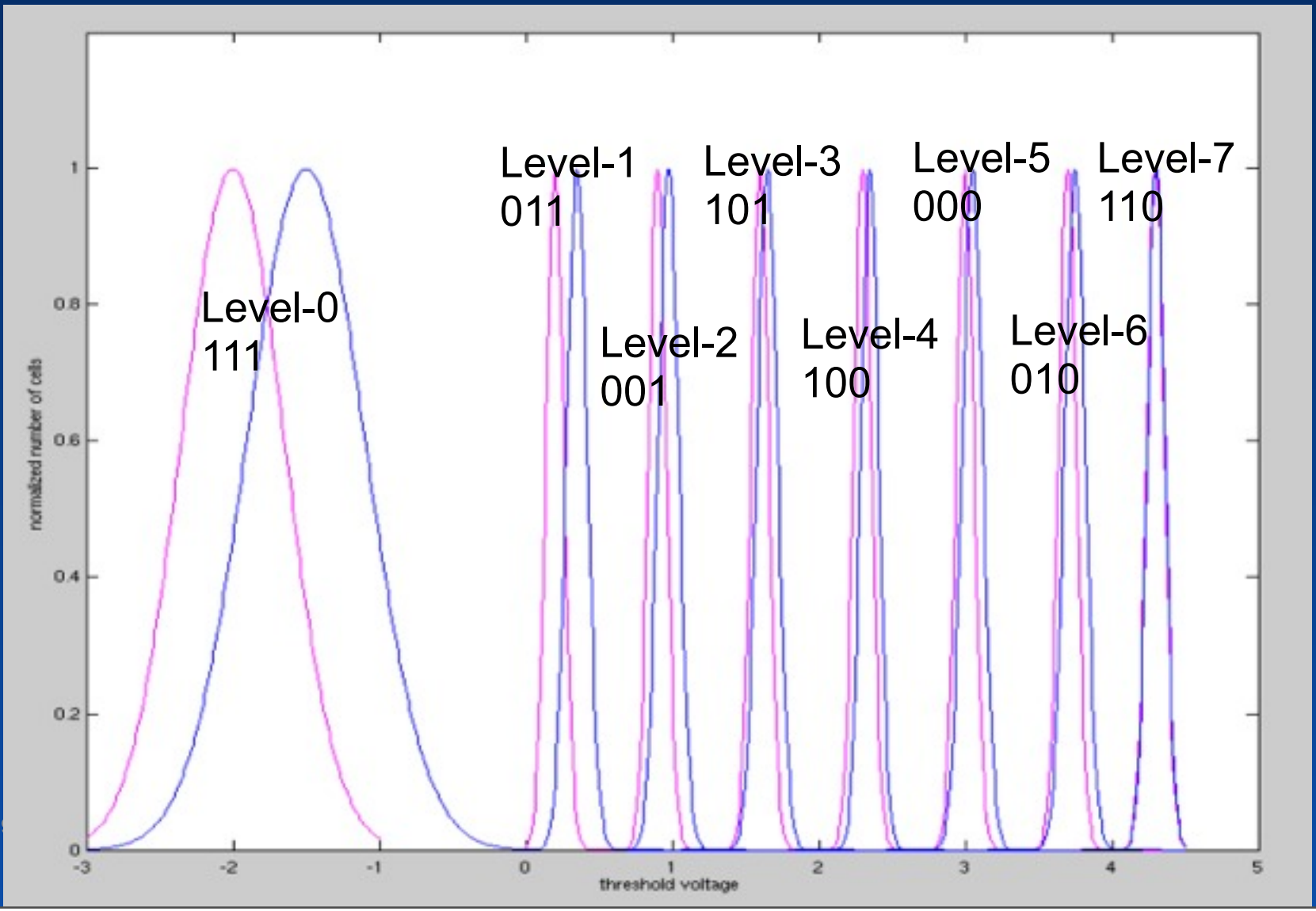
Floating-Gate (FG) Coupling

- FG to FG coupling causes inter-cell interference.



A. Berman, Y. Birk, FMS 2010

Distributions Shift/Broaden



Neighbors

- For 3 bits per cell, FGFG coupling causes level 7- level 0- level-7 pattern to migrate to the 7-1-7 pattern.
- 7-0-6 and 6-0-7 patterns are also significantly impacted.
- For 2 bits per cell 3-0-3 pattern, (followed by the 3-0-2 and 2-0-3 pattern).

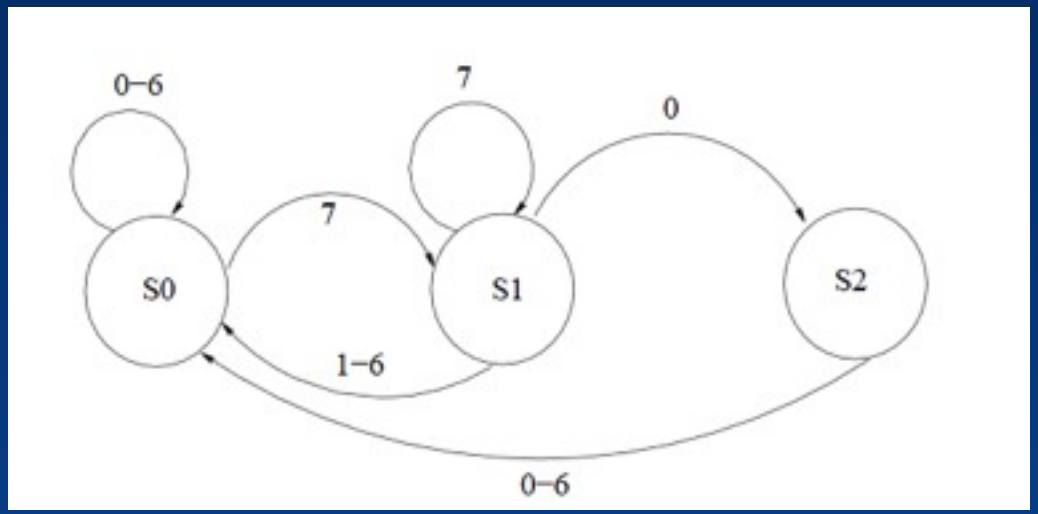
Neighbors

- GOAL- Forbid the 7-0-7 pattern to be written to the NAND.
- One Solution- USE CONSTRAINED CODING.

Constrained Code

- The constrained code forbids or almost eliminates the spurious patterns.

Constrained systems



- Forbids the 7-0-7 pattern.
- Capacity- Theoretical limit on constrained code- How much minimum redundancy?
- Maximum Eigen-value of the Adjacency Matrix.

Capacity

- Adjacency Matrix
- Each (*i,j*)-th entry is the number of outputs from level *i* to level *j*

$$\begin{pmatrix} 7 & 1 & 0 \\ 6 & 1 & 1 \\ 7 & 0 & 0 \end{pmatrix}$$

- Capacity=$\log_2 \lambda_{max}$ = 2.9972 bits

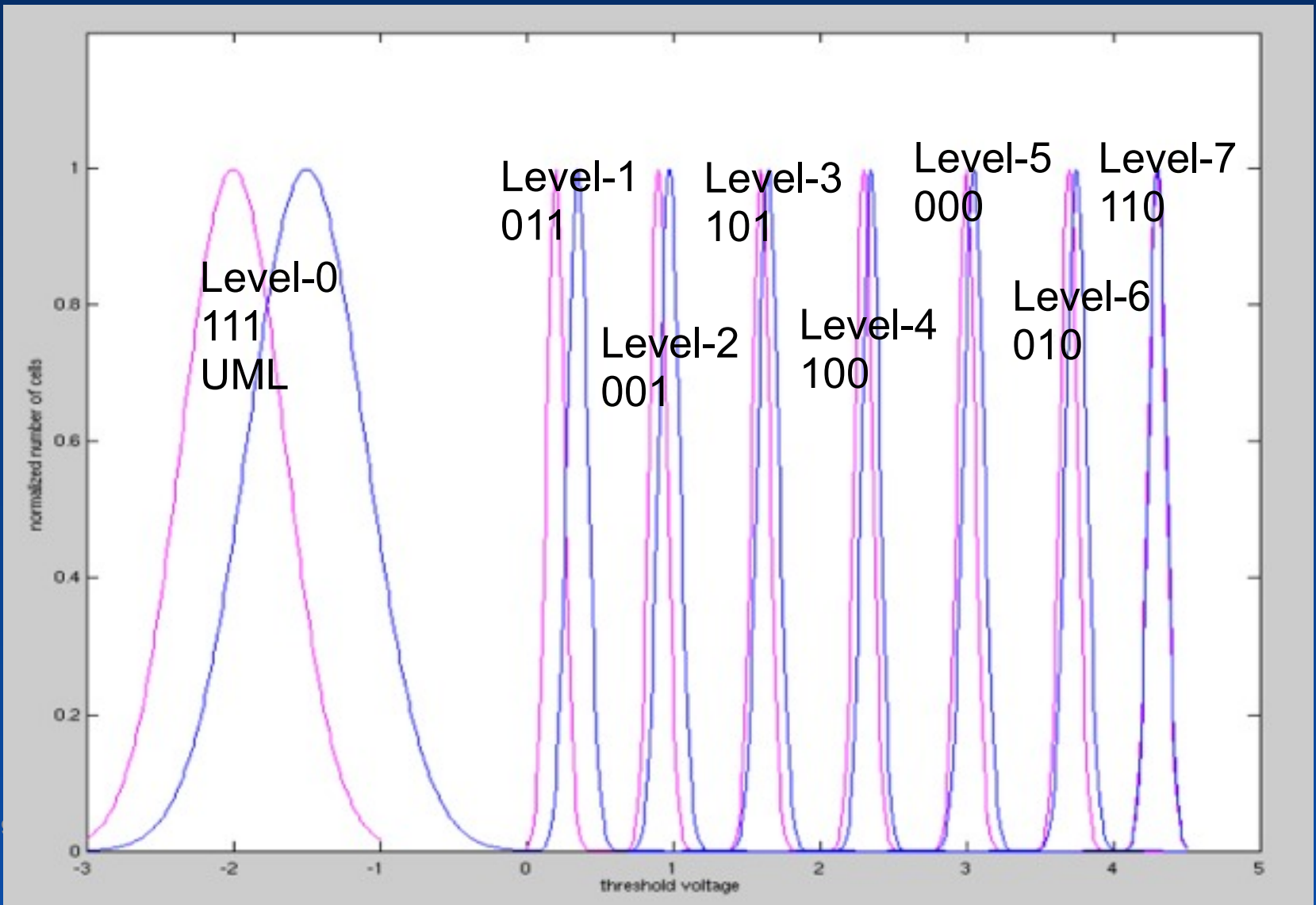
Level Information for Encoding/Decoding

- Constrained code operates on levels- maps levels to levels.
- Encoding needs level information.
- Decoding any page needs level information.
- NAND outputs only bit information for all pages.
- Drawback- NAND has output level information while reading lower, middle and upper pages.

Impose Further Constraints

- Constrained code can only map a level-7 to level-6 and level-0 to level-1.
- That constrained code does not change the lower and middle page bits.
- Only upper page bits can get flipped by the constrained code.
- Block codes which only map level-7 to level-6 and level-0 to level-1 are low rate- at least 5% spares.

Distributions Shift/Broaden



Variable length constrained coding for the 7-0-7

- Scan the levels from left to right.
- Check for the 7-0-7 pattern.
- If a 7-0-7 pattern is seen, modify this to a 6-1-6 pattern.
- If a 6-1-6 pattern is seen, leave it unmodified.

Encoding

- Input Bits
- 000 001 100 111 111 100 **110 111 110** 010 100 …
- Input Levels to the Constrained Encoder
- 5 2 4 0 0 4 7 0 7 6 4 …
- Output Levels after Constrained Encoding
- 5 2 4 0 0 4 6 1 6 6 4 …
- Output Bits
- 000 001 100 111 111 100 **010 011 010** 010 100 …
- Flipping only the Upper Page Bits.
- Appended Bit-stream

Appended Bit-stream

- 000 001 100 111 111 100 **010 011 010** 010 100 … 1…….
- Appended bit-stream stores information about the levels which were modified.
- Advantage- Since lower and middle page bits were not modified, there is no need for level information for decoding lower and middle page.

Appended Bit-stream

- Convert appended bit-stream to level information.
- This is the overhead penalty for this constrained code.
- Length of the appended bit-stream is variable.
- Limit the length to a maximum predetermined value- implies that 7-0-7 pattern is minimized and not completely eliminated for some inputs.

Average Overhead

- All levels are equi-probable, probability of a level=1/8.
- Total 8^3 distinct 3-tuple levels.
- 7-0-7 and 6-1-6 cause a bit to be inserted in the appended bit-stream.
- Average Symbol Rate= $8^3/(8^3+2/3)=0.9987$ → 0.13% extra levels

Fix the overhead

- Fix the number of overhead bits- N levels.
- Chose N such that with a very high probability p- 0.9999, the number of 7-0-7 patterns written into the NAND is smaller than a fixed number m→ N(*p,m*).

Spurious Patterns

- Extend the design to eliminate (or almost eliminate) the 7-0-7, 6-0-7 and 7-0-6 patterns.
- 7-0-7→ 6-1-6, 6-0-7→6-1-7, 7-0-6→ 7-1-6

Noiseless Decoding

- Lower and Middle page unchanged

For Upper page-

- Read all level information including the appended level information.
- Converts appended level information into appended bit-stream information.
- Counter=1→ Point to first bit of the appended bit-stream
- Scan the read-out levels from left to right.
- If 6-1-6, 6-1-7, 7-1-6 pattern seen, check the appended bit-stream bit and either flip or keep the bits unchanged.

Noiseless Decoding

- Use the read-out level information and not the decoded level information.
- 7-0-7-0-7 (before CC)→ 6-1-6-1-7 (CC)
- 6-1-6-1-7→ 7-0-7-1-7 (not invertible)

Decoding

- Input to the Decoder
- 5 2 4 0 0 4 6 1 6 6 4 … (1…
- 5 2 4 0 0 4 7 0 7 6 4 …

- Output Bits
- 000 001 100 111 111 100 1**10** 1**11** 1**10** 010 100 …
- Flipping the Upper Page Bits.

Noisy Level Information

- A 6-1-6 pattern maps to a different pattern.
- A non-(6-1-6) pattern maps to a 6-1-6 pattern.
- 3 patterns- 7-0-7, 7-0-6, 6-0-7 mapped to 6-1-6, 7-1-6, 6-1-7.

Error Propagation

- A valid 6-1-6 pattern mapping to a different pattern causes an insertion in the appended bit-stream.
- A non-valid pattern mapping to the 6-1-6 pattern causes a deletion in the appended bit-stream.

Synchronization

- 707547064165607534371631660751716…
- 616547164165617534371631661751716…
- 00 10 01 10 01 10 ……
- [616(000) 617(001) 716(010) 707(100) 607(101) 706(110)]
- MSB (noiseless) 1 1 1 0 1 0…. (100 110 101 010 101 010 …)
- From readout levels reconstruct the MSB
- 616547164165517534371631661751716…
- 1 1 0 1 0 ……. Reconstructed appended bit-stream
- 1 1 1 0 1 0…… Noiseless bit readout from appended stream
- Deletion at position 3 in the reconstructed appended bit-stream.
- Estimate the inserted and deleted positions

Synchronization

- Extra redundancy added for synchronization.
- Synchronization considered for the insertion/ deletion channel.
- Combining the insertion/deletion channel information to generate input for the decoder.
- Rate of the synchronization code- 2% overhead.

MAP decoder for synchronization

- Insertion/Deletion probabilities computed from rber.
- Viterbi detector.
- Establishes synchronization.
- Crucial for limiting error propagation.

Synchronization sim results

- Reduces/Eliminates 7-0-7, 7-0-6 and 6-0-7 patterns
- Constrained coding improves the rber.

Rber with no constrained coding	Rber with constrained coding (after decoding)
5e-3	4.7e-3
7.5e-3	7e-3
1e-2	9.5e-3
1.5e-2	1.4e-3