Advanced Management for 3bpc NAND Flash devices

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DensBits

Outline

- ECC for High Reliability 3bpc Embedded System
  - ECC Requirements
  - DensBits' solution
- Ungraceful power-down
  - Problem definition
  - Common solutions and DensBits' solution

ECC Requirements

- Powerful – Must correct many more errors
  - Powerful hard decoding
  - Powerful soft decoding
- Low latency – Must support higher throughput and IOPs
- Low power consumption – Embedded system requirement
- Low gate count

- **But: "Long BCH Codes are Bad",** S. Lin & E. J> Weldon, Information & Control,1967

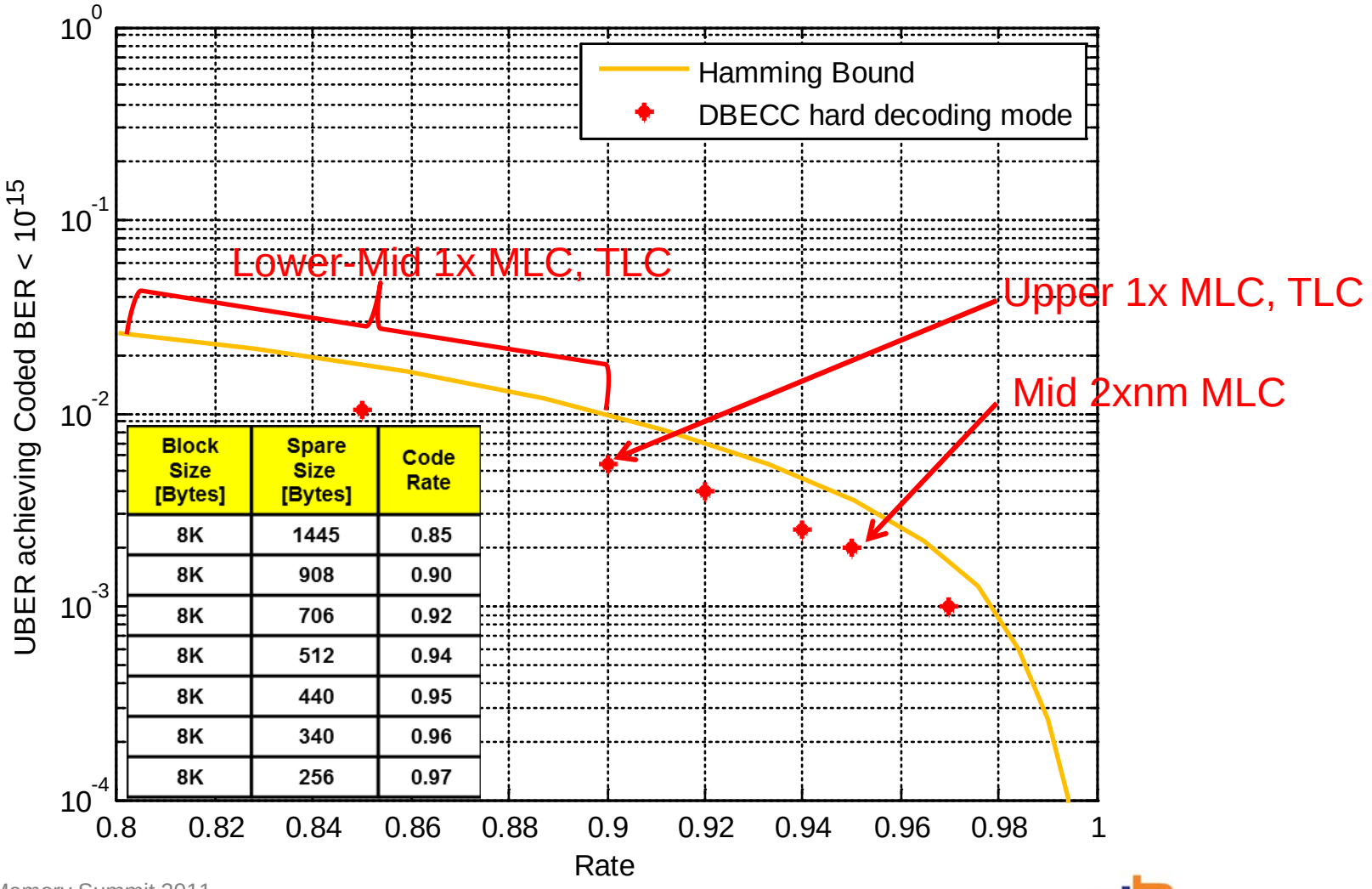
DensBits' ECC

- DensBits' **proprietary, patent pending** coding system (not LDPC nor BCH)
- **Configurable coding system**, the chunk size and code rate are input parameters set via software
  - Chunk size: 512B-8KB
  - Code rate: 0.5 - 0.99
- **Slim design / low power:** 380KG / 7.5mA (65nm, 100MHz Clock)
- **Near-optimal error correction** per chunk size
  - Near Hamming bound (theoretical limit for hard decoding)
  - Near Shannon bound (theoretical limit for soft decoding)

DensBits' ECC (Cont.)

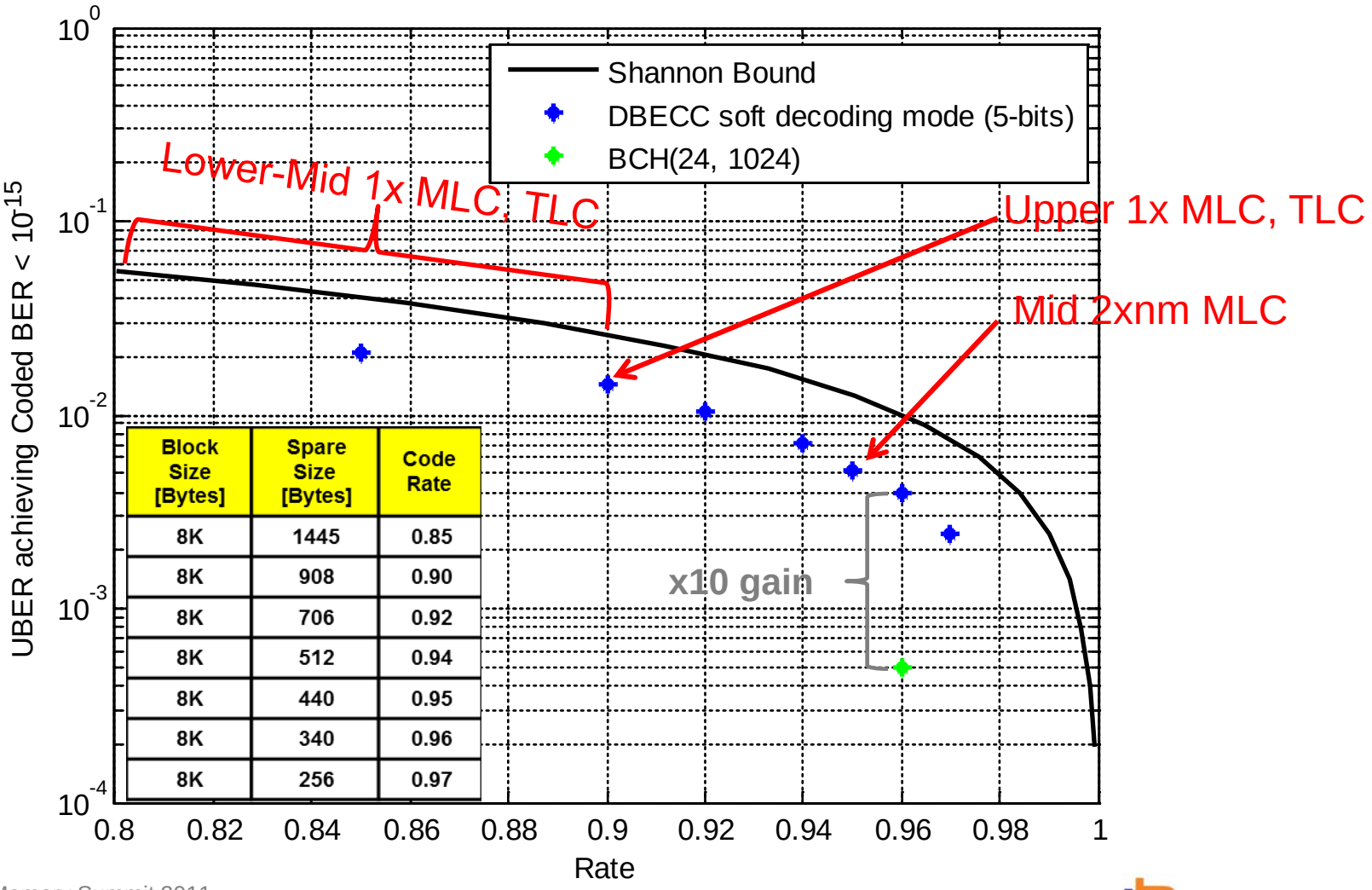
- Partial decoding support, enabling **low read latency**
  - Decode 1 or 2 KB out of an 4 or 8 KB codeword
  - Improved read performance, e.g., **high IOPs** for SSD / eMMC

ECC (Cont.)



Block Size [Bytes]	Spare Size [Bytes]	Code Rate
8K	1445	0.85
8K	908	0.90
8K	706	0.92
8K	512	0.94
8K	440	0.95
8K	340	0.96
8K	256	0.97

ECC (Cont.)



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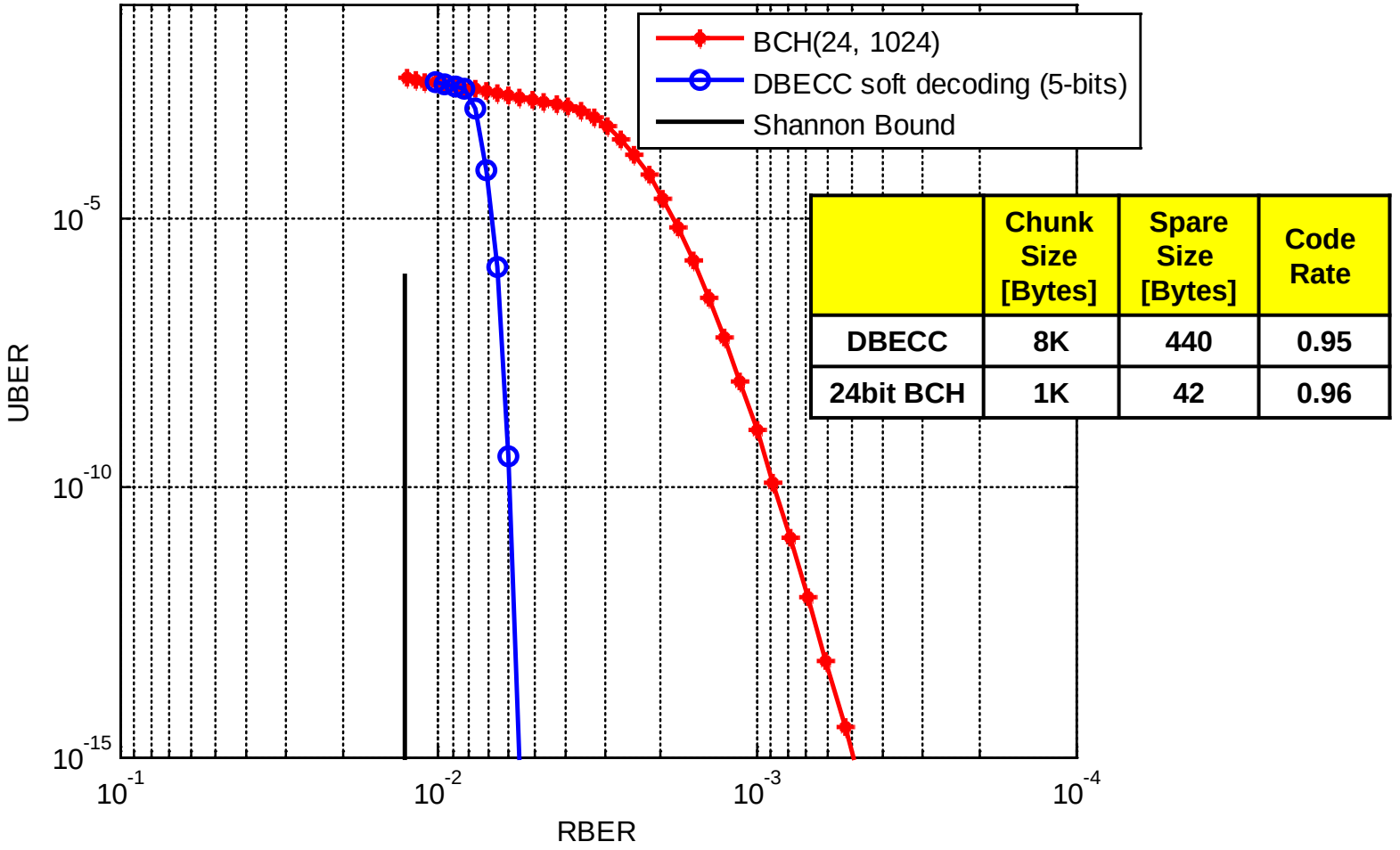

	Chunk Size [Bytes]	Spare Size [Bytes]	Code Rate
DBECC	8K	440	0.95
24bit BCH	1K	42	0.96

ECC (Cont.)

- Examples for several chunk sizes and code rates

Code Rate		RBER @ UBER<1E-15			
		Chunk Size			Shannon Limit
		2KB	4KB	8KB	
0.9	DBECC Hard / Hamming Bound	4E-3 / 7.8E-3	5.2E-3 / 9.1E-3	5.5E-3 / 1E-2	
	DBECC Soft	9.5E-3	1.2E-2	1.4E-2	2.6E-2
0.95	DBECC Hard / Hamming Bound	8E-4 / 2.5E-3	1.3E-3 / 3.1E-3	2E-3 / 3.8E-3	
	DBECC Soft	3.6E-3	4.4E-3	5.3E-3	1.3E-2

ECC (Cont.)

	Hardware Implementation	
Manufacturing Process	65nm	65nm
Clock	100MHz	100MHz
Throughput	100MB/s	400MB/s
Latency	4us	4us
Power Consumption (inc. external buffers)	7.5mA	30mA
Gate Count	380KG	700KG

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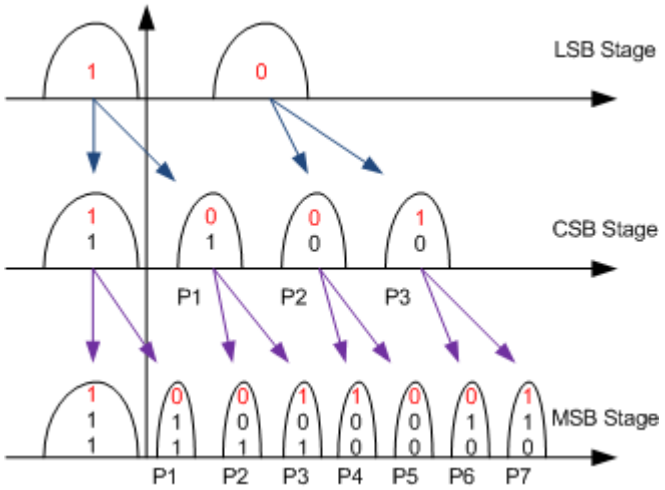
- **Ungraceful power-down**
  - **Problem definition**
  - **Common solutions and DensBits' solution**

Power down scenarios

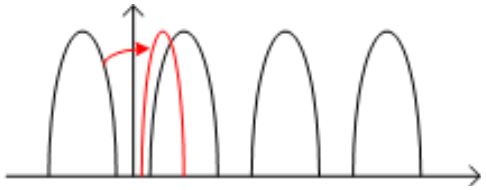
- Managed power off
  - Required data-bases are stored prior to power down
- Sudden power off between transactions (graceful power off)
  - All written data are recoverable through meta-data
- Sudden power off within a write transaction (Ungraceful power loss)
  - All data except for last (interrupted) transaction must be recovered
  - **Past data may be damaged due to interruption**

Ungraceful power loss

- **Unfinished programming may destroy past data:**
  - Normal Programming procedure:



  - Interrupted programming:



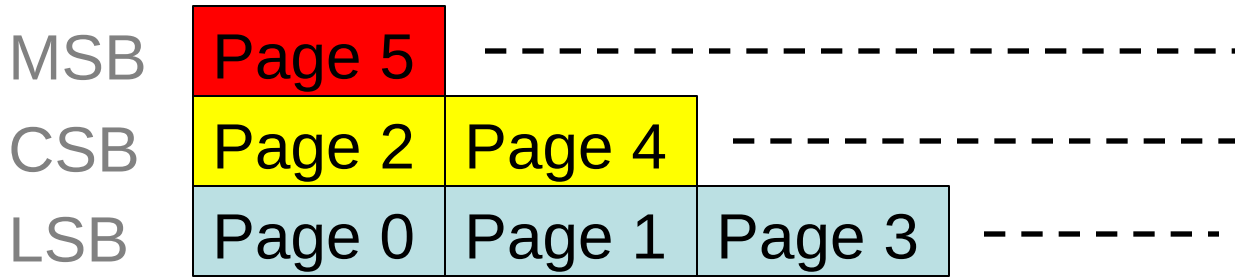
Ungraceful power off (Cont.)

- Page programming order:

LSB	CSB	MSB
0	2	5
1	4	8
3	7	11
6	10	14
9	13	15

Ungraceful power off (Cont.)

- Interrupted CSB page programming may damage lower LSB page
- Interrupted MSB page programming may damage lower LSB and CSB pages



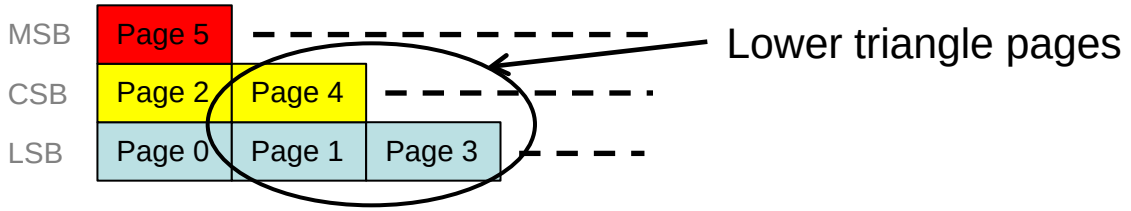
Ungraceful power loss (Cont.)

- Existing solutions:
  I. Soldered battery preventing ungraceful power-downs
     - Not applicable if battery is replaceable

  II. Use a super-cap that holds VDD until current page programming operation completes
     - Added cost
     - Form factor may not allow insertion of super-cap

Ungraceful power loss (Cont.)

- Existing solutions:
  - III. Recover past data prior to last interrupted transaction using stored backup data:
    1. Allocate a data “backup” block
    2. Pre/Post page programming operation: pages belonging to the lower triangle are “backed up”



  - Performance impact due to backup operation. Impact highest during short transactions

IV. DensBits solution uses a proprietary backup solution whose performance impact is less than 5%

Thank You