

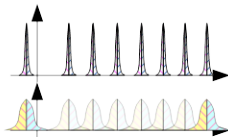
High-Efficiency SSD for Reliable Data Storage Systems

-Improving endurance and data reliability of next generation flash in embedded applications

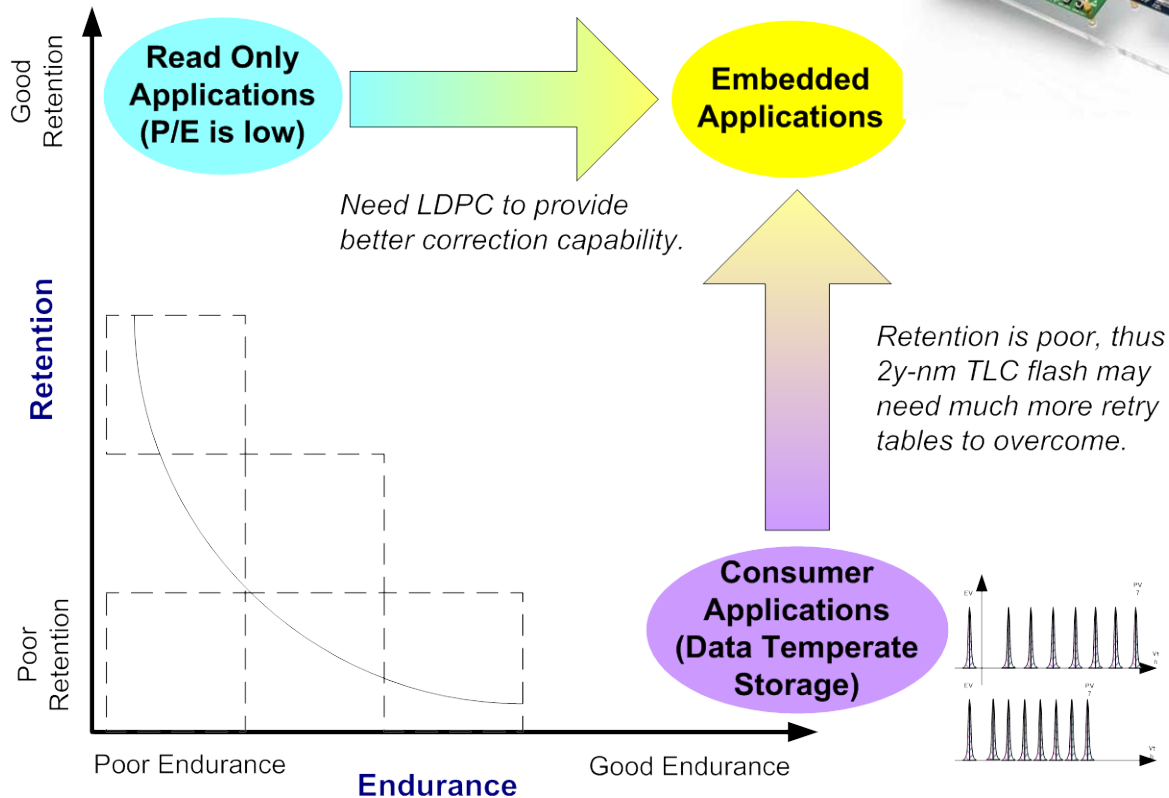
Jeff Yang
Principle engineer
Silicon Motion, Inc.
jeff.yang@siliconmotion.com

- The challenges of TLC flash in embedded applications
- The methods to overcome the retention and endurance disturbance
- Soft-decoding for larger noise
- Impact of soft-decoding
- Endurance enhancement of TLC flash
- Conclusion

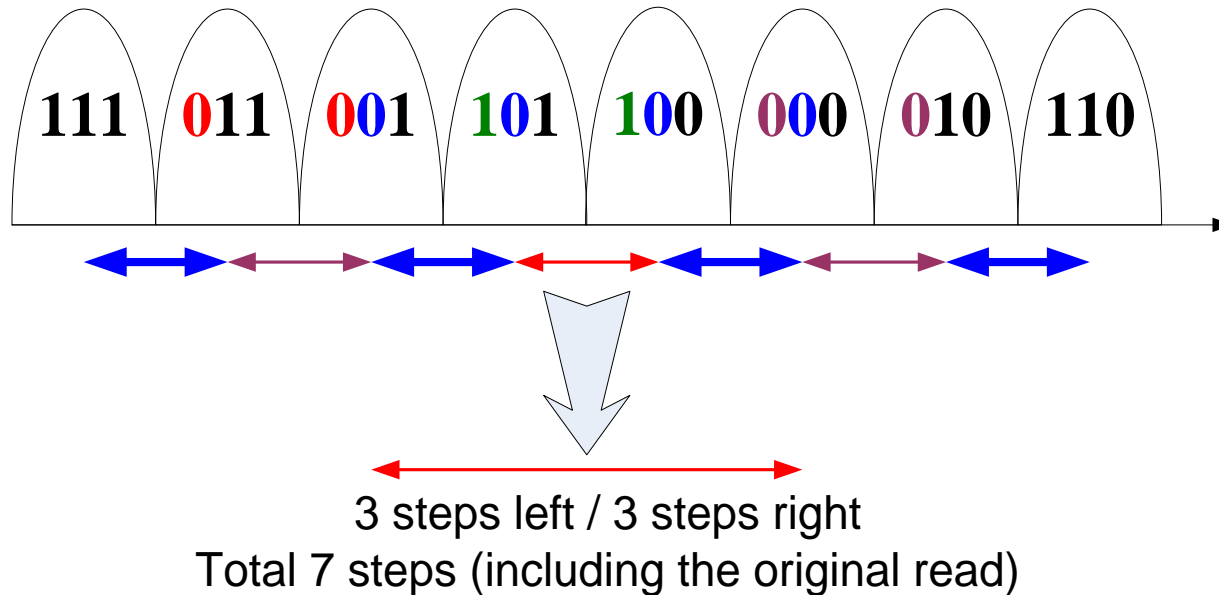
The Challenges of TLC Flash in Embedded Applications



Retention is good, but the error bits increase faster along with the P/E cycles.

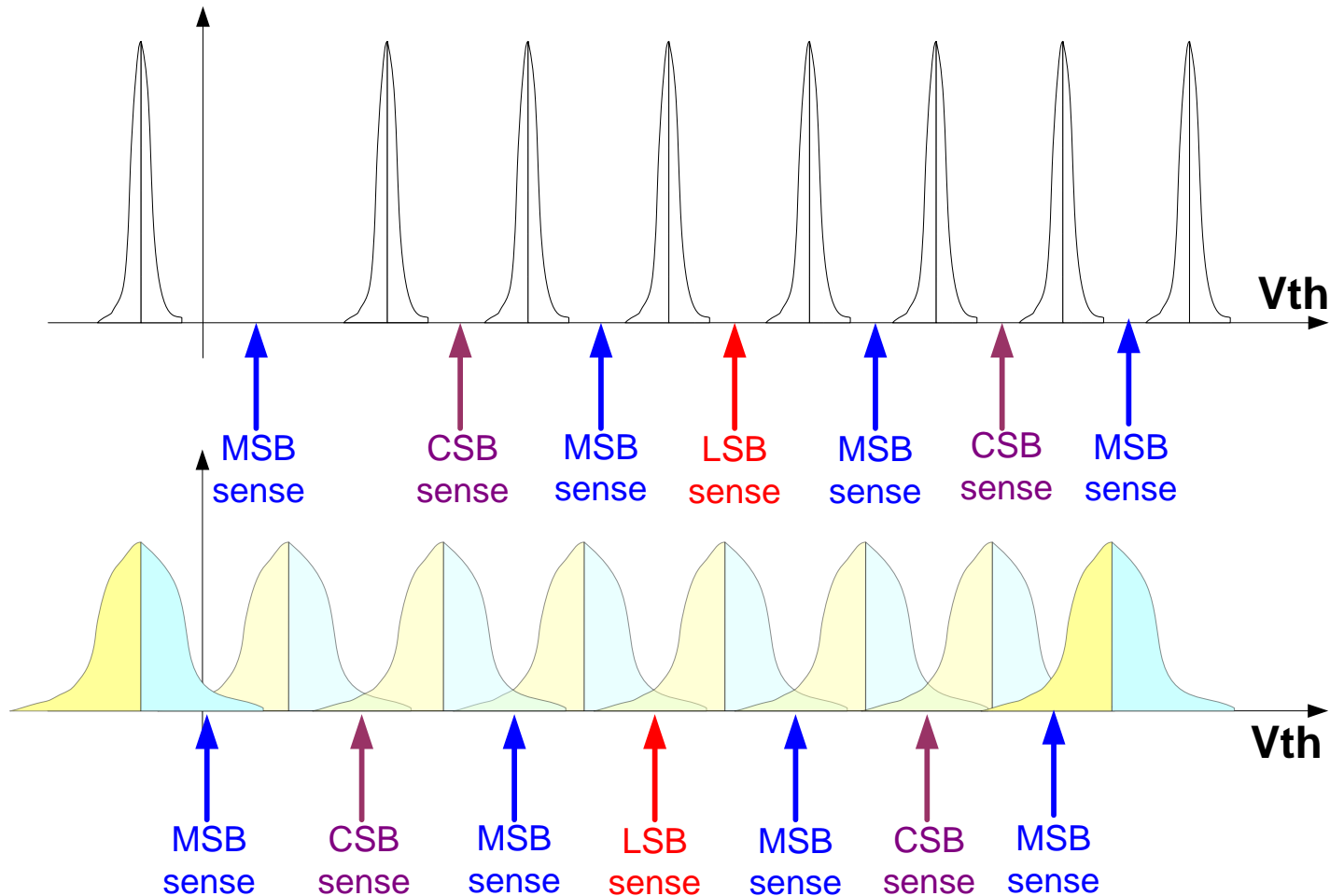


Read Retry Interface Mechanism

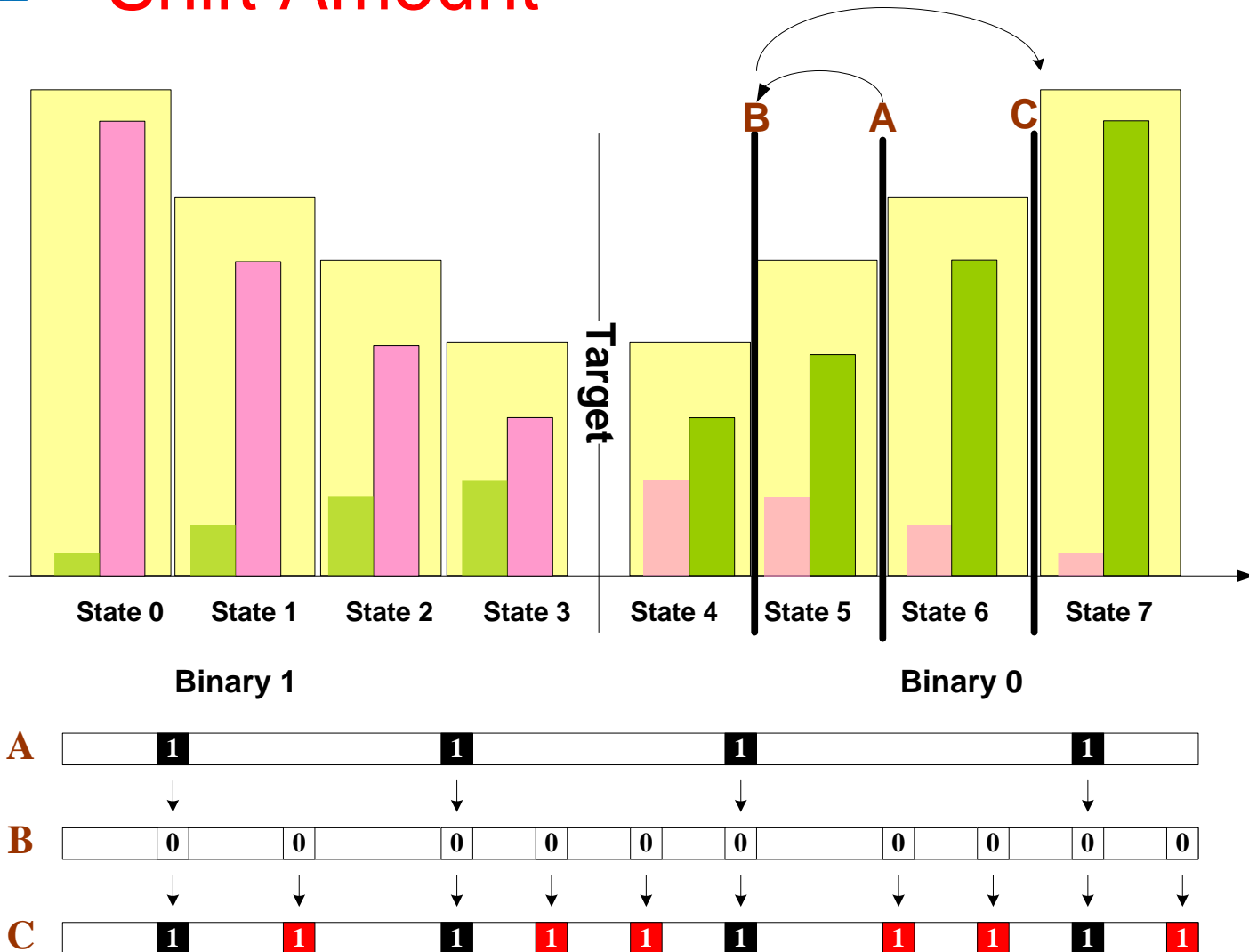


- The Read Retry Interface is typical in TLC flash.
- This interface can be used for:
 1. State distribution reconstruction
 2. Adaptive V_{th} tracking
 3. LDPC codes with soft-decoding (help correct more bit errors).

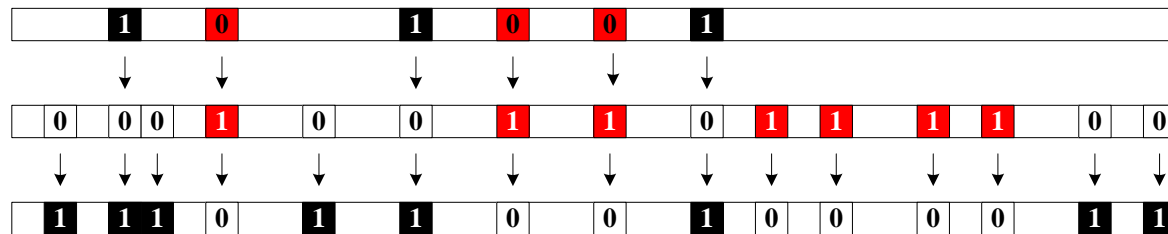
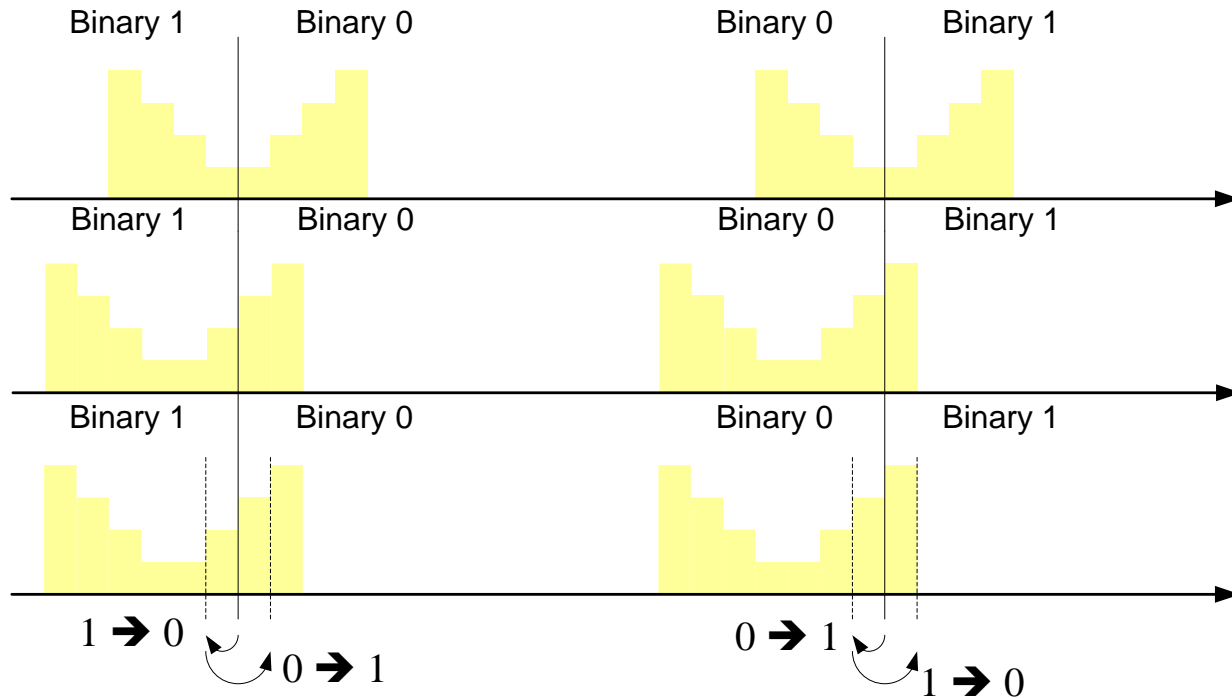
The Methods to Overcome Retention and Endurance Disturbance



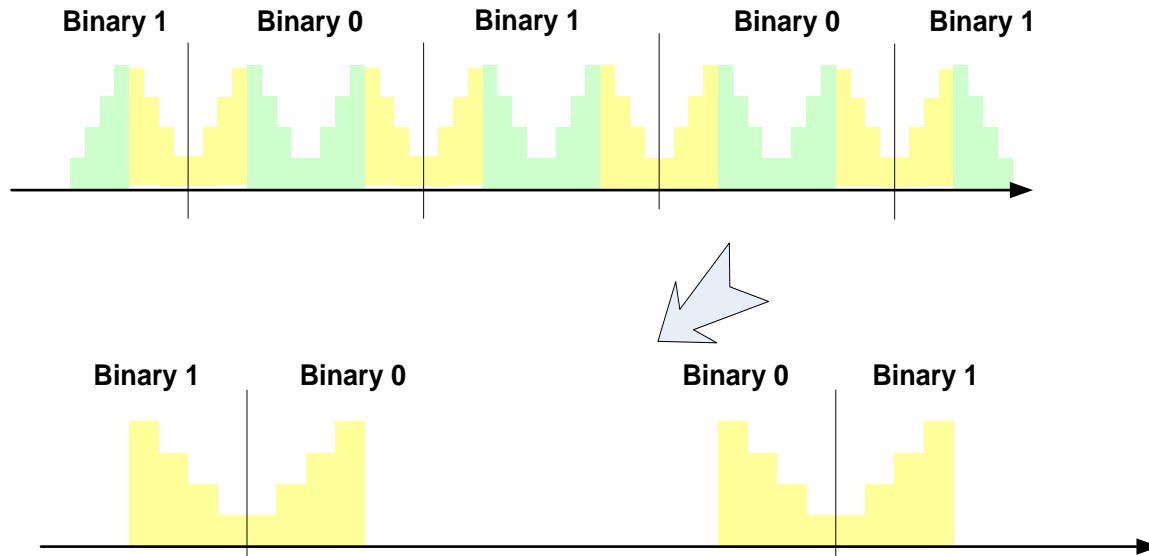
Detecting LSB Direction and Shift Amount



Detecting CSB Direction and Shift Amount

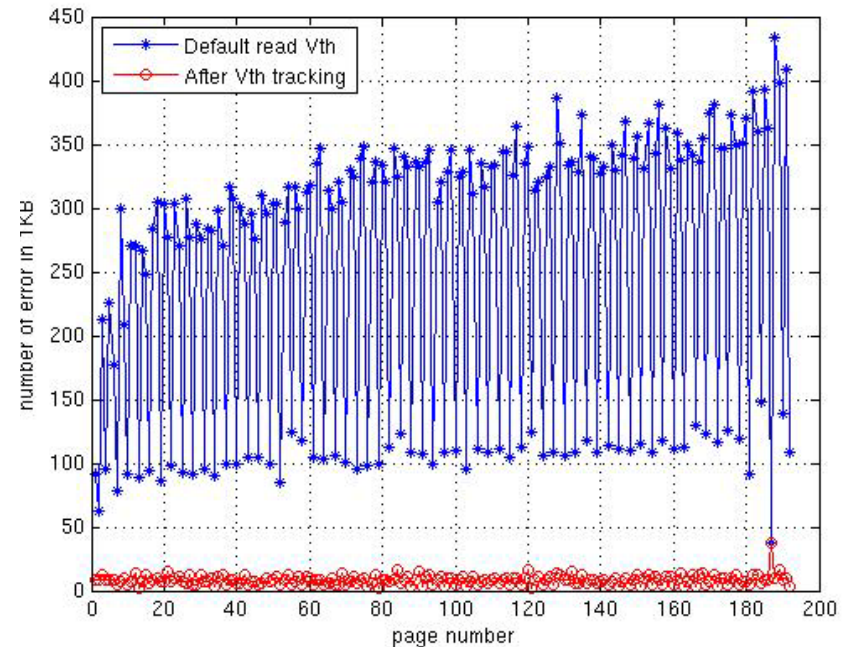
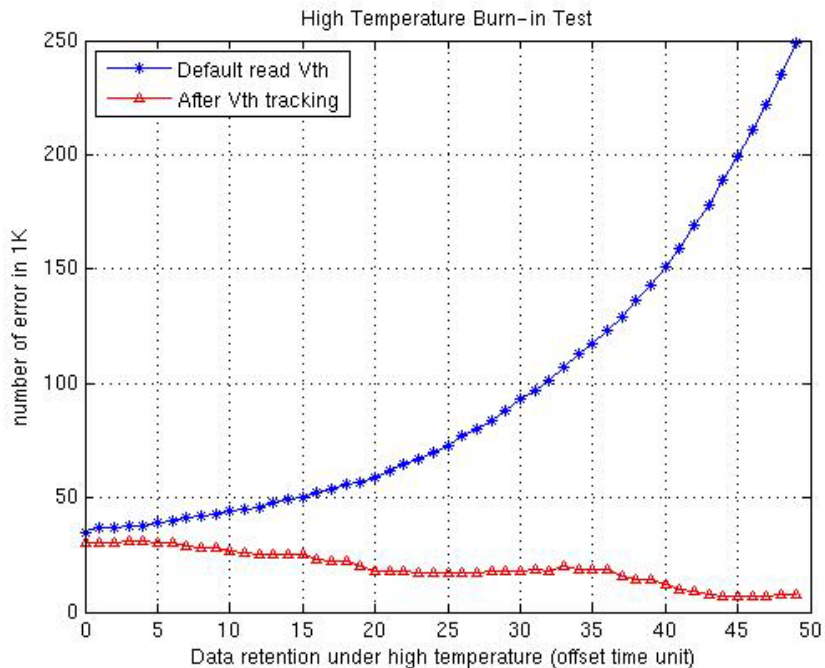


Detecting MSB Direction and Shift Amount



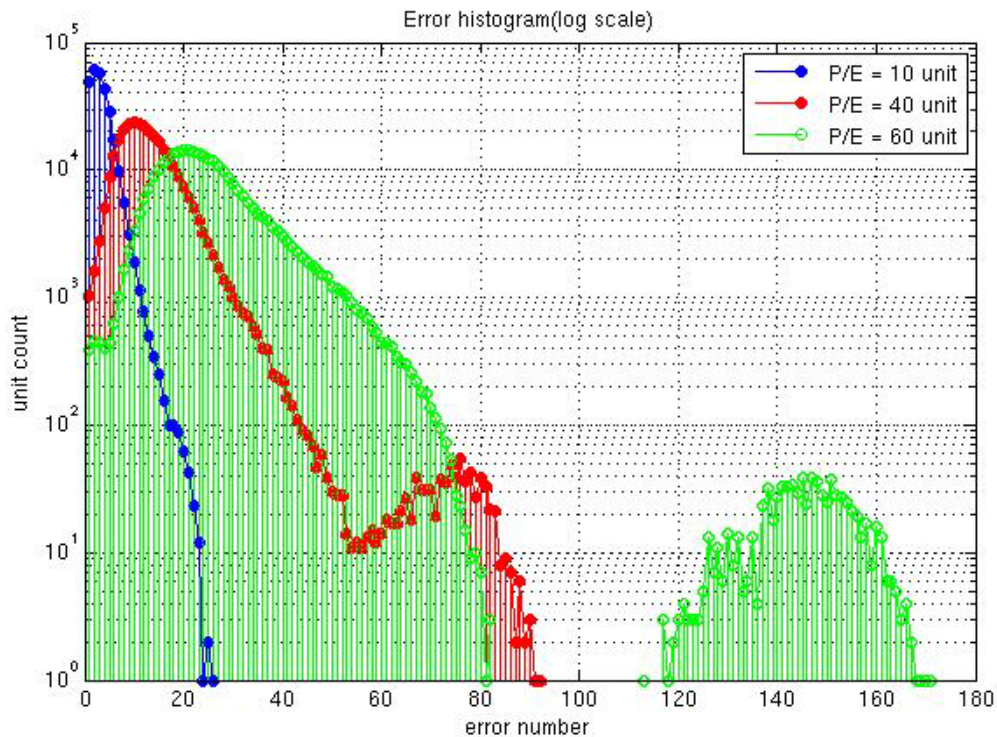
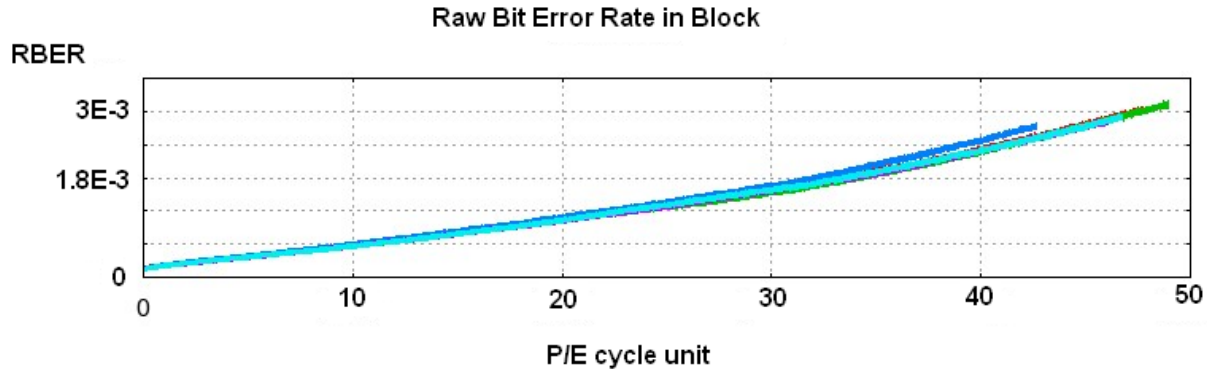
- The MSB Vth is equal to two CSB cases.
- The shift probability of the upper two Vth is greater than the lower two.
- When the lower two Vth values are fixed, shift the upper two Vth first and fine-tune them to the best location.
- If the upper two Vth values stay at the best location but are still uncorrectable, fix these values to the best location and shift the lower two Vth.

Tracking Vth in One Block

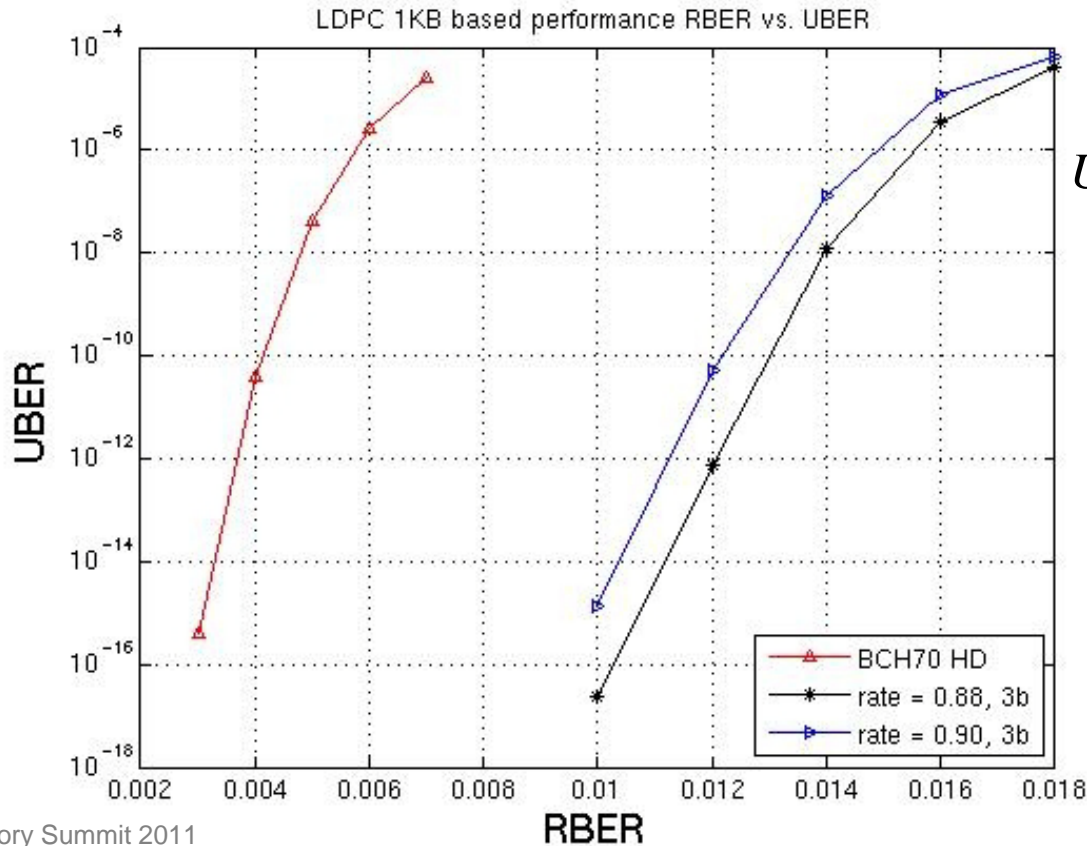
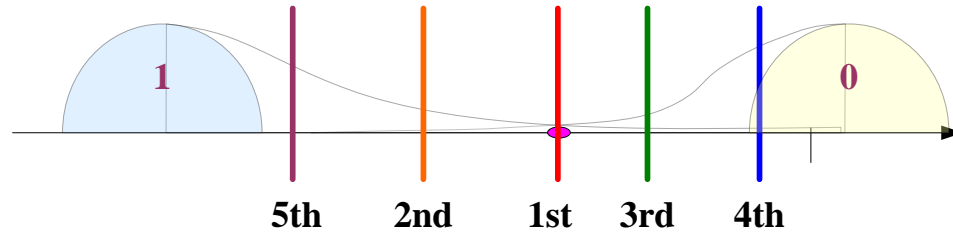


- The data in the same block suffers similar disturbances.
- Only the first page applies the detailed Vth tracking.
- All the pages other than the first page follow the previous page's Vth location, and the location for the next page is going to be fine-tuned.
- After Vth tracking, the pure noise effect shall be taken into account.

Soft-Decoding for Larger Noise



Performance of LDPC Soft-Decoding over AWGN

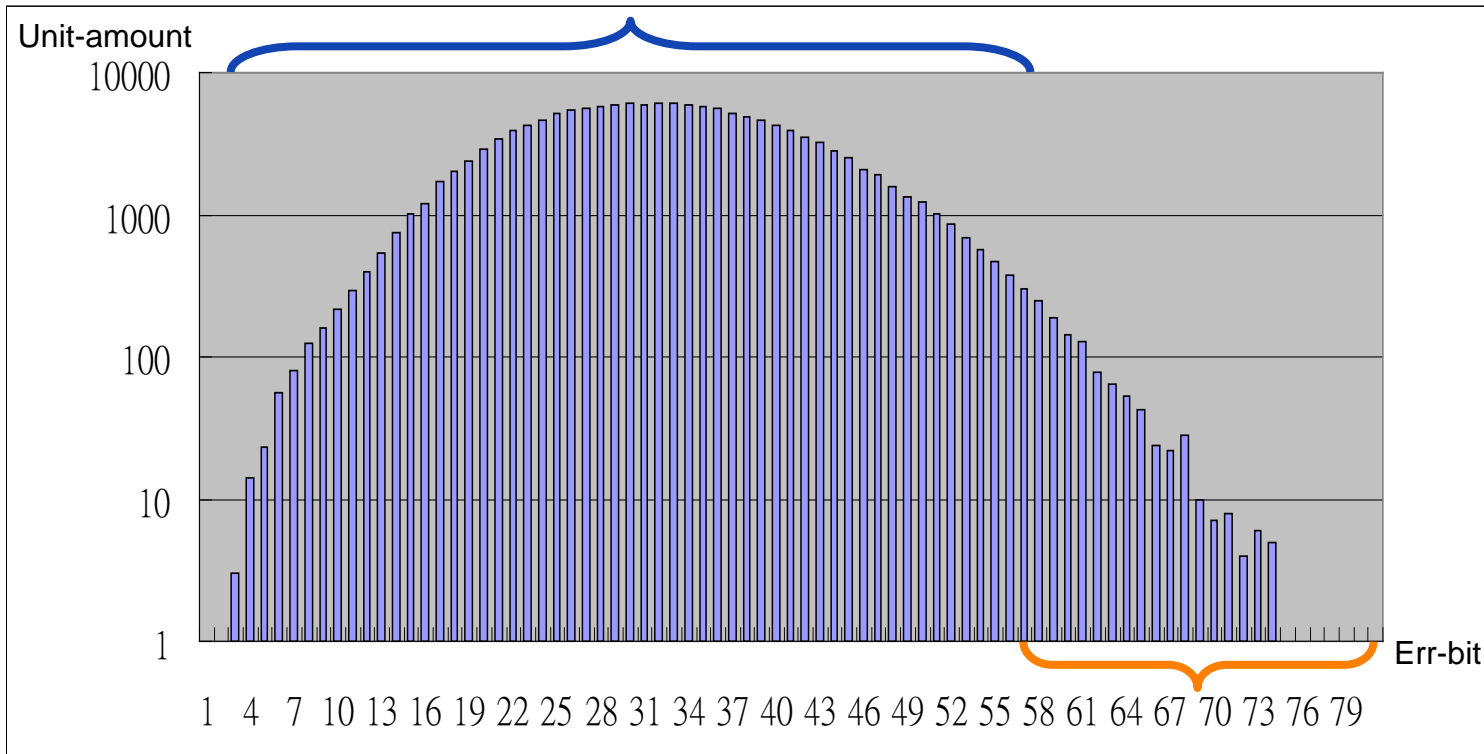


$$UBER = \frac{\text{codeword error rate}}{\text{message bit}}$$

$$= \frac{\text{codeword error rate}}{8192 \text{ bit}}$$

LDPC Real Endurance Test

LDPC hard-decoding can correct most of errors since the flash storage system behaves like BCH.



BCH is unworkable, but LDPC soft-decoding is workable.

The test shows LDPC provides a highly reliable system.

Impact of Soft-Decoding

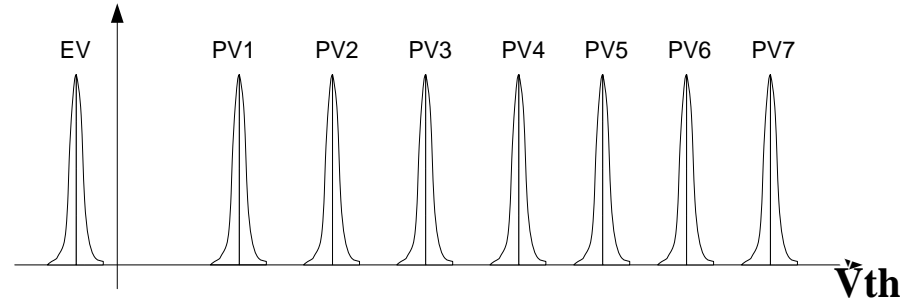
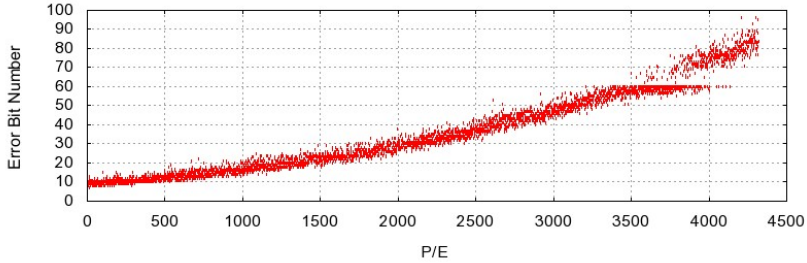
- Soft-decoding improves the data storage reliability.
- Acquiring soft information will consume more power on read.
- The higher transfer throughput of flash interface is required.
- The 1KB-based LDPC decoder for USB/SD2.0 applications is around four times as complex as the BCH decoder with the same constraints (code rate, message length, etc.)
- The overall gate counts of USB/SD2.0 controllers turn into double when the BCH is replaced by LDPC.

Additional Benefits of Flash Controllers with LDPC

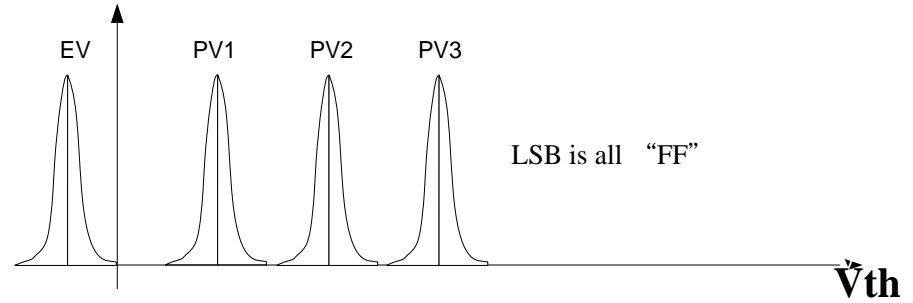
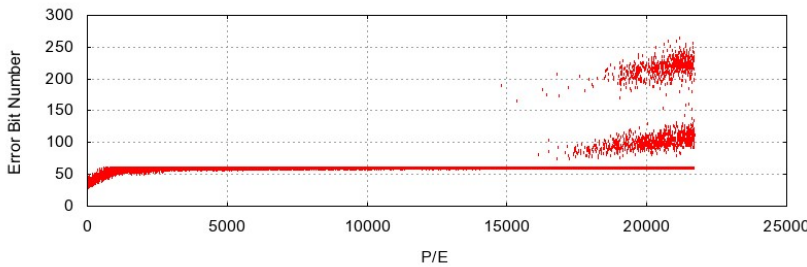
- The testing cost increases as the NAND flash process continues to advance (3x → 2x → 2y → 1x nm).
- The testing cost of high-capacity flash chip (8/16 GB above) may be close to, or exceed the controller's price.
- Examples:
 - A: Flash controller with BCH + flash-die cost
→ Lower yield + higher testing cost
 - B: Flash controller with LDPC + flash-die cost
→ Higher yield + lower testing cost
- Example B may be a better cost-efficient solution.

Examples of Different Endurance Performance in 4GB TLC Flash

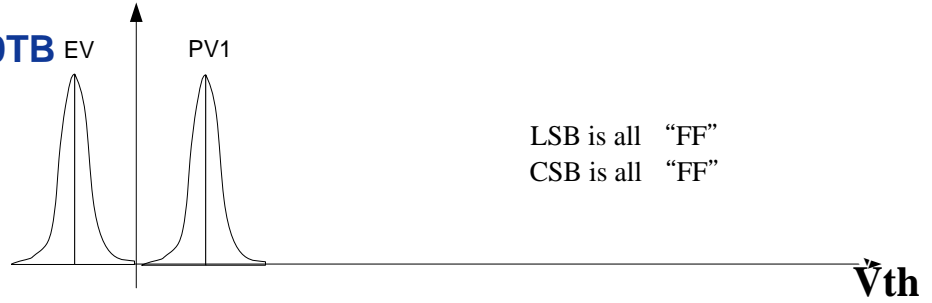
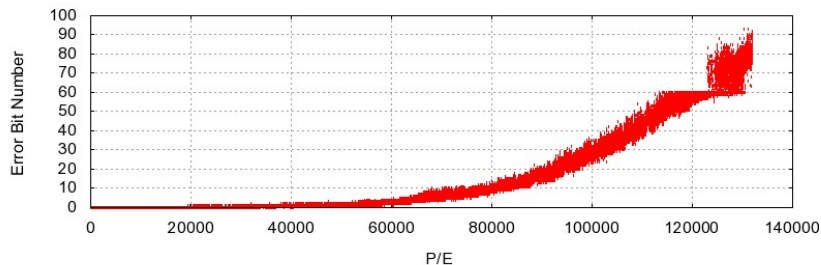
Max Error Bit(1K) **4GB x 4K = 16TB**



Random Max Error Bit(1K) **2.6GB x 20K = 53TB**

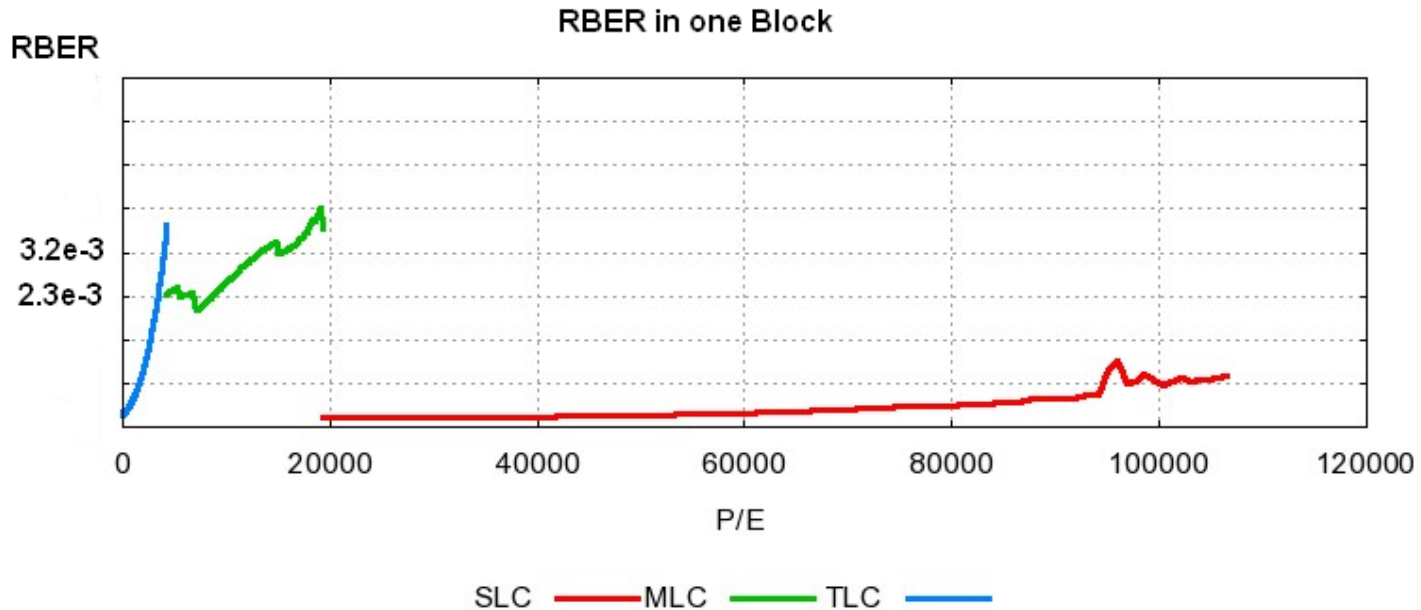


Max Error Bit(1K) **1.3GB x 120K = 160TB**



ReliableMode

Endurance Enhancement of TLC Flash



- In some applications, only the wear capacity (not the data capacity) needs to be considered:

- TLC access period: 4GB x 4K (cycle) = 16TB
- MLC access period: 2.6GB x 16K (cycle) = 41.6TB
- SLC access period: 1.3GB x 80K (cycle) = 104TB
- Total media-wear capacity = 160TB

10X improvement

- Vth tracking and LDPC soft-decoding provide a good error correction capability to reduce the endurance and retention disturbance.
- With the endurance enhancement, TLC flash can fit in a variety of embedded applications.
- Silicon Motion's NAND flash controllers equipped with robust LDPC decoding engine offer one of the best cost-efficient systems and are ready for tests and validations.



Thank You!

Q & A