Improving NAND Reliability with Low-Density Parity Check Codes (LDPC)

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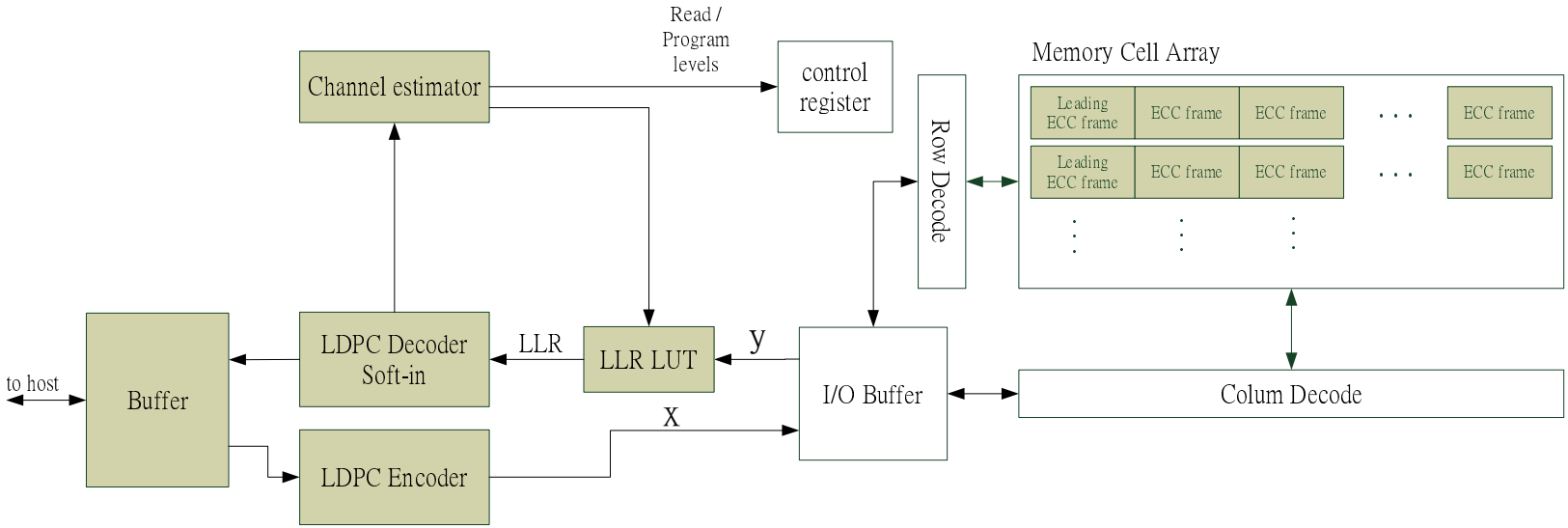
PHISON

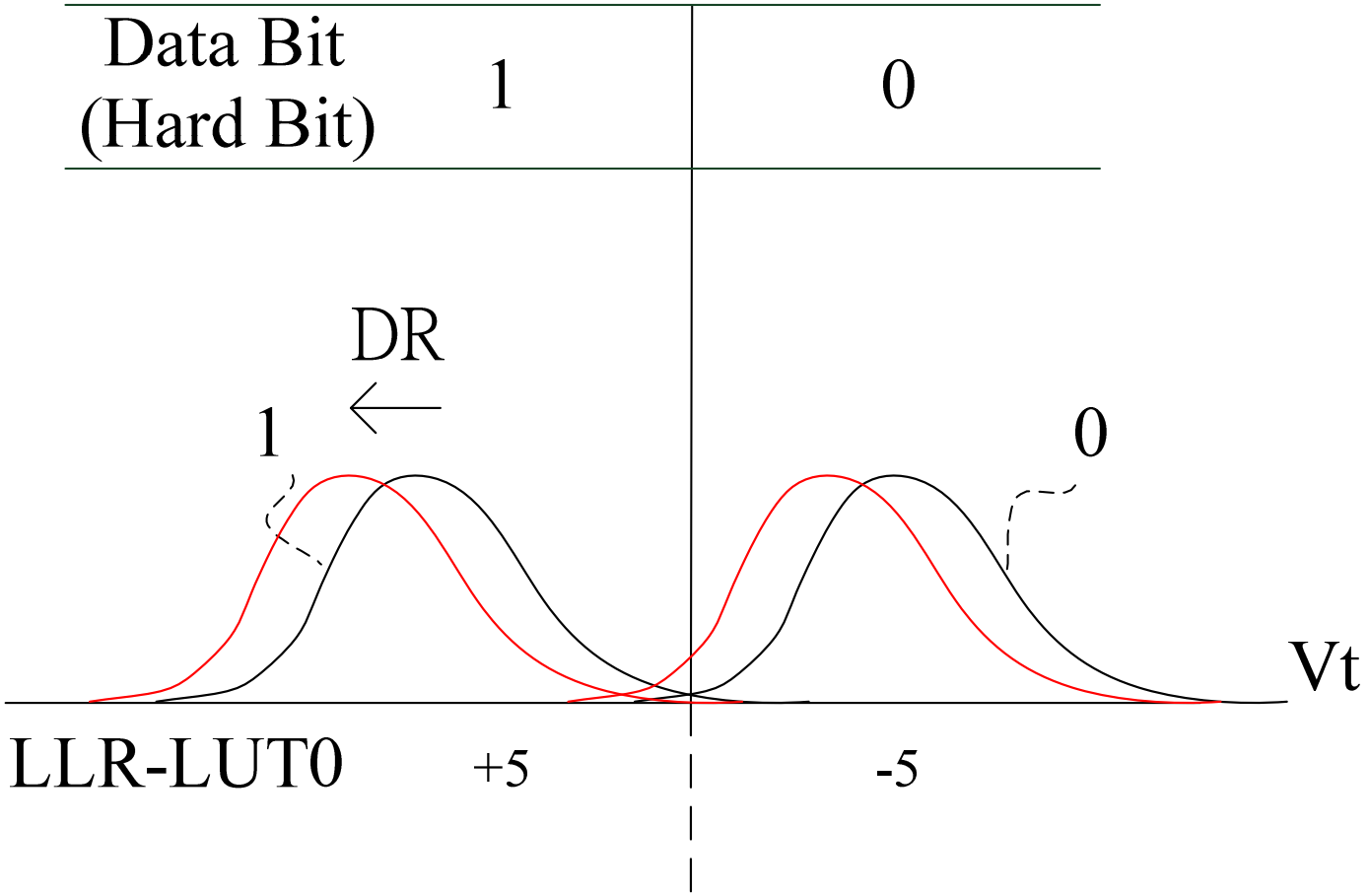
Log-Likelihood-Ratio (LLR)



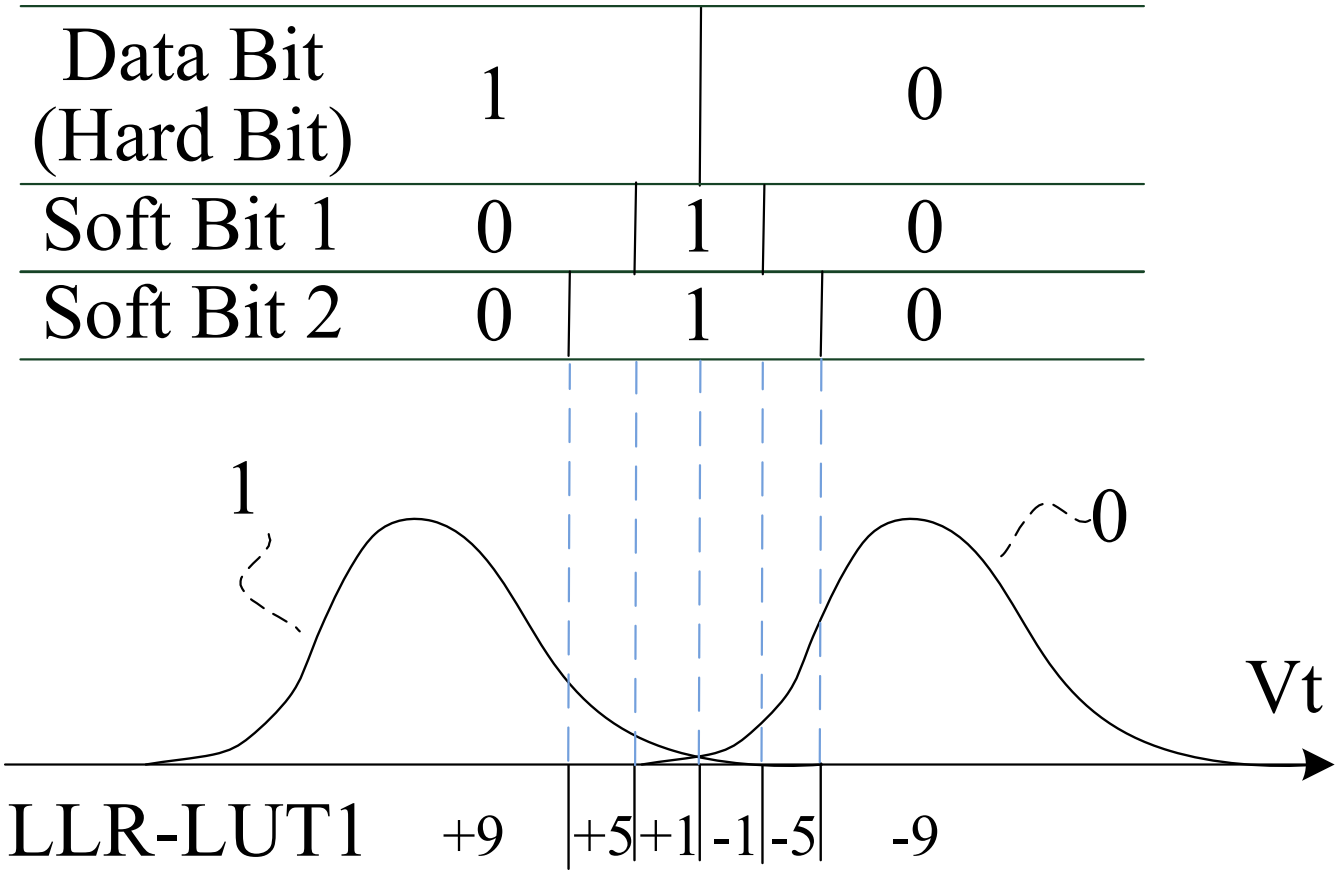
$$LLR(y) \triangleq \log\left[\frac{P(x=1 \mid y)}{P(x=0 \mid y)}\right]$$

LLR value	Representation
+9	Input bit is very likely to be “1”.
+1	Input bit is likely to be “1”.
-1	Input bit is likely to be “0”.
-5	Input bit is more likely to be “0”.

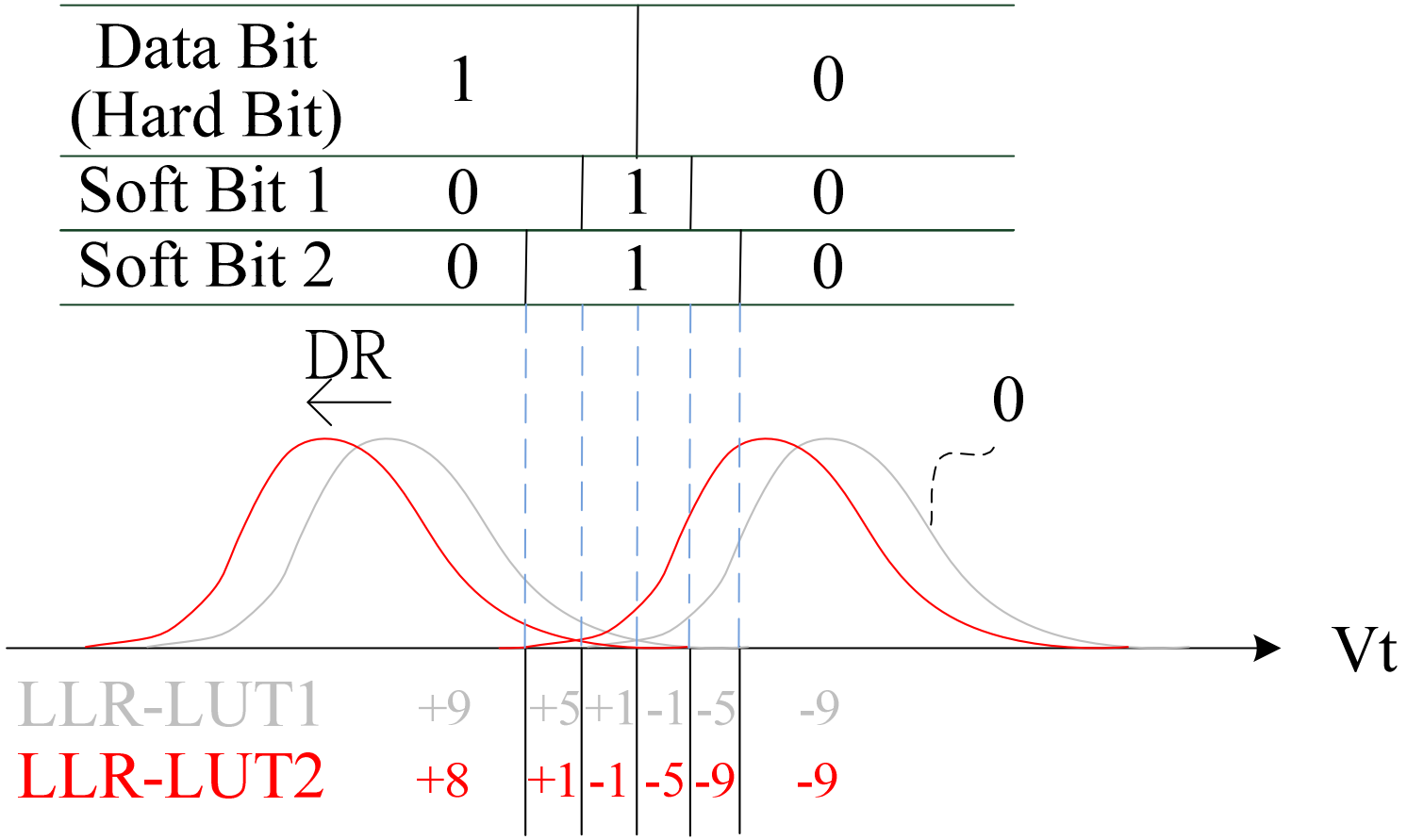
LLR-LUT0 for Data (HB)



LLR-LUT1 for HB & SB



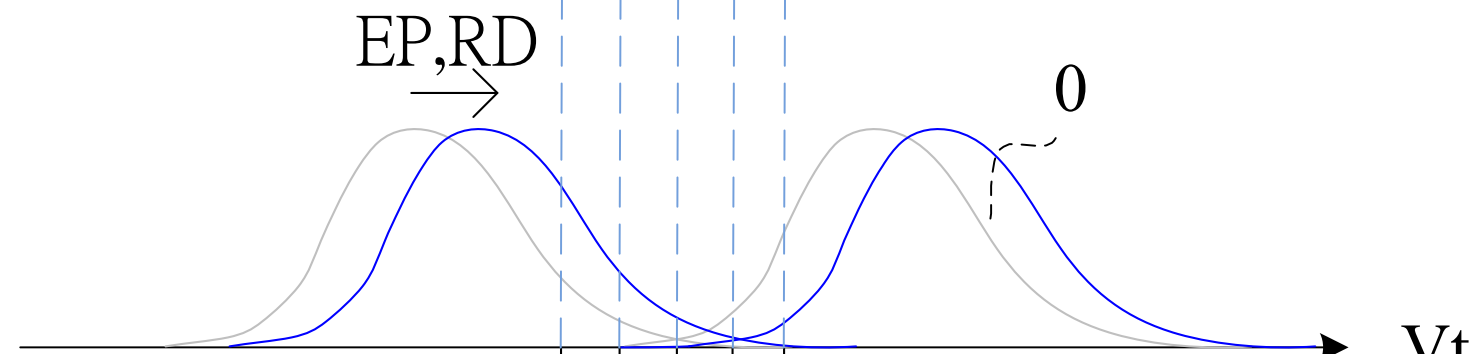
LLR-LUT2 for Data Retention (DR)



※ Eliminate the most of error bits by changing to LLR-LUT2

LLR-LUT3 for Usage

Data Bit (Hard Bit)	1		0
Soft Bit 1	0	1	0
Soft Bit 2	0	1	0

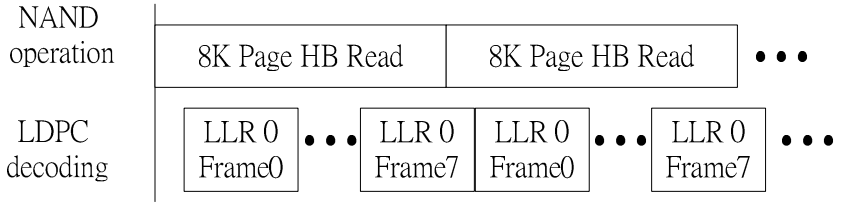


LLR-LUT1	+9	+5	+1	-1	-5	-9
LLR-LUT2	+8	+1	-1	-5	-9	-9
LLR-LUT3	+9	+9	+7	+2	-1	-8

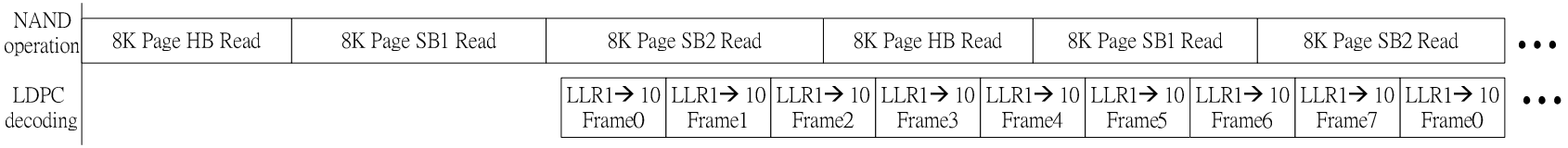
※ Eliminate the most of error bits by changing to LLR-LUT3

LDPC Decoding Process

- 1. HB Decoding Mode (similar to BCH)

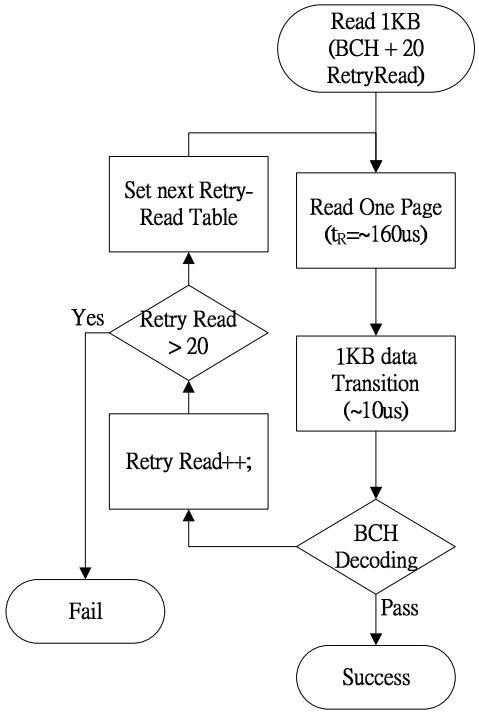


- 2. SB Decoding Mode

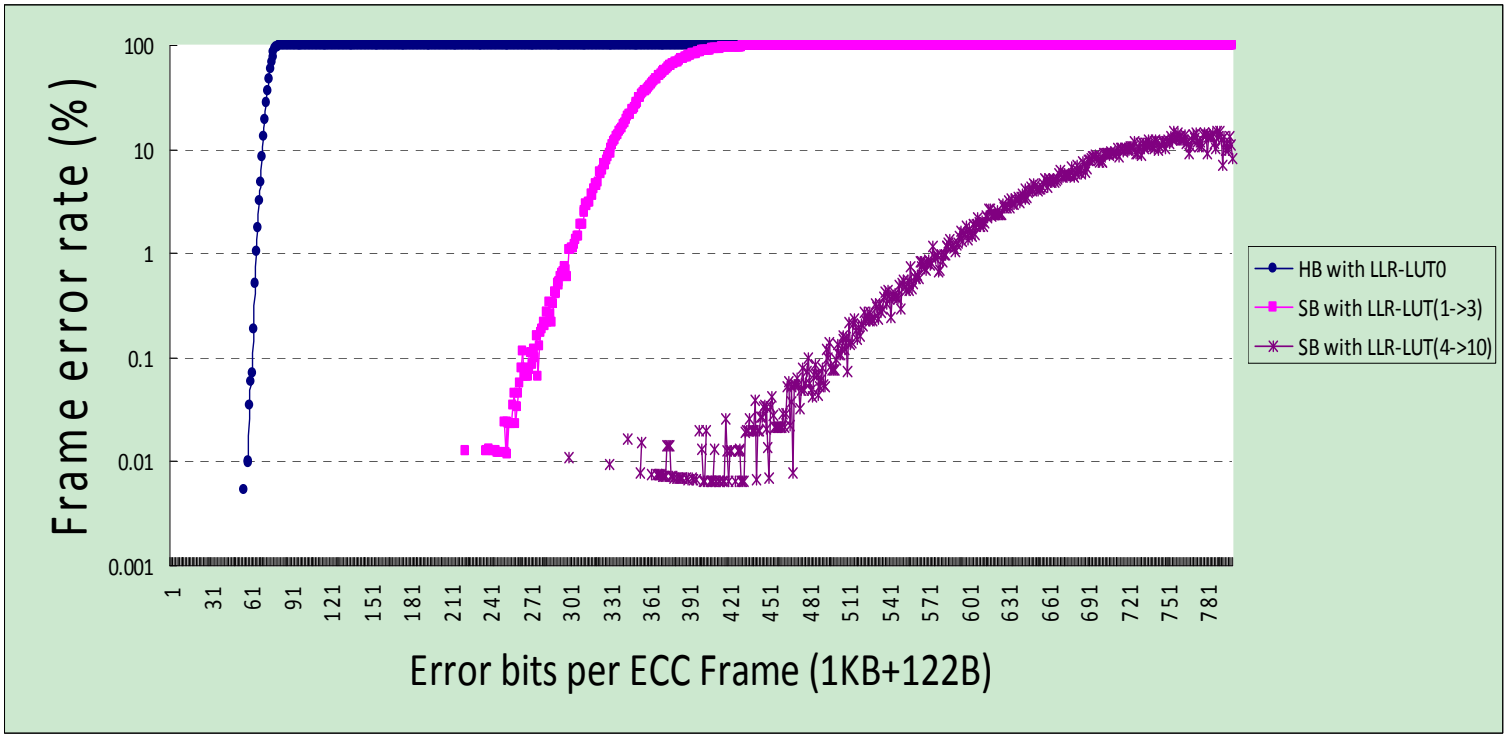


LDPC vs. BCH

	BCH	BCH + 20 RetryRead	LDPC HB	LDPC HB &SB + LLR-LUT (1→10)
Latency	Low	High	Low	Medium
Gate Counts	Small (t≦68 per 1KB)		Large (t~200 per 1KB)	
Correction Capability	Limited	Better	Better	Best



LDPC solution Testing on real TLC-NAND (Page size=8KB+976B)



※ Test Condition : 1. EP 2. EP+DR1Year

※ Test frame amount : 8,064,717

Proposed LDPC solution for the next-generation NAND (8KB+1072B)

- Compare Correction Capability with BCH on AWGN Channel:

Page Size	LDPC HB only (ECC frame:1KB)	LDPC HB&SB
8KB+976B (available NAND)	~68bits BCH (~100%x68bits BCH)	~136bits BCH (~200%x68bits BCH)
8KB+1072B	~93bits BCH (~127%x73bits BCH)	~192bits BCH (~260%x73bits BCH)