



# Current and Emerging Memory Technology Landscape

Greg Atwood

Micron Technology

[Gatwood@Micron.com](mailto:Gatwood@Micron.com)

# A New Era Emerging for Memory?

## Convergence of many factors/pressures:

- Increasing importance of memory to user experience
  - Our lives are becoming one big shared database, with IOPs becoming more important than MIPs
- Both NAND and DRAM facing scaling challenges
  - No hard “wall,” but increasing complexity
- Explosion of “new” memory storage concepts
  - New storage physics are enabling new usage models
- Evolving memory hierarchy
  - New features, relentless cost reduction, and need for I/O performance are remaking the memory hierarchy

**Memory is moving from a support role to a defining system role**

# Memory-Relevant Trends

## Enterprise

(Servers/Storage)

- Performance-driven (generally I/O limited)
- “Green” focus bringing power into foreground
- Reliability vs. cost is the trade-off

## Computing

(Desktops/Laptops)

## Mobile

(Laptops/MIDs)

- Ease of use
- Instant-on/off
- Power vs. “good enough” performance trade-off

## Cellular

(Phones)

# Memory Scaling Challenges

Just as memory usage becomes “interesting”...

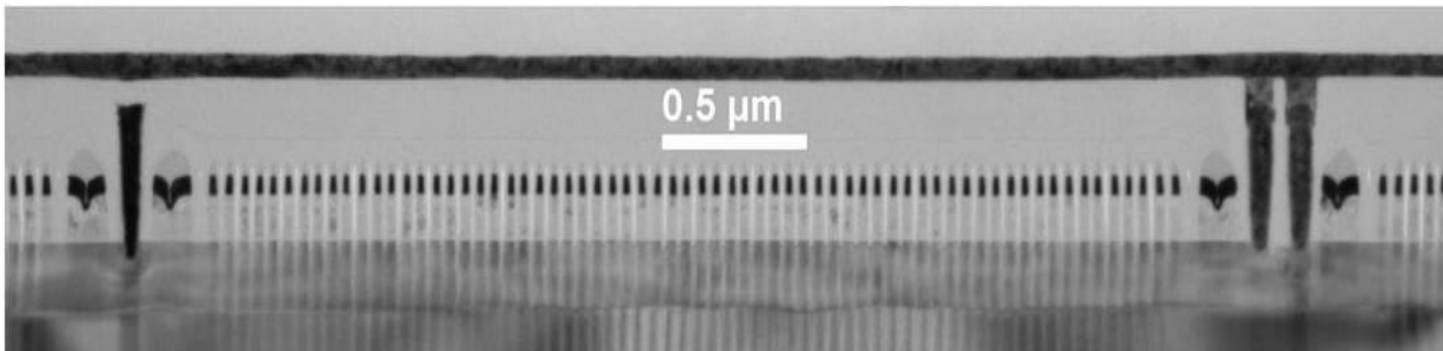
- “Planar” nonvolatile (NVM) technology scaling is becoming difficult:
  - MOS transistor-based cell; charge-storage memory effect
  - Starting to encounter physical scaling limitations
  - Manifesting first as reliability → endurance/retention
  - Increasing degree of memory management required for functionality → memory abstraction
- No scaling “brick wall,” but complexity is increasing the level of management required to maintain added functionality

# Flash Cell Scaling Challenges

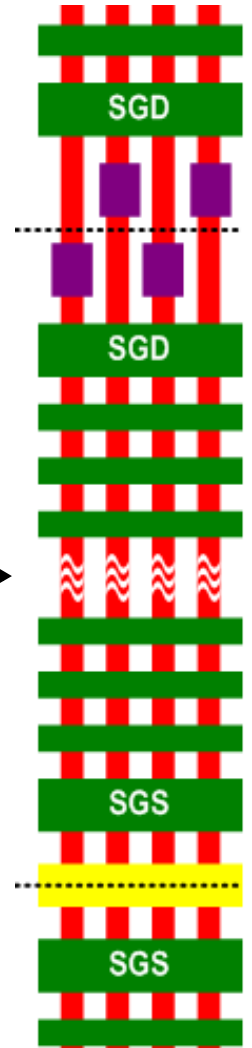
Basic NAND structure has changed little over time...

Main scaling issues:

- Few-electron problem
- Capacitance limitations
- Tunnel and interpoly charge retention
- Voltage isolation
- Parasitic charge trapping
- Read and write noise



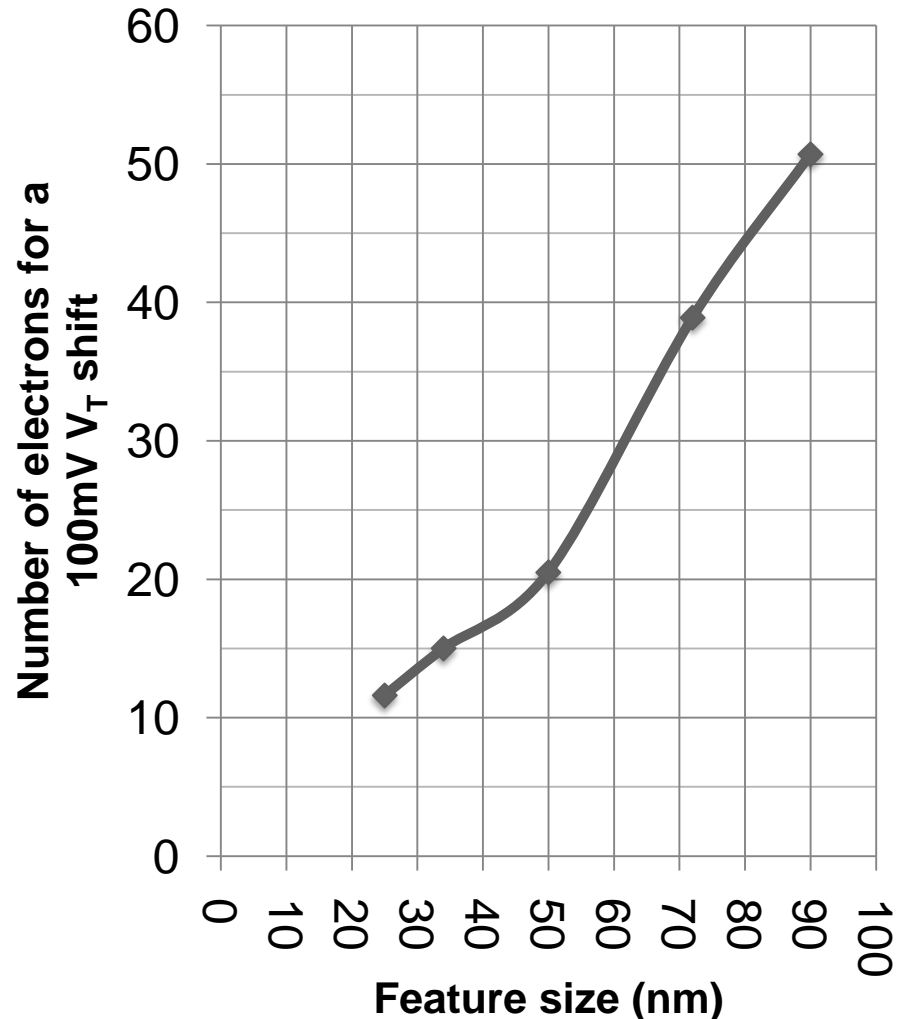
*State of the art:  
25nm NAND*



# Few-Electron Effect

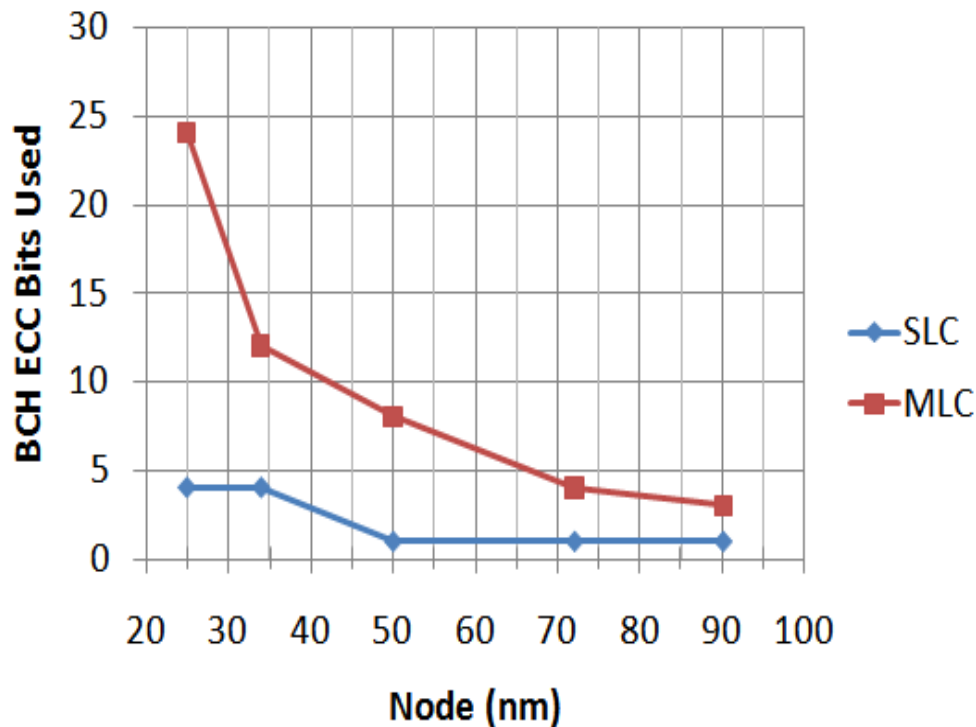
For a floating-gate cell, the number of electrons required for a  $V_T$  shift scales with the FG capacitance

At 25nm, MLC states are separated by 30–50 electrons (300–500mV)



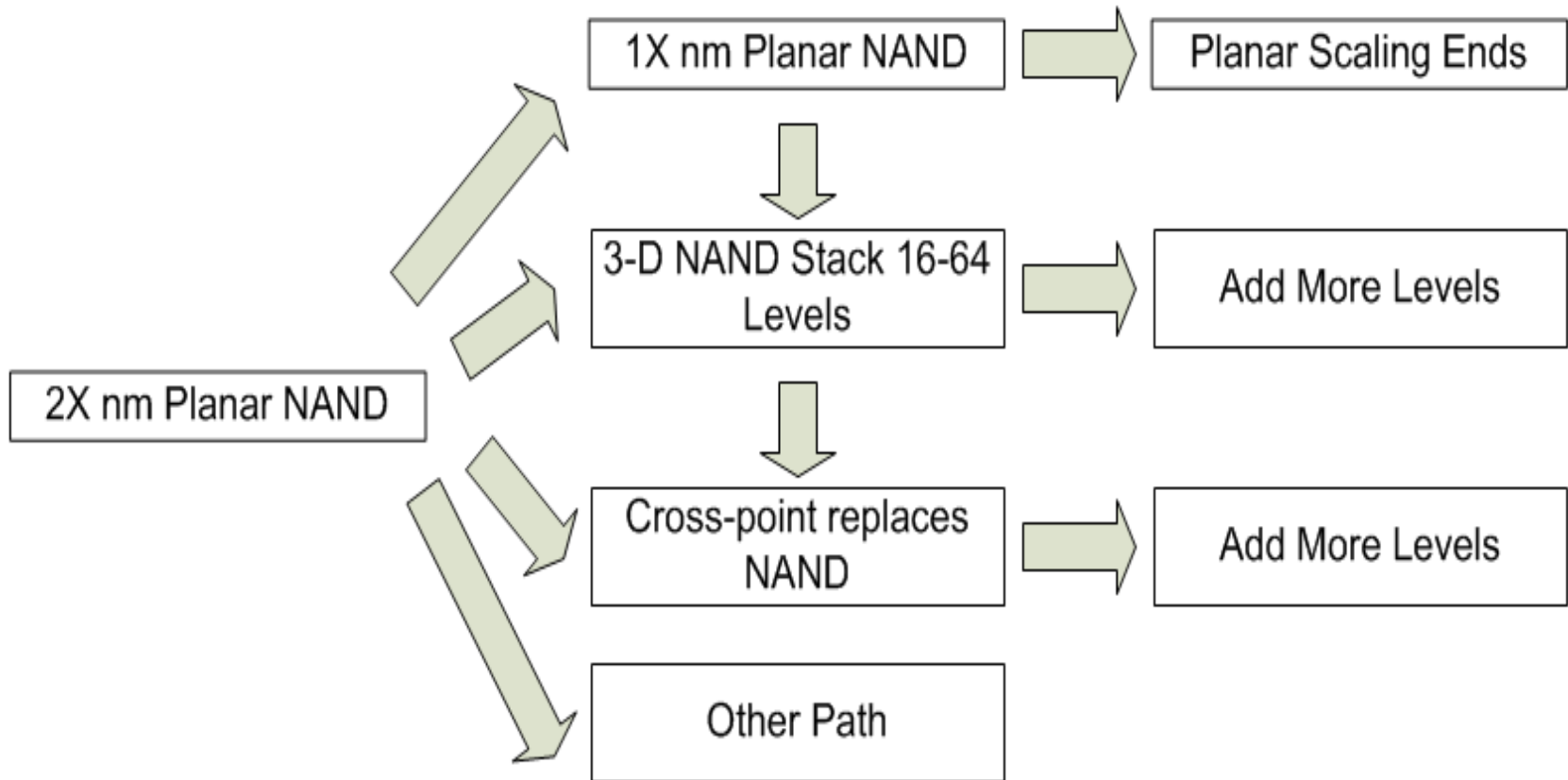
# Scaling at a “System Level”

NAND media scaling issues are being addressed through system-level management tools such as error correction, wear leveling, and block retirement—  
but **straightforward options are being exhausted**



# NAND Scaling Roadmap

Several possible scenarios...

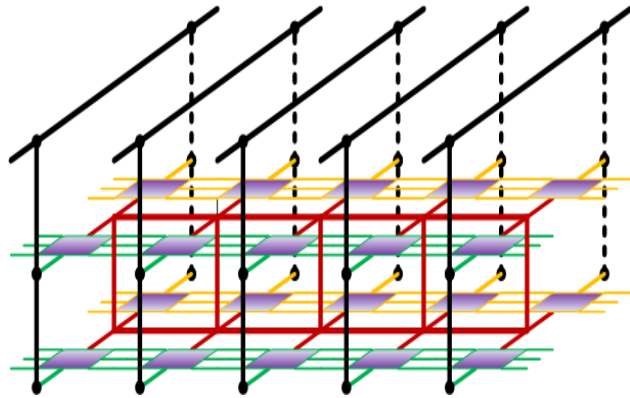




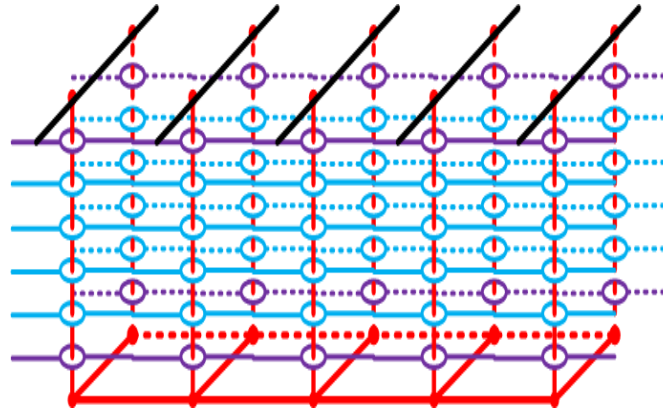
# Going 3-D → Three Major Options

- **Deck-by-deck NAND** – SOI for upper decks
- **Vertical NAND** – Vertical cells arranged in vertical strings
- **Cross-point** – RRAM (resistive RAM) cells

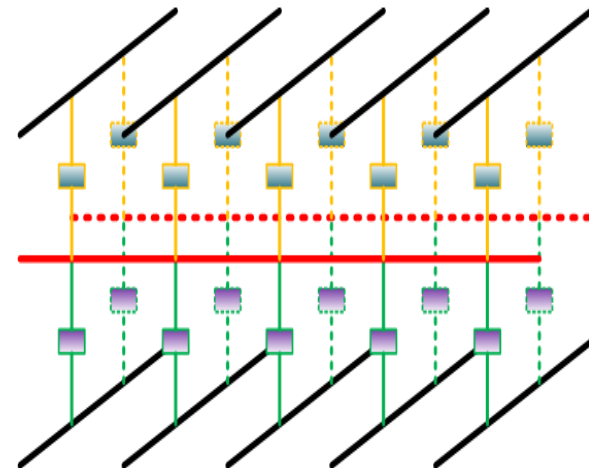
**Deck-by-Deck  
NAND**



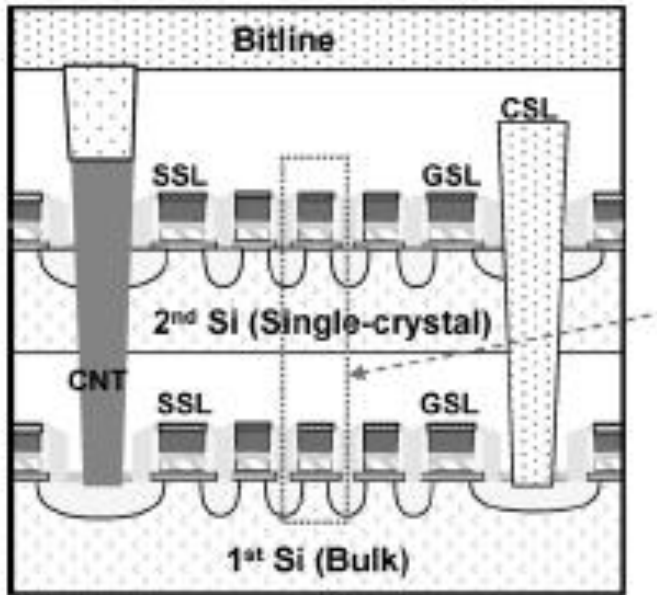
**Vertical NAND**



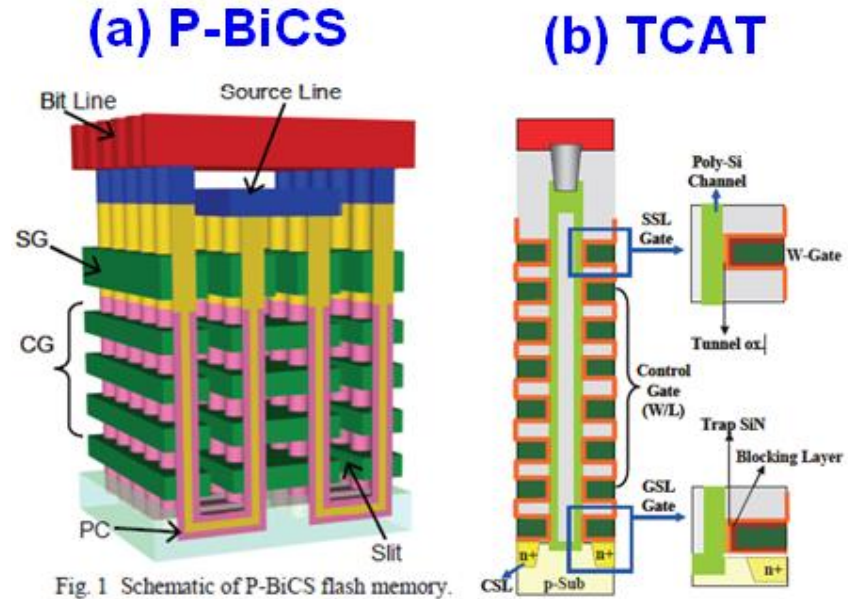
**Cross-point  
RRAM**



# 3-D NAND Highlights



**Deck-by-Deck: Dual-Deck**



**Vertical NAND**

- Significant industry effort on 3-D NAND development
- Conference publications showing promising results
- Possibility to extend NAND roadmap for several generations

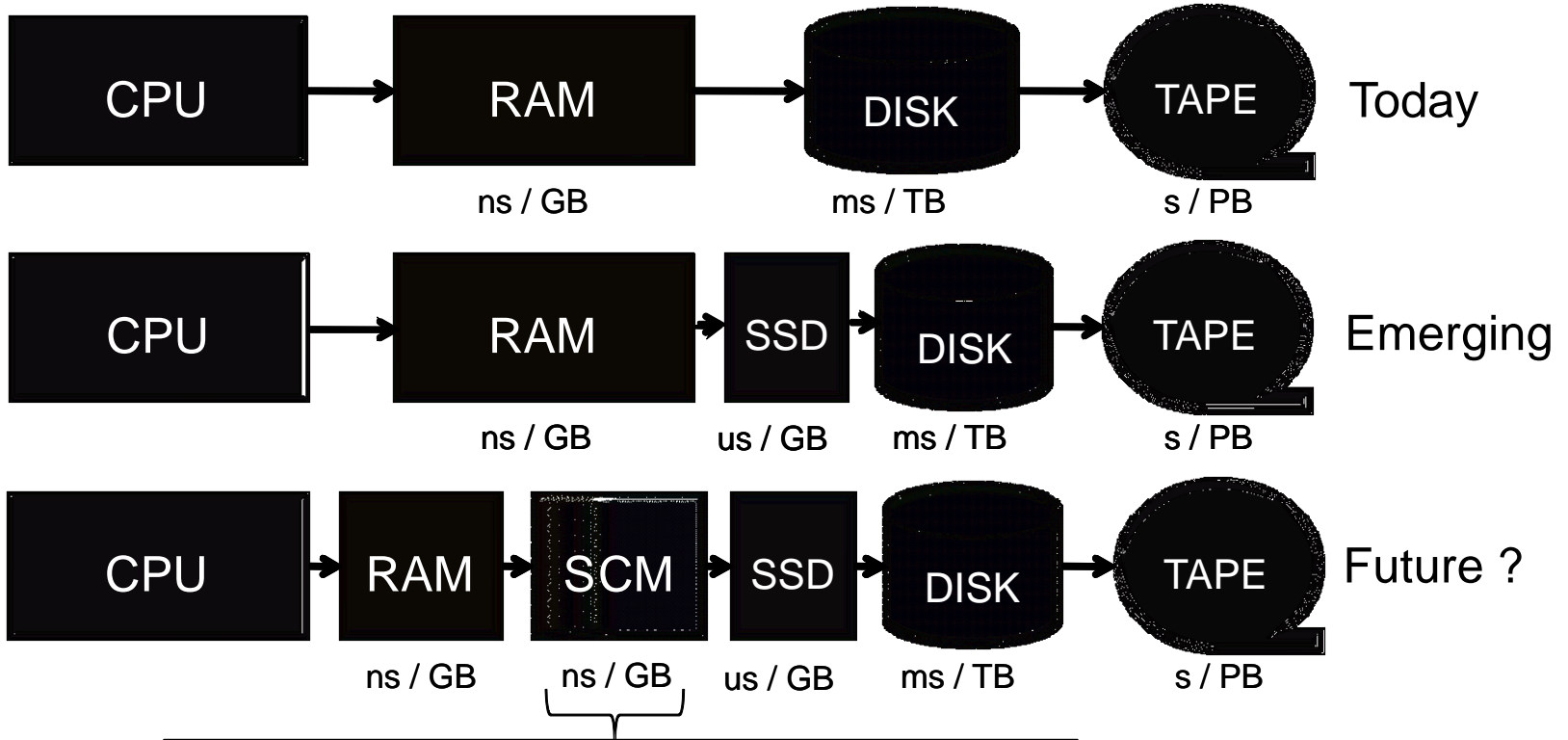
# Requirements for NAND Successor

- Cost structure – beat NAND costs:
  - MLC-capable
  - 3-D-stackable
  - Simple process flow
  
- Scalability:
  - In x & y with lithography
  - In z with number of layers
  
- Reliability, performance, and power:
  - To meet emerging usage requirements
  - At component and system level

# NAND Successor Not the Only Target

## New Memory Hierarchy?

Balancing Latency, Power, Cost, and Endurance



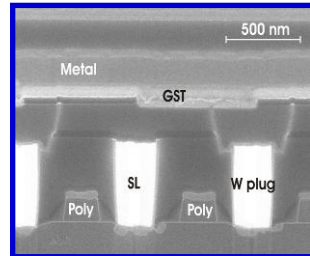
Latency ~ RAM Power ~ NAND  
 Bit Alterability ~ RAM Endurance >> NAND  
 RAM > Cost > NAND

# Alternative New-Memory Concepts

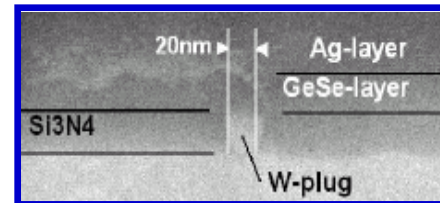
## FERAM



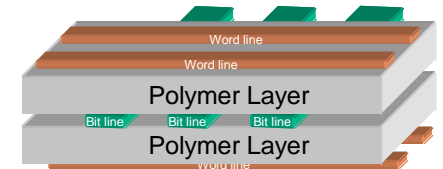
## PCM



## CBRAM



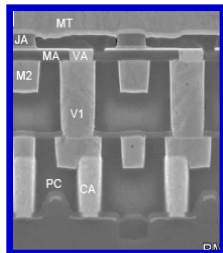
## Polymer FeRAM



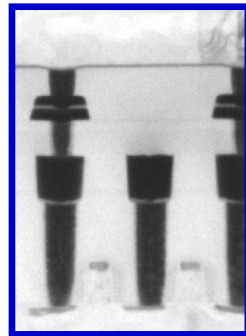
## CNT



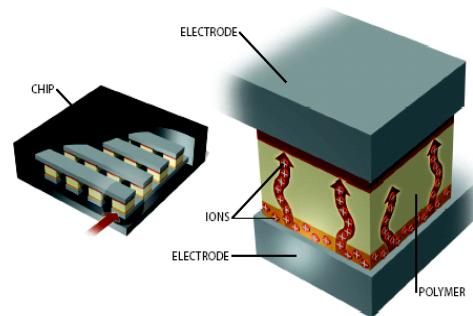
## MRAM



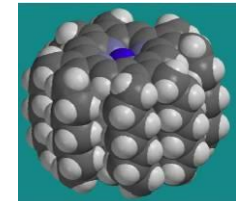
## MOx-RRAM



## Polymer RRAM



## Molecular



Explosion of “new” memory concepts:

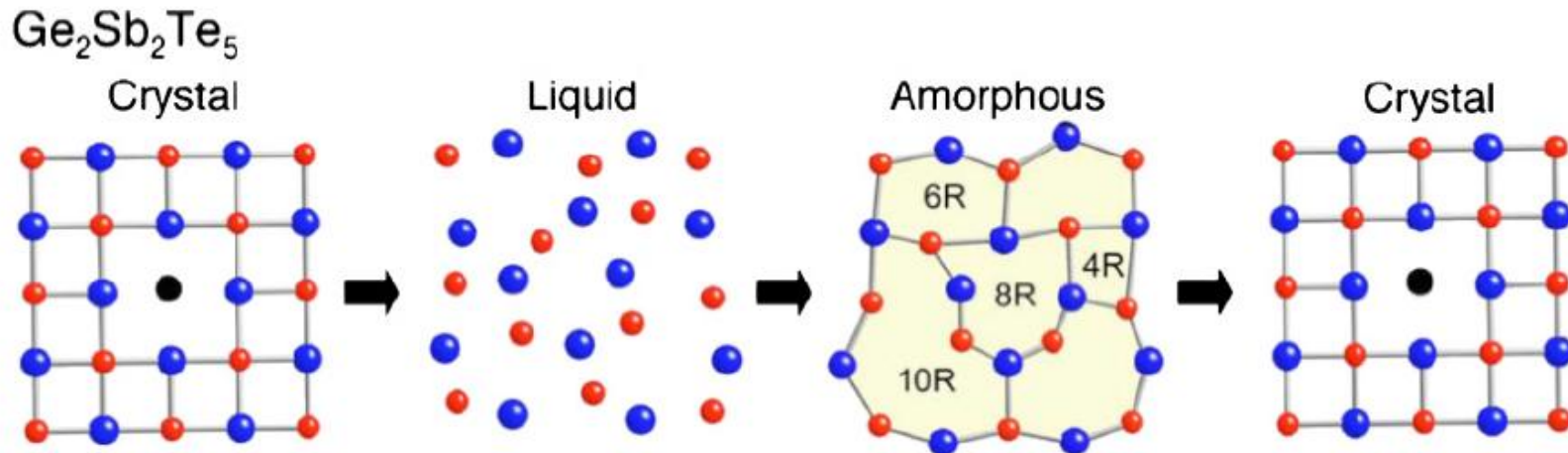
- New storage materials, new storage concepts
- Many ideas, varying functionality/cost, most unproven

# Phase Change Memory Case Study

- Of the emerging RRAMs, PCM is the most mature:
  - Already in low-volume production
  - Demonstrated at Gb density vs. other EM at Mb density
  - Announced by multiple memory companies
- PCM has been heavily studied for 10+ years:
  - Widely published – lots of good-quality technical content
  - Chalcogenide-based material understanding is fairly mature
  - Many active researchers in both industry and academia
- Provides insight into other emerging-materials systems:
  - Many of the RRAMs share similar attributes with PCM

# Why Phase Change Materials Are Interesting

- Amorphous and crystalline phase structures are similar  
→ Easy transition between phase states
- Material contains voids and vacancies  
→ Easy movement of atoms
- Volume of crystalline and amorphous phase closely matched
- Large set of materials to choose from for best performance



# Phase Change Memory Concept

## Storing mechanism:

Amorphous/polycrystal phases of a chalcogenide alloy; example shown is  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  (GST)

## Sensing mechanism:

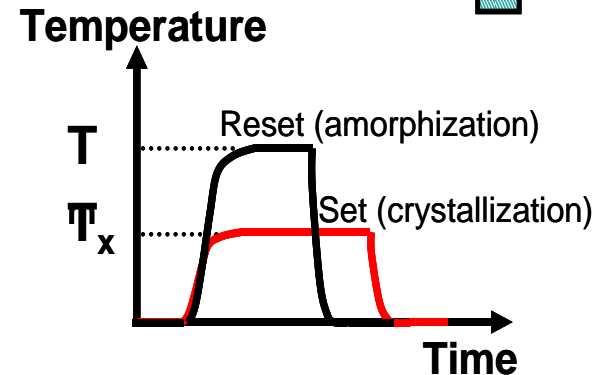
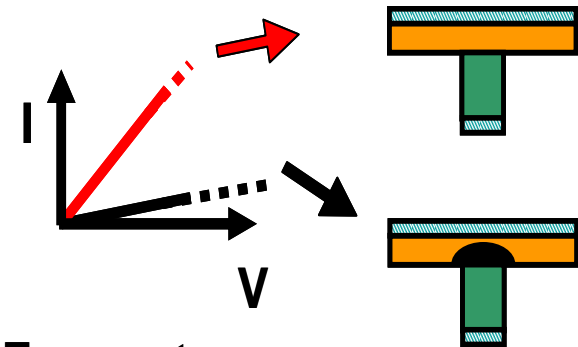
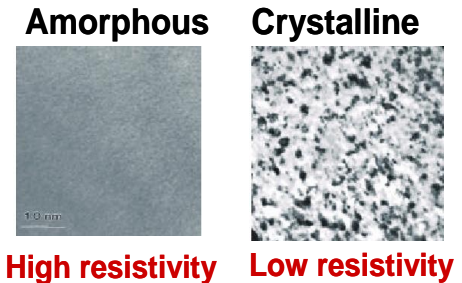
Resistance change of the GST

## Writing mechanism:

Self-heating due to current flow (Joule effect)

## Cell structure:

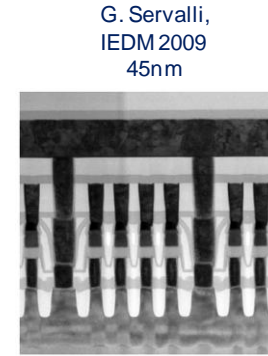
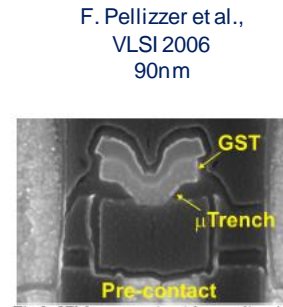
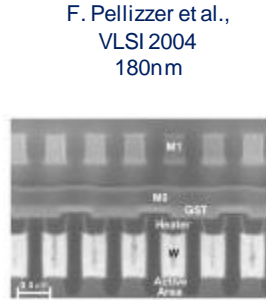
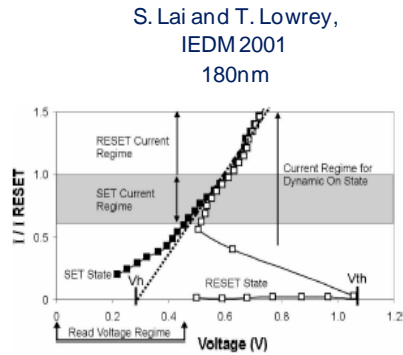
1 diode, 1 resistor (1D/1R)



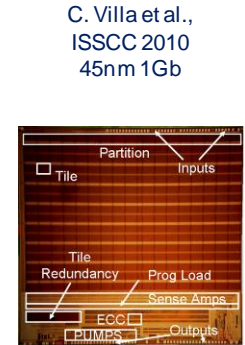
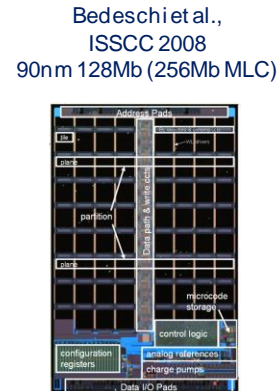
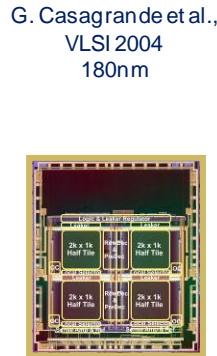
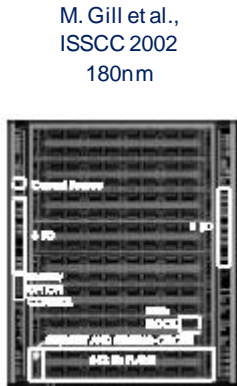


# History of PCM Development

## PCM cell



## PCM array & chip



2001

2003

2005

2007

2009

2011

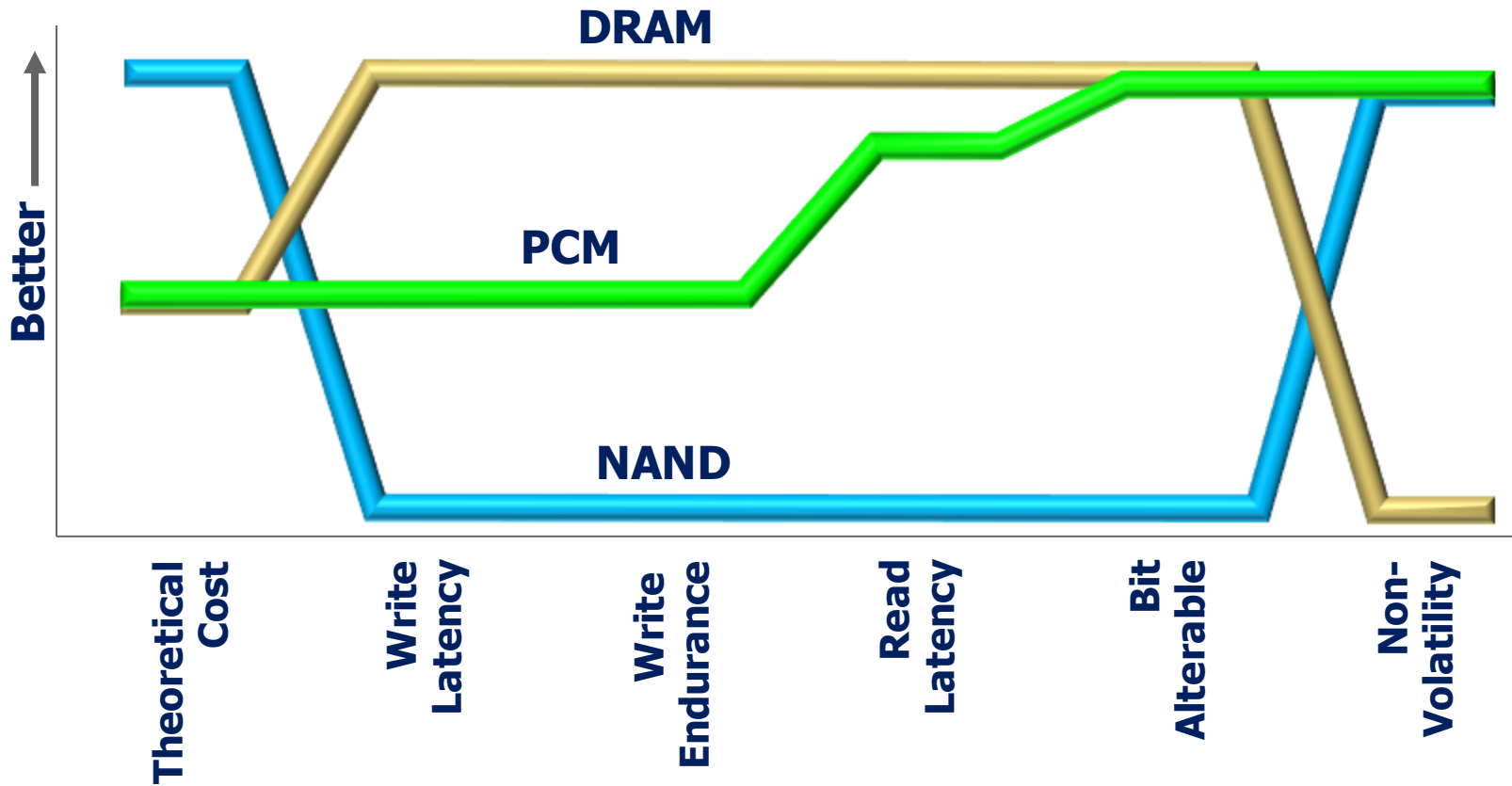
Concept  
Demonstration

Technology Validation  
Product Reliability

Manufacturing

# PCM Characteristics

PCM offers attributes of RAM and NAND  
Roughly aligned to “storage-class memory”



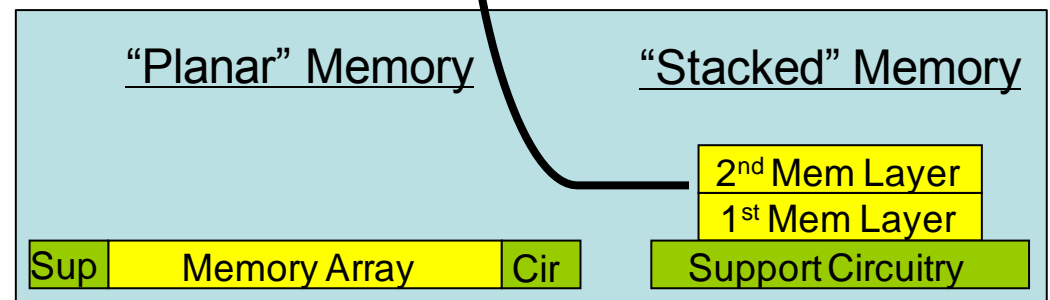
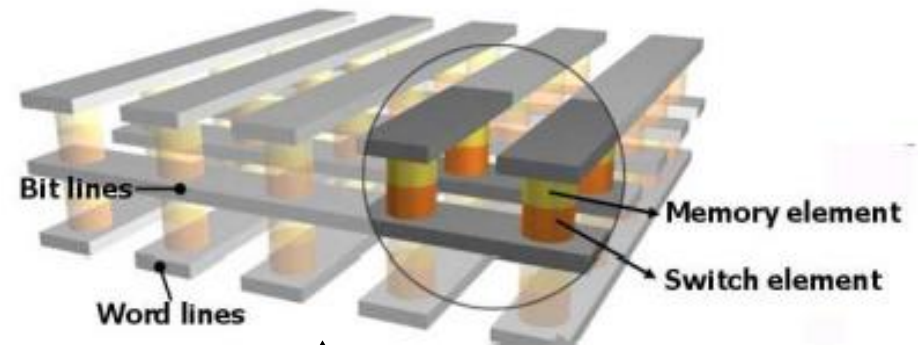
# PCM Applications Opportunities

- **Wireless system** to store XiP, semi-static data
  - PCM bit alterability allows direct-write memory
- **Solid state storage subsystem** to store frequently accessed pages and elements that are easily managed when manipulated in-place
  - PCM caching to improve performance & reliability
- **Computing platforms** taking advantage of nonvolatility to reduce power
  - PCM offers endurance and write latency that are compelling for a number of novel solutions

# 3-D Cross-Point Memory— Best Chance to Reach NAND Cost?

## Cross-point memory *features*:

- Simple small  $4F^2$  cell  
→ low potential cost
- Suitable for 3-D stacking  
→ cell size  $(4/n)F^2$
- Array over circuitry  
→ better array efficiency





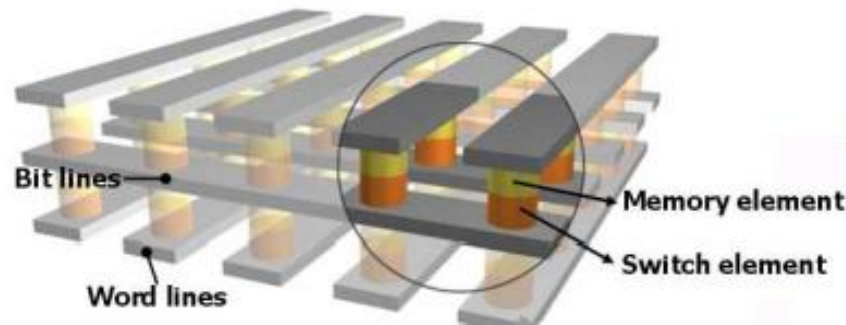
# Wide Range of Cross-Point Options and Combinations

## Selection Device

- Homojunctions → polySi p/n junctions
- Heterojunctions → P-CuO/n-InZnO
- Schottky diode → Ag/n-ZnO
- Chalcogenide ovonic threshold switching (OTS) materials
- Mixed ionic electronic conduction (MIEC) materials

## Memory Device

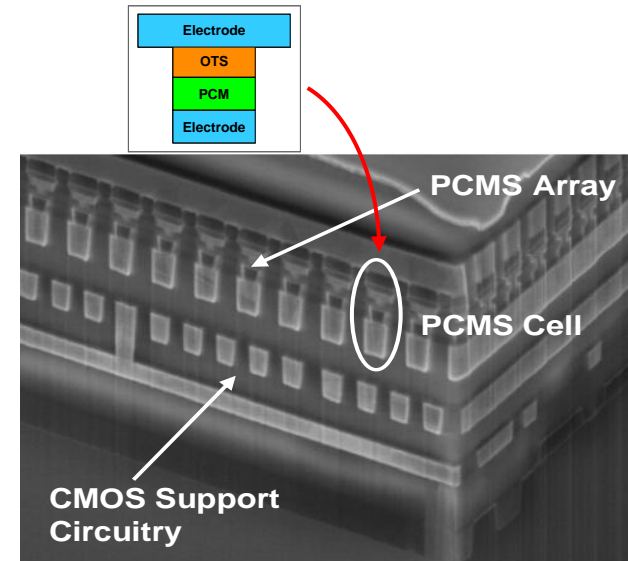
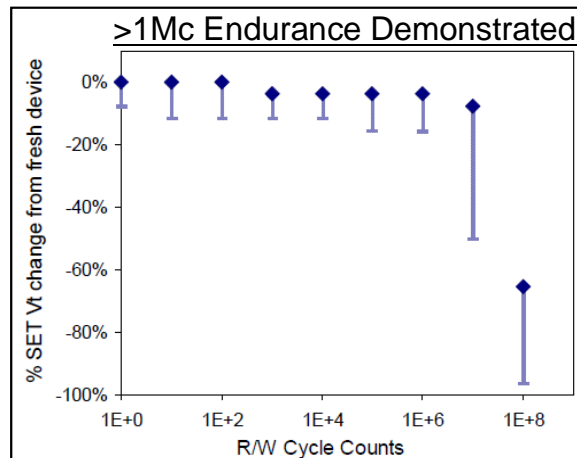
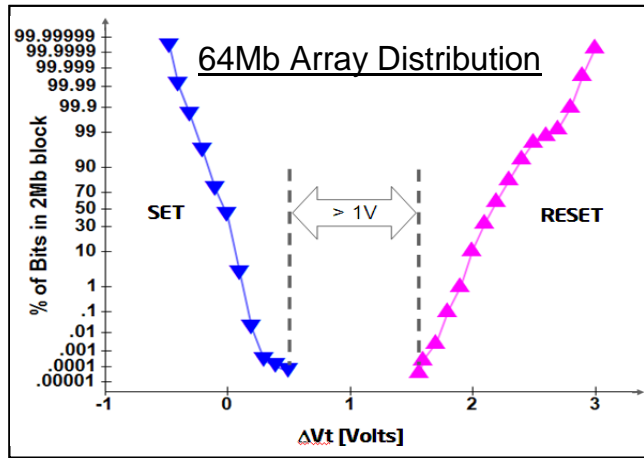
- STTRAM
- RRAM or CBRAM
- PCM



# Phase Change-Based Cross-Point

Stacked phase change memory 64Mb demonstrator:

- Same PCM memory concept
- Ovonic threshold switch – OTS as selection device
- OTS is the same class of materials as PCM but “frozen” in the amorphous phase



3-d corner view of PCMS array

# Summary: A New Era Emerging for Memory!

- Increasing importance of memory to user experience:
  - Our lives are becoming one big shared database
- Increasing importance of memory to system performance:
  - Server performance and power, client portability, and instant-on
- Both NAND and DRAM facing scaling challenges:
  - No hard “wall,” but increasing complexity
  - New storage concepts are emerging for cost and features
- Evolving memory hierarchy around NVM capabilities:
  - Moore’s Law cost treadmill → NVM becoming high-performance storage
  - New memory features → possibility of storage-class memory

**Memory is moving from a support role to a defining system role**

*Revisit Micron’s FMS 2011 presentations at:  
[www.micron.com/fms](http://www.micron.com/fms)*