# High Density, High Reliability Carbon Nanotube NRAM

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Nantero

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# Nantero Overview

- Founded in 2001 to develop nonvolatile memory using carbon nanotubes (CNT) for high density standalone and embedded applications
  - CNT engineering in Boston
  - Circuit design, product, test, device & integration engineering in Sunnyvale
  - Government Business sold to Lockheed Martin in 2008 & successful NRAM test on space shuttle mission
  - Commercial development partnerships with IDMs & fabless companies for embedded and standalone memory applications in progress
- Technology development & IP licensing business model
  - >133 US patents awarded, >205 US applications pending, plus more worldwide
  - WSJ patent score card:
    - The only semiconductor start-up ranked (2009)
    - #2 ranked for scientific strength of IP (2010)
  - IEEE Spectrum; Semiconductor Manufacturing Category
    - #5 worldwide (2009)
    - #2 worldwide and #1 in US (2010)

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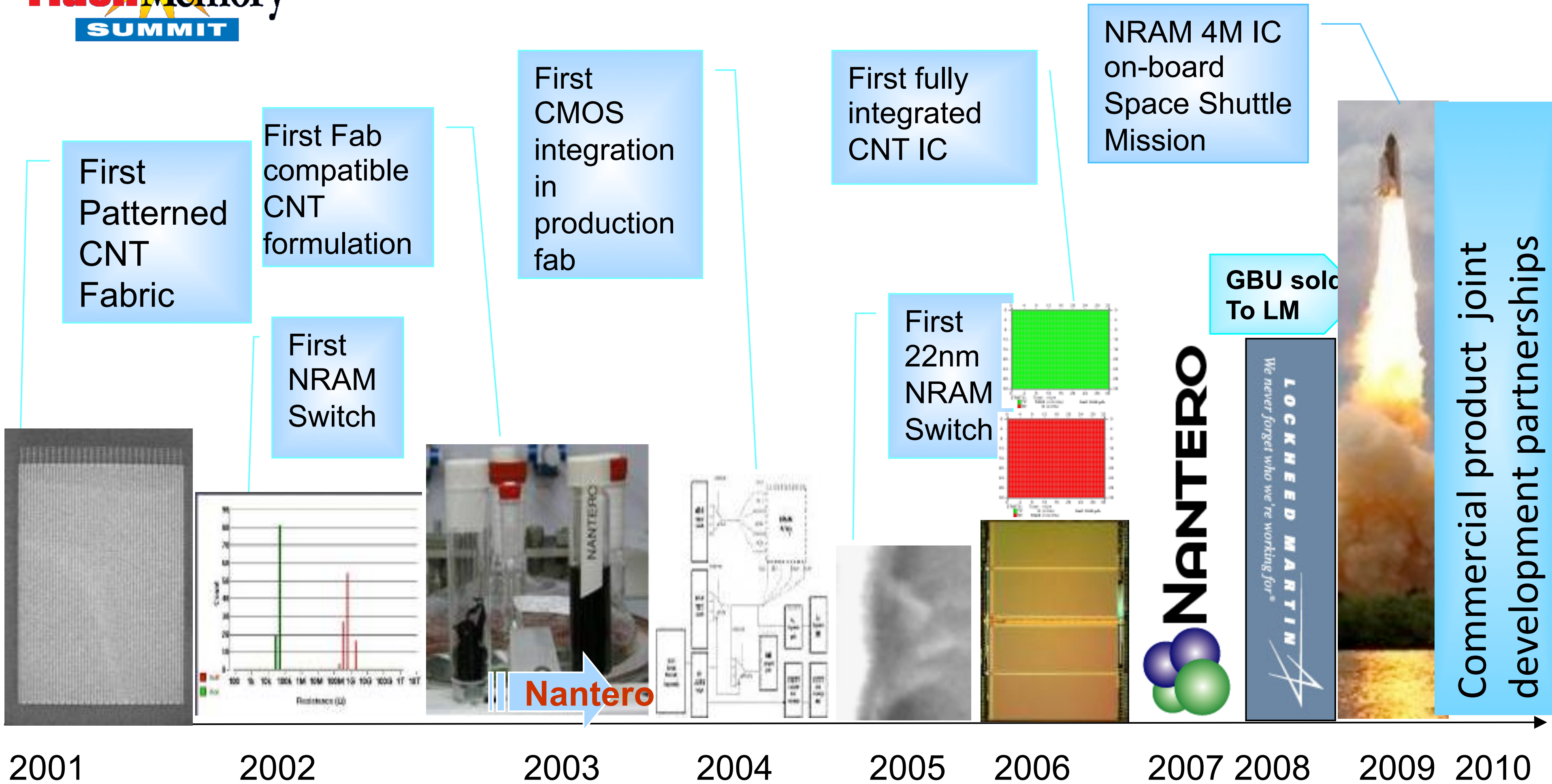
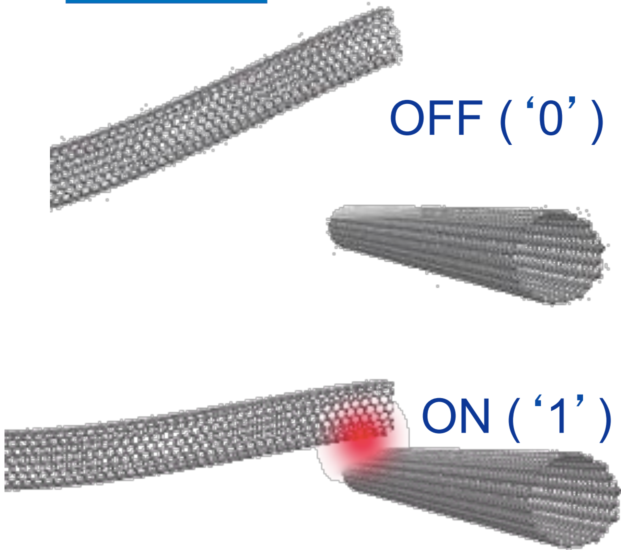
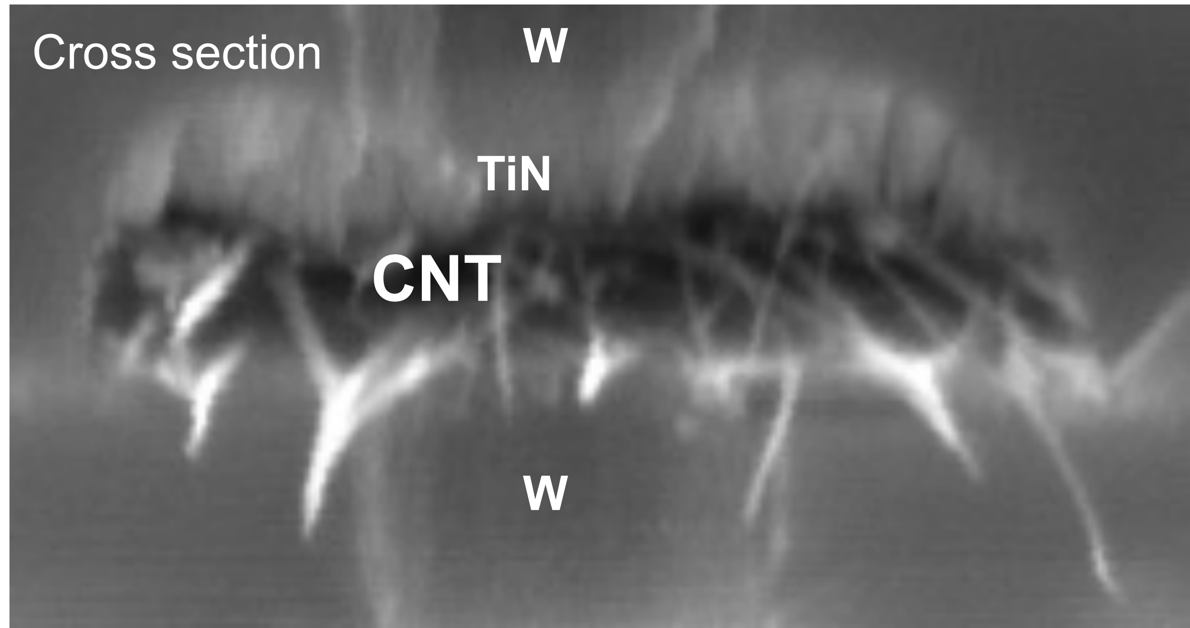
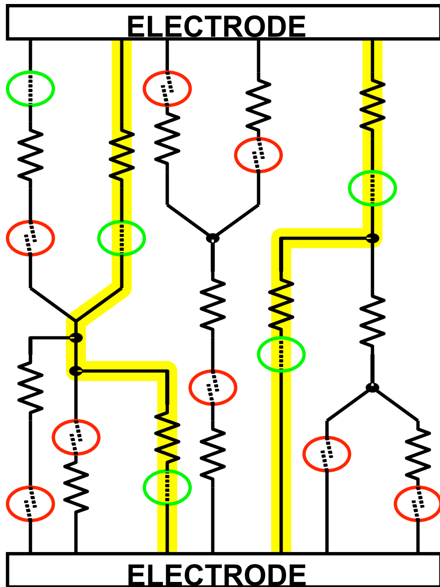
# Nantero Timeline



# NRAM: RRAM with CNT Resistance Change Material




-RESET (ON → OFF): CNT-to-CNT are not in physical contact = high resistance
-SET (OFF → ON): CNT are in physical contact = low resistance

SET is an electrostatic operation while RESET is phonon driven operation (phonon heating of CNT contacts)

# NRAM Mechanism

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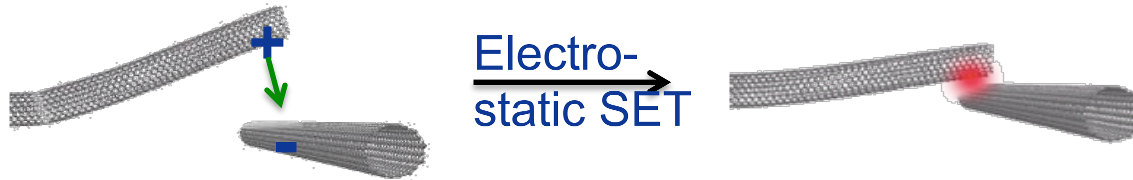
- **SET: electrostatic operation**
  - Write voltage → electrostatic CNT-CNT attraction → CNT junction closure (ON)




  - CNTs remain in ON state due to physical adhesion (Eact ~ 5eV)

- **RESET: phonon driven operation**
  - Voltage applied → CNT phonon excitation → CNT separation (OFF)

  - CNTs remain in OFF state due to high mechanical (1TPa) stiffness (Eact>>5eV)

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# CNT Process Integration

-CNT Spin-on foundry capability at SVTC on 300mm & 200mm coat tracks

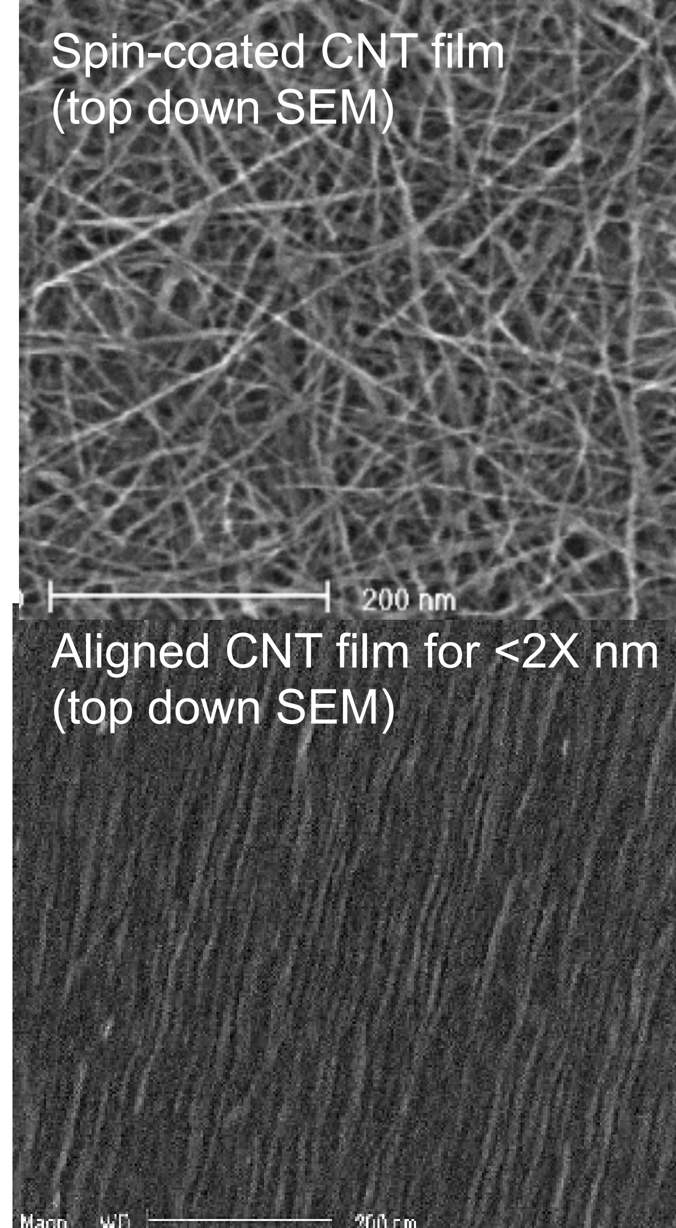
-Tracemetals meets typical BEOL contamination specs (TXRF: <1E11/cm2)

-CNT wafers being processed using 248nm, 193nm dry & *immersion* lithography

-CNT Integration temperatures at standard 425C BEOL and higher if W interconnect only

-Conventional tooling for CNT RIE dry etch and post etch cleaning

-CNT density controllable for different technology nodes

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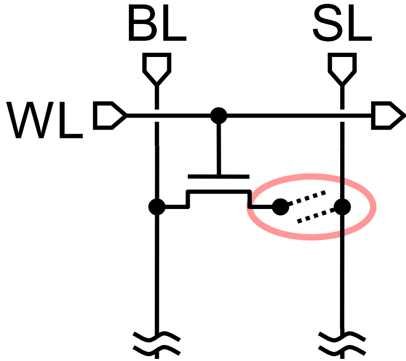
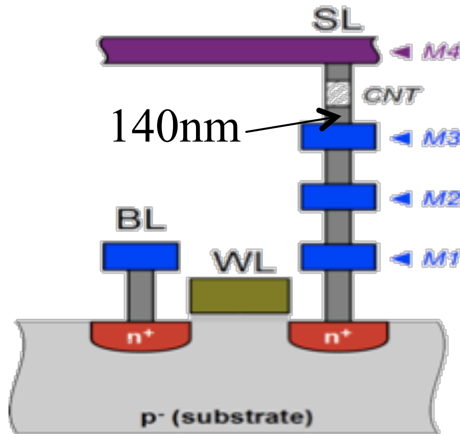
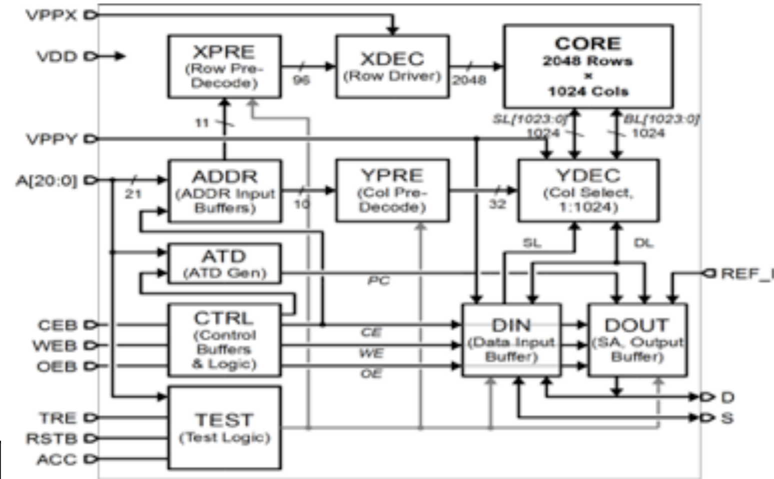
# 4Mb 140nm Carbon Nanotube NRAM



| 140nm 4Mb sample | Write: SET & RESET (-65C to +165C operation) |
|---|---|
| Voltage (CNT) | ~ 3.5 V (scales to 1V with window, CD & pulse speed) |
| Write & read time | < 20 ns (CMOS limited) |
| Current | I (power supply)=1uA/bit |
| Energy | 0.01 fJ / nm2 |
| Window (adjustable) | 100 kohm(ON)/100 Mohm(OFF) |
| Endurance<br>Read disturb | >1E9 cycles (unlimited expected)<br>>1e15 reads (non-destructive) |
| Retention | >10 years at 300C (Eact~5eV) |

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# NRAM Devices at 99.997% Yield

- -93% of the word lines at 100% bit yield (complete 1Mb bank; 512WLs, 2kb each)
- only ~30 bits in 1Mb bank failing (all in 1st cycle)
- No bit fallouts during cycling
- Total bit yield is 99.997%
- Redundancy adequate to repair the device

row number (0-512)

Column number (0-2048)

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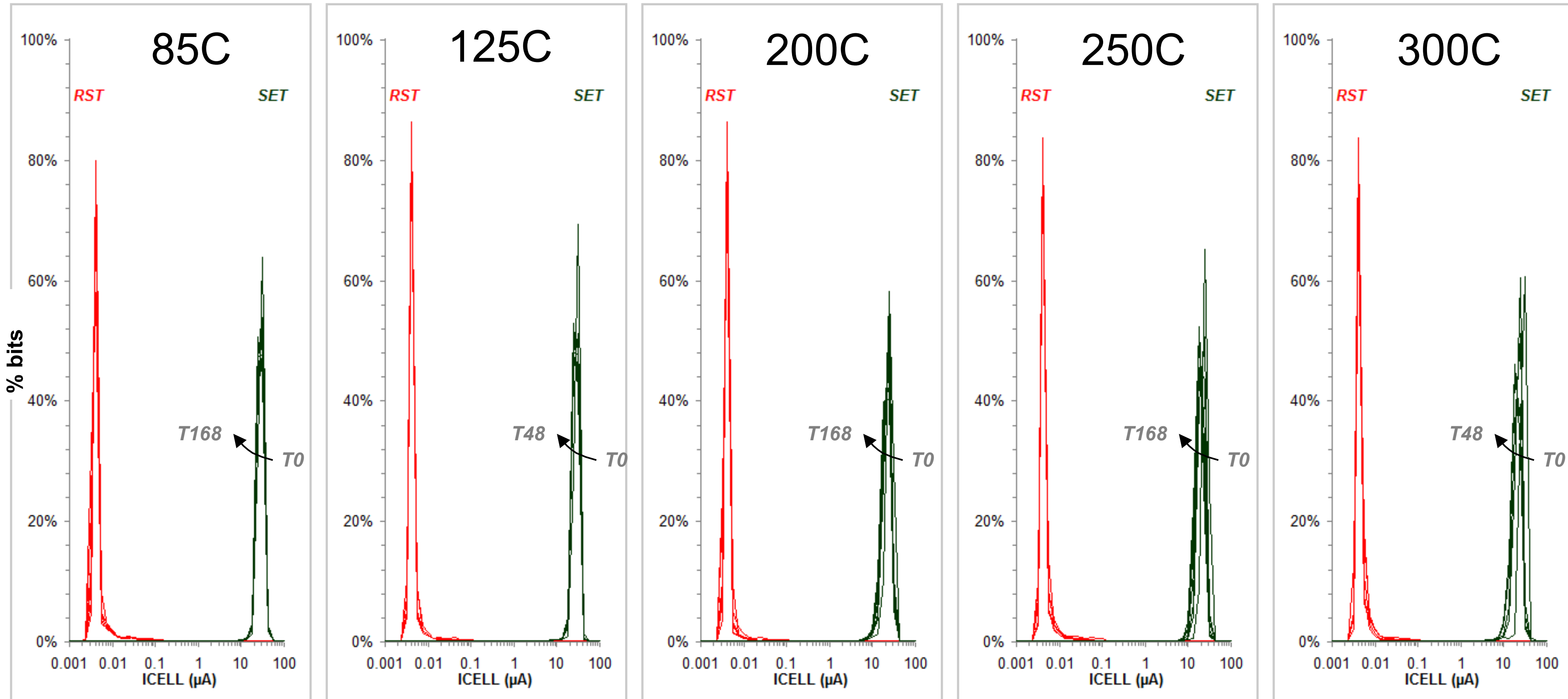
# NRAM Data Retention: >10 Years @ 300C

T0= before bake
T1= after 1 hour bake
T4= after 4 hour bake
T24= after 24 hour bake
T48= after 48 hour bake
T96= after 96 hour bake
T168=after 168 hour bake *

**Data retention: >10years at 300C (3σ)**
**Activation energy: 5.4eV(median), 4.5eV(3σ)**




32kbit / die for each temp

Icell (in µA) at 1volt

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# NRAM Endurance: >1E9 Cycles

Read current at 1V in nA

40k
20k
10k
6k
4k
2k
1k
600
400
200
100
60
40
20
10
6
4
2
1

Stable window through >1B cycles

0 M 100 M 200 M 300 M 400 M 500 M 600 M 700 M 800 M 900 M 1000 M 1100 M 1200 M

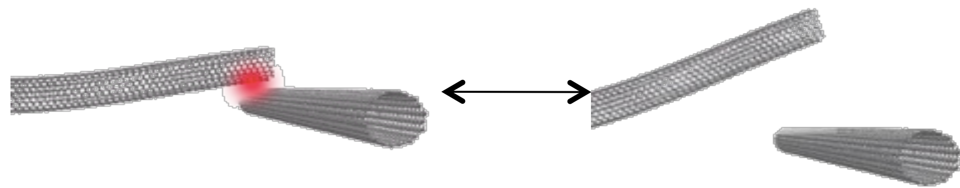
Cycle #

Fixed Voltage & pulse width cycling:

3.5V / 20nsec (SET & RESET)

>1 billion cycles without window degradation

Unlimited endurance expected based on mechanism



# NRAM Technology Summary

- 140nm 4Mb CNT NRAM samples available
- RAM-like <20ns write & read (non-destructive)
- Unlimited endurance expected (1E9 cycles demonstrated)
- Highest reliability of any NVM: >10 years @ 300C (Eact ~5 eV)
- Minimum size select device for 1T1R cell (scalable to 1V/<10uA)
- Low process cost: no HV transistors; 1 BEOL mask for NRAM
- Scalable technology: <5nm CNT-CNT switch; MLC possible
- 300mm and 200mm CNT spin-on foundry capability available
- Transferrable NRAM POR process using only standard BEOL materials (no exotic metals) worked out

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# NRAM Memory Applications

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- NRAM for post-NAND
  - Scalability to <5nm
  - Low write current
  - Dense 1T1R & 1D1R cells
  - MLC capable

- NRAM for post-DRAM
  - Scalability to <5nm
  - High endurance
  - Fast write time
  - Low write current

- NRAM for embedded NVM
  - Low cost
  - Highest reliability
  - Competitive macro size
  - Scalability

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