Designing Scalable, Configurable Controllers for SSDs

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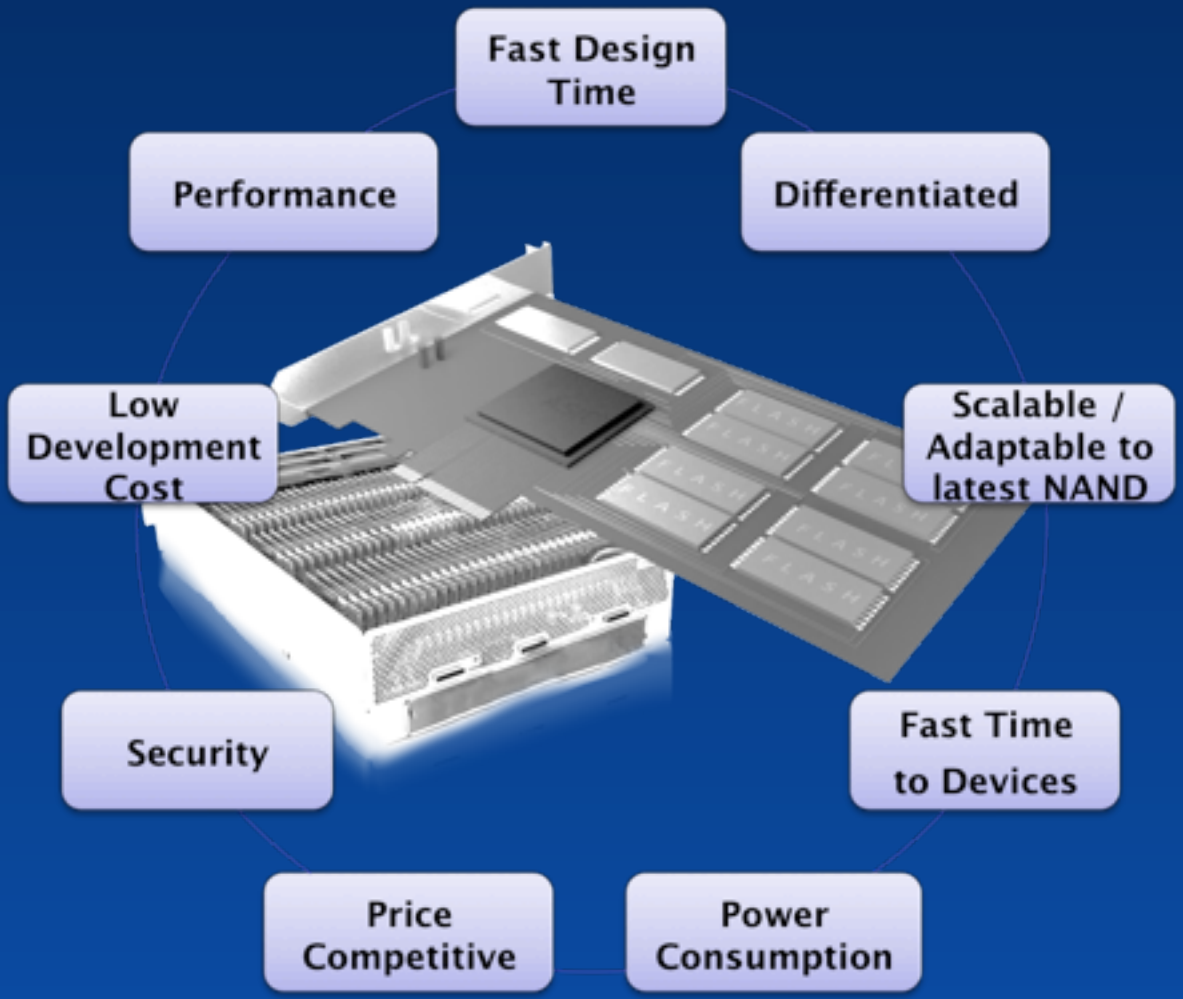
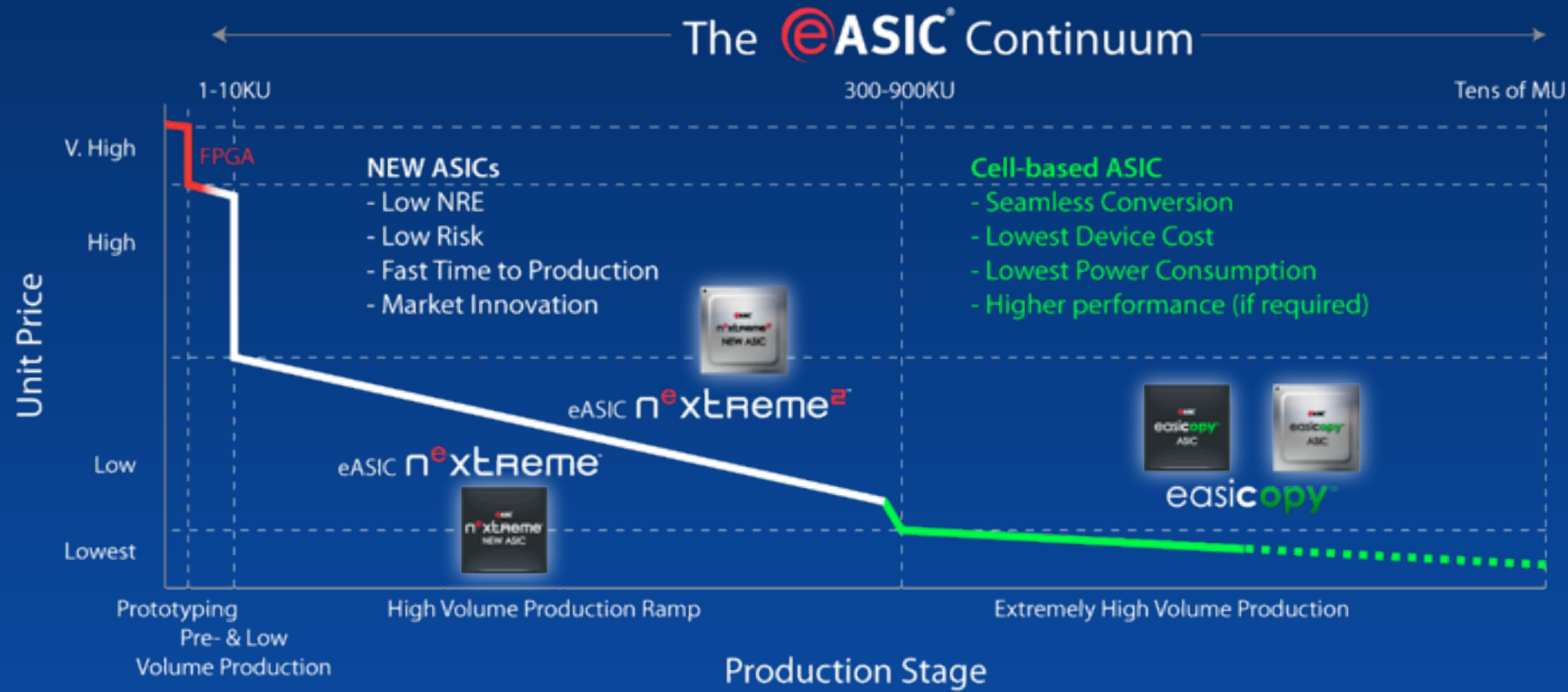
SSD Design Challenges



Traditional SSD Design Options

	FPGA	ASSP	Cell-based ASIC
Low Development Cost	✓	✓	
Fast Design Time	✓	✓	
Scalable/Adaptable	✓		✓
Differentiated	✓		✓
Fast Time to Devices	✓	✓	
Power Consumption		✓	✓
Price Competitiveness		✓	✓
Performance		✓	✓
Security			✓

The eASIC Approach



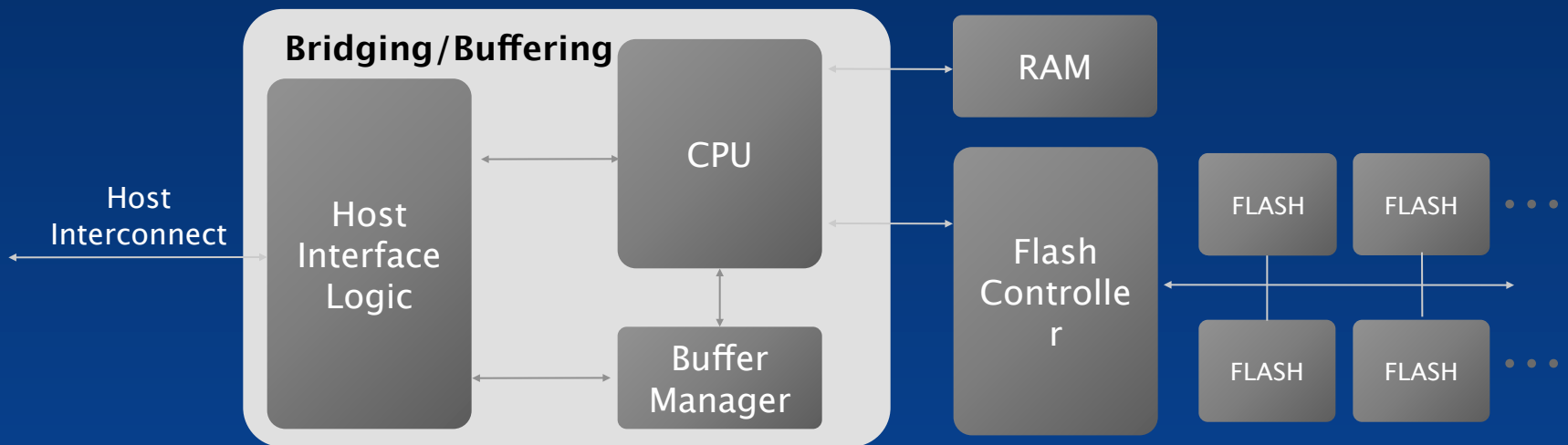
NEW ASIC: A New Design Platform

	eASIC NEW ASICs	Comments
Low Development Cost	✓	A fraction the cost of cell-based ASIC
Fast Design Time	✓	Right by construction design – simpler design
Scalable/Adaptable	✓	Many family members/configurable interfaces
Differentiated	✓	Uniquely configurable using one via-layer
Fast Time to Devices	✓	Only one layer changes from design to design
Power Consumption	✓	50-80% lower power than an FPGA
Price Competitiveness	✓	Shipping in volume in PC hybrid-drives
Performance	✓	Between FPGA and Cell-based ASIC
Security	✓	No external bit-stream or software access

Scalable Design Solutions

	NEW ASIC			Cell-based ASIC
				
Max. Logic Cells	360K	740K	580K	
Max. bRAM (Mb)	5.6	11.5	16.5	Seamless Migration From NEW ASIC To Cell-based ASIC
Max bRAM (#blocks)	175	320	468	
Max I/Os	790	792	630	
Max 6.5Gbps SERDES	–	–	32	

Generic SSD Functional Diagram



- Performance Throughput
- Flexible Interconnects

- Quickly adaptable to support the latest FLASH

eASIC Devices for SSDs

Customized Bridging/Bufferng

- 32-bit CPUs
- PCIe
- SAS
- SATA
- Proprietary Interfaces

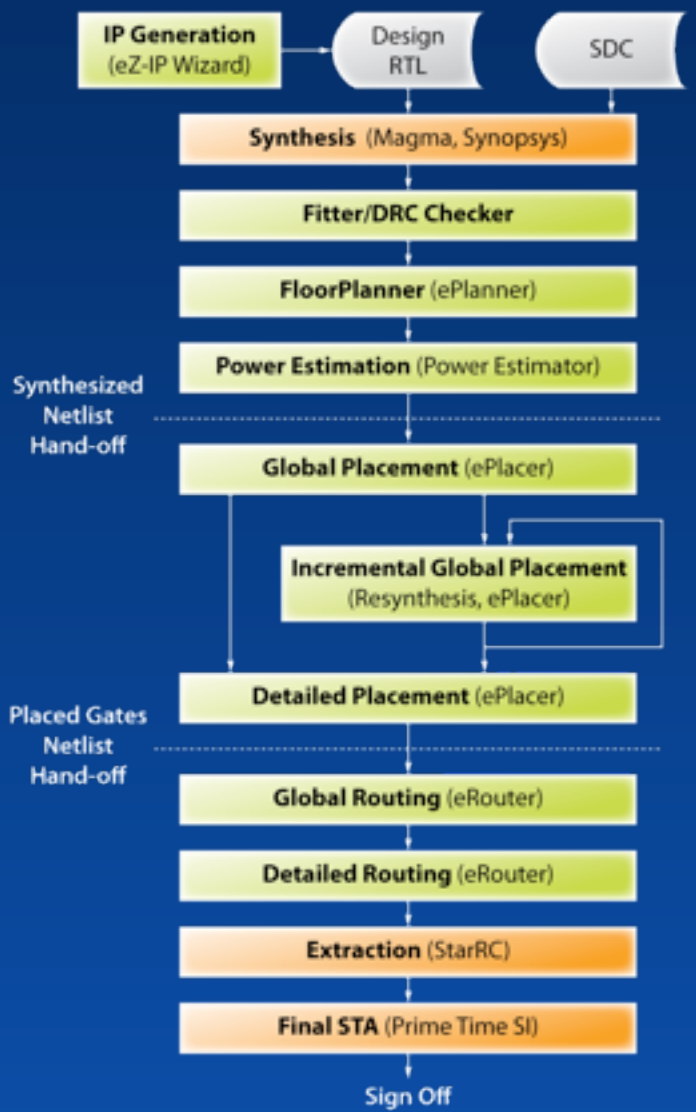
Customized Flash Controller

- ONFI / Toggle
- Proprietary Interfaces

Right by Construction Design

	From FPGA to eASIC NEW ASIC
Design Conversion	eASIC (or customer)
Timing Constraints	eASIC (or customer)
Testbench	Customer
RTL Simulation	Customer
Synthesis	eASIC (or customer)
DFT Insertion	Not Required
Power Mesh Design	Not Required
I/O Ring Design	Not Required
Clock Tree Synthesis	Not Required
Package/Substrate Design	Not Required
IR Drop	Not Required
Placement	eASIC (or customer)
Routing	eASIC
Extraction	eASIC
LVS/DRC	eASIC
STA	eASIC
ATPG	eASIC (only one layer changes)
Formal Verification	eASIC

Design Flow



1. Convert FPGA PLLs, bRAMs, I/Os to eASIC using IP generators within eASIC eTools
   - Synthesize using Magma or Synopsys
   - Floor planning / create optimal region placements
   - Optional power estimation
   - Global and detailed placement using eASIC's ePlacer
2. Routing of vias using eASIC's eRouter
   - Extraction and STA using ASIC grade tools
   - Formal verification after every stage using ASIC grade tool

Summary

- eASIC NEW ASICs enable design of scalable, configurable SSD controllers
  - Lower cost and power than FPGAs
  - Simple to design like FPGAs – Right by construction design
  - Single via-layer configurable for fast design & manufacturing time
  - Enhanced security – No FPGA-like external bit-stream
  - Multiple devices for scalable solutions
  - Already shipping in SSDs