Phase Change Memory Landscape

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Phase Change Memory Values

Attribute	PCM	NOR	NAND	DRAM
Non-Volatile	Yes	Yes	Yes	No
Granularity	Small/Byte	Large	Large	Small/Byte
Erase	No	Yes	Yes	No
Software	Easy	Moderate	Hard	Easy
Power	~Flash	~Flash	~Flash	High (SB)
Write Bandwidth	~100 MB/s	~1 MB/s	~10 MB/s	~1000 MB/s
Read Latency	50 - 100 ns	70-100 ns	15 - 50 us	20 - 80 ns
Endurance	10^{6+}	10^{5}	10^{4-5}	Unlimited

PCM provides an new set of features combining components of NVM with DRAM

Phase Change Memory History

January 1955: Kolomiets/Gorunova - semiconducting properties of chalcogenide glasses
September 1966: Stanford Ovshinsky files first patent on phase change technology
September 1970: 256b PCM memory demonstrated – Gordon Moore
June 1999: Ovonyx joint venture is formed to commercialize PRAM technology
February 2002: Intel demonstrates 4Mb test vehicle
August 2004: Samsung announces successful 64 Mbit PCM array
September 2005: Samsung announces successful 256 Mbit PCM array
July 2006: BAE Systems sells the first commercial PCM, Radiation Hard 512Kx8 chip
September 2006: Samsung announces 512 Mbit PRAM device
October 2006: Intel and STMicroelectronics show a 128 Mbit PCM chip
February 2008: Intel and STMicroelectronics announce four-state MLC PCM
December 2008: Numonyx announces production 128 Mbit PCM device
September 2009: Samsung announces production start of 512 Mbit PCM device
October 2009: Intel and Numonyx announce an all thin film 3-D PCM device
December 2009: Numonyx announces 1 Gb PCM at 45 nm
April 2010: Numonyx releases Omneo PCM Series (P8P and P5Q), both in 90 nm
April 2010: Samsung releases 512Mbit PCM with 65 nm process, in Multi-Chip-Package

PCM Development Activities

Mainstream Development

Scaling the existing architecture, providing the smallest cell size, following the lithography roadmap

Early Evaluations

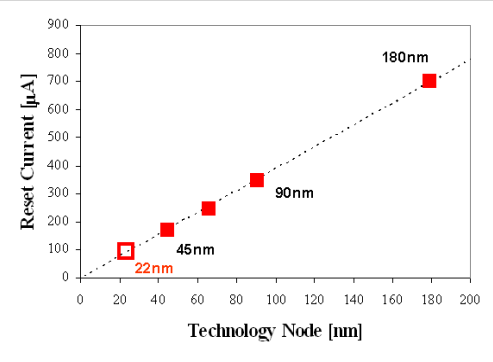
Introduction of Multi-Level-Cell exploiting the analog storage capability of PCM

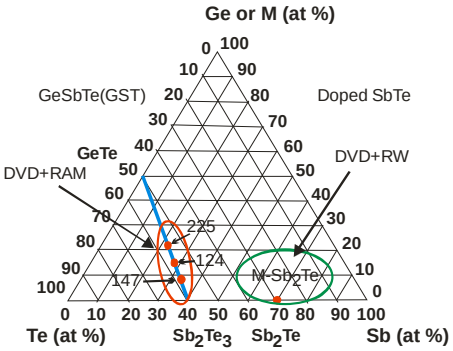
Ongoing Research

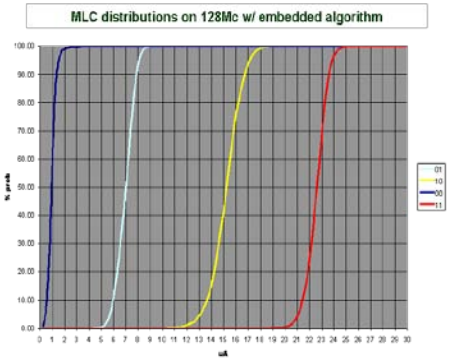
Exploration of new chalcogenide alloys which may open new application fields

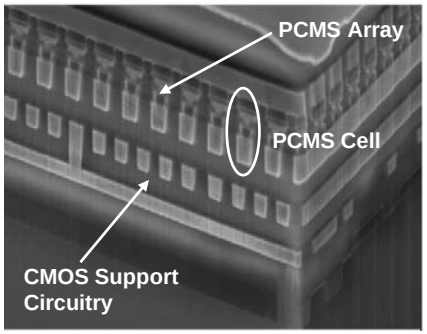
Prof of Concept Research

Exploitation of a true cross-point array which will allow vertical stacking of more than one memory layer









3-d corner view of PCMS array