Session 306: Future of Phase Change Memory

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Agenda

- Current State
- Value Proposition
- Technology Ramp Model
- Adoption Barriers

Phase Change Memory (PCM) Overview

	DRAM	PCM	NAND Flash
Read energy	0.8 J/GB	1 J/GB	1.5 J/GB [28]
Write energy	1.2 J/GB	6 J/GB	17.5 J/GB [28]
Idle power	~100 mW/GB	~1 mW/GB	1–10 mW/GB
Endurance	∞	$10^6 - 10^8$	$10^4 - 10^5$
Page size	64B	64B	4KB
Page read latency	20-50ns	~ 50ns	~ 25 μs
Page write latency	20-50ns	~ 1 μs	~ 500 μs
Write bandwidth	~GB/s per die	50-100 MB/s per die	5-40 MB/s per die
Erase latency	N/A	N/A	~ 2 ms
Density	1×	2 – 4×	4×

Source: Chen, Gibbons, Nath, CIDR '11, Intel, Microsoft

- Reads close to DRAM
- Write latency 10X+ worse
  - But 100X+ better than NAND flash
- 100X+ better endurance
- Low idle power vs. DRAM

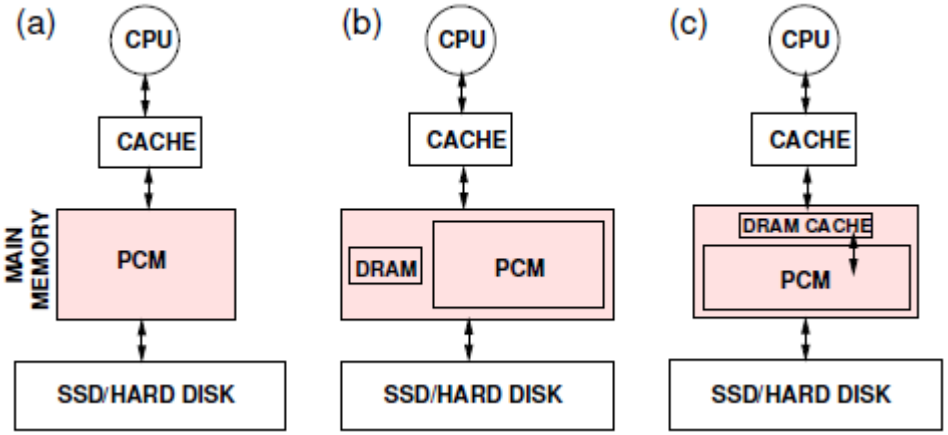
Value Proposition

- Lower Idle Power: for mobile
- Hybrid Enterprise Flash Cache Controller
- System Memory Hierarchy
- Flash Cache Endurance for Enterprise:
  - Better endurance for high IOPS environments
  - MLC NAND endurance getting worse in new process geometries

Hybrid Enterprise Flash Cache Controller
PCM and NAND

- PCM for Metadata/logs
  - Block table
  - Partial writes
  - Garbage collection
  - Hot data tagging
- PCM for RAID parity
  - Fast
  - Less ECC
  - Better endurance
- PCM write thru cache

System Memory Hierarchy



Source: Chen, Gibbons, Nath, CIDR '11, Intel, Microsoft

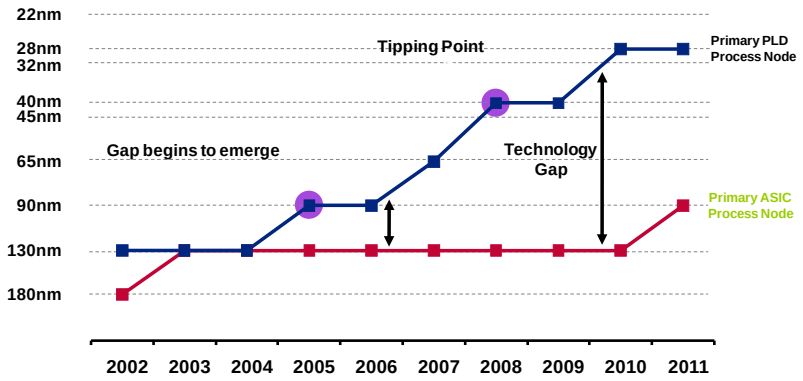
- O/S is DRAM aware: (b)
  - Also "storage class memory"
  - Application written to take advantage of it
- DRAM cache hidden: (c)

Technology Ramp

- Today: mobile
- Shorter term:
  - Customer prototyping within a year
  - Hybrid enterprise flash cache controllers
  - High transaction rate enterprise flash cache
- Longer term:
  - General enterprise flash cache replacement
  - Applications which are DRAM and PCM aware

Adoption Barriers

- Fast innovation
  - Hybrid controller algorithms
    - What is hot, what goes where
    - Partial writes, write thru, …
- Uncertain forecast
- Need fast TTM
- Differentiation
  - Dedupe, hybrid algorithms, etc.
- High ASIC dev. costs
  - Increasing technology gap
    - vs. FPGA
  - 8G SerDes PHY
    - Usually on 40 nm
    - PCIe Gen3, 12G SAS



PLDs Outstripping Traditional ASICs in Technology and Total Cost of Ownership

Thank You