Total Solution for Designing Mobile Storage Systems

Yuping Chung

Product Marketing Manager

Arasan Chip Systems
San Jose, CA 95131

Agenda

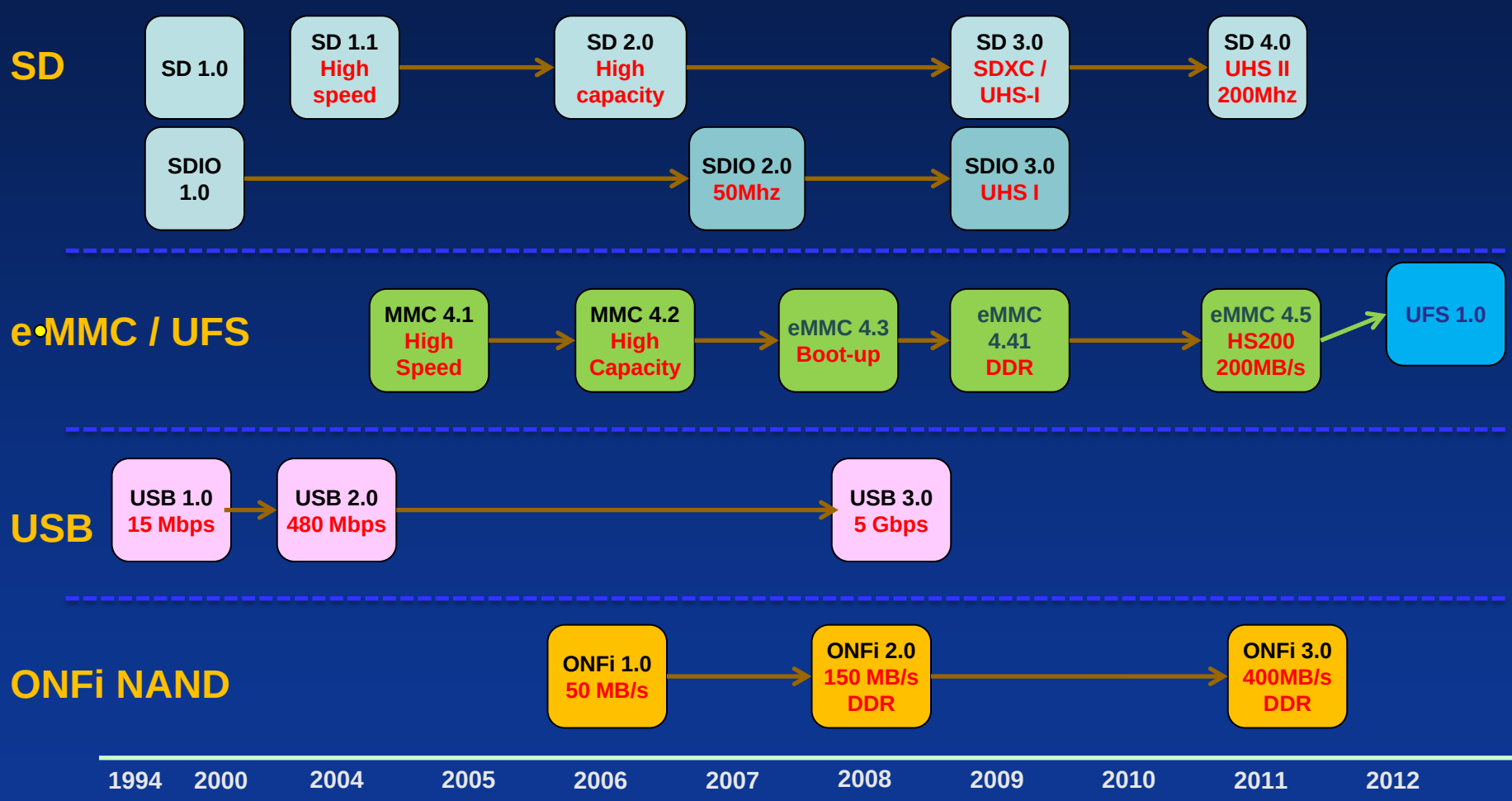
- Mobile Storage Interfaces
- Challenges to Mobile Storage System Designs
- Total IP Solution Approach

Typical Mobile Storage Devices

- Mobile Devices
  - Smartphone, Tablet, eReader, Digital Camcorder, Camera, etc

- Mobile Storages
  - Embedded Storage
    - NAND flash
    - e•MMC Managed NAND storage
  - External Storage
    - Micro SD cards
    - USB thumb drives, USB HDD
    - Other removable memory cards

Typical Mobile Devices Support Major Mobile Storage Interfaces



Challenges of Designing Mobile Storage Systems

1. Complexity of Integration

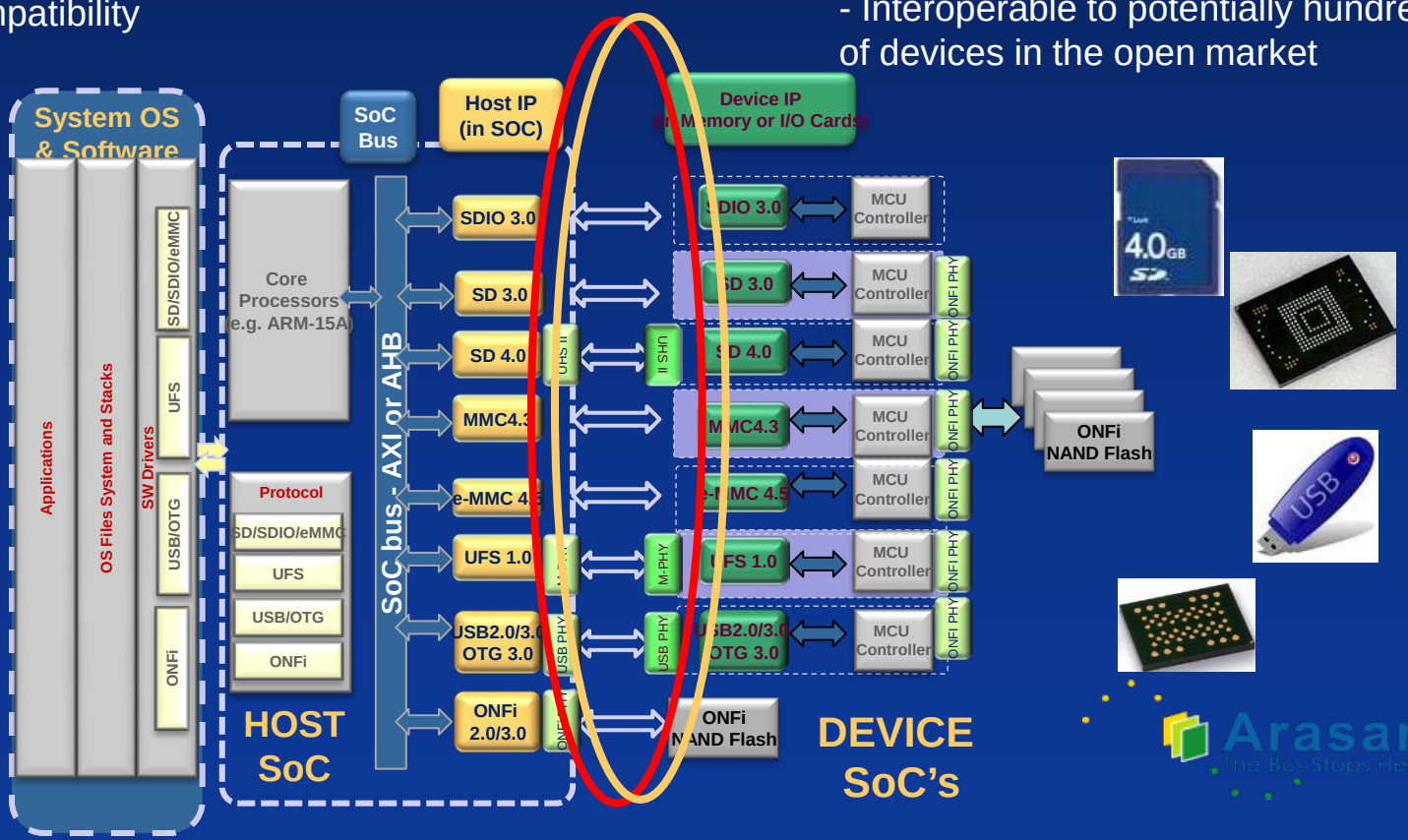
a) Physical Layer Analog Interface
b) Controller Digital Design
c) Controller Firmware and OS Software Drivers
d) OS File Systems & Stacks

2. Compliant to Multiple Standards

- Backward Compatibility

3. Compatibility

- Interoperable to potentially hundreds of devices in the open market



Santa Clara, CA
August 2011

SD 4.0 / e•MMC 4.5 Design Considerations

SD 4.0

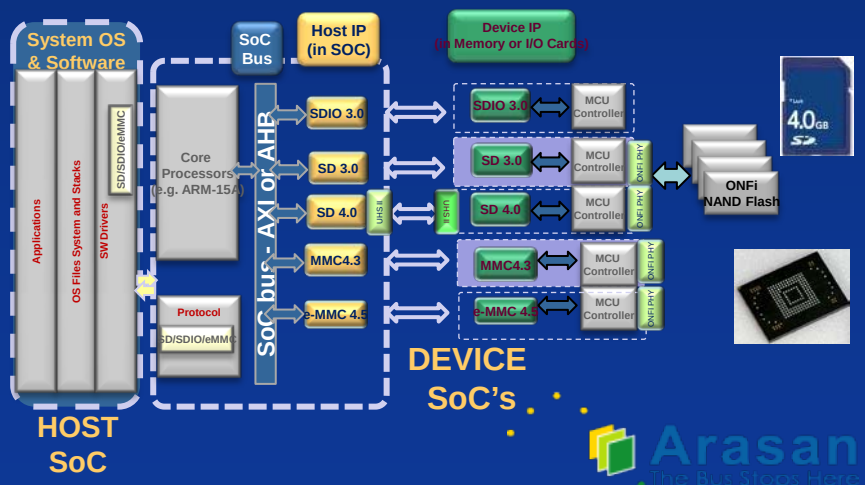
- backward compatible to SD 3.0/2.0/1.0
- Faster UHS-II PHY 1.56 Gbps/lane at 52MHz
- Additional pins for differential signaling
  - D0 +/- and D1 +/-

e MMC 4.5

- Published in June 2011 for embedded only
- Adds 200Mhz mode for max 200MB/s @ 8-bit data bus
- 4 KB access
- Removed secure erase and secure trim
- Adds Discard & Sanitize command
- *e*2•MMC - optional cache command and two optional internal voltage nodes

Challenges:

- Backward Compatible to
  - SD 3.0, SD 2.0, SD 1.0
  - e•MMC 4.4, 4.3, 4.2, 4.1
- New SD UHS-II PHY & Additional SD Differential Signals
- Interoperability

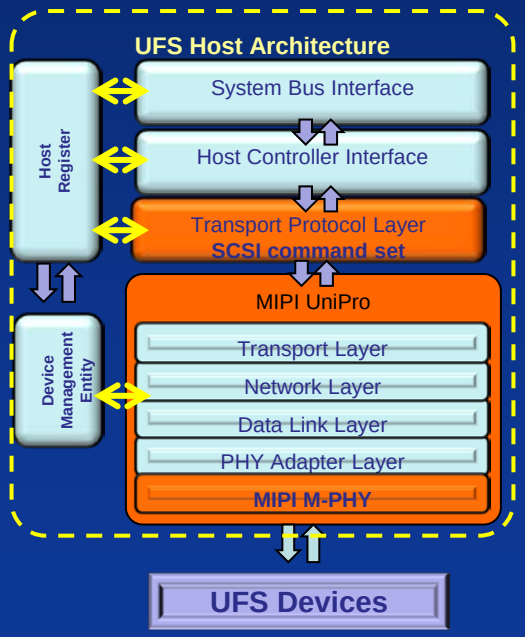


UFS 1.0
Design Considerations

- Universal Flash Storage is originally part of Mobile Industry Processor Interface (MIPI) Alliance
- Performance - 5.8 Gbps max per lane
  - Gear 1 - 1.25 Gbps
  - Gear 2 - ~3 Gbps optional
- Physical Layer adopts MIPI's M-PHY
- Link Layer adopts MIPI's UniPro
- Protocol layer adopts SCSI, but with own command set

Challenges:

- New standards adopting **MIPI M-PHY** and **MIPI UniPro**
- High speed M-PHY 5.8Gbps
- New Compliance and evolving Interoperability ecosystem

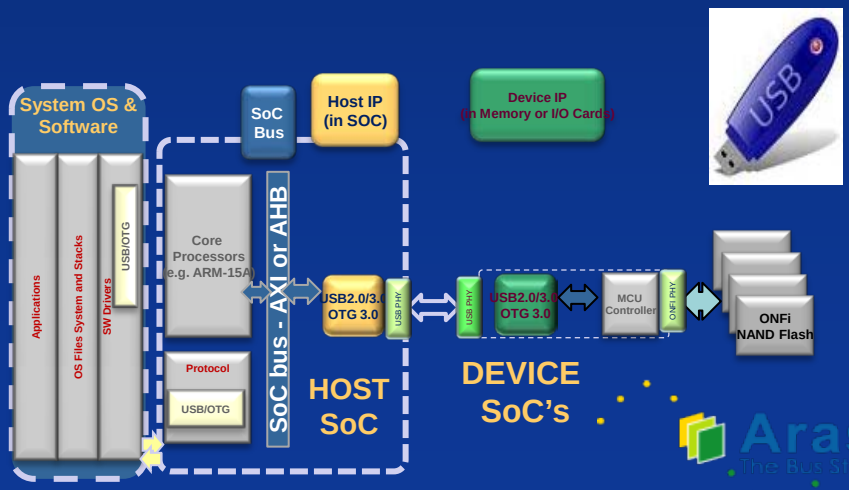


USB 3.0
Design Considerations

- USB SuperSpeed @ 6Gbps
- Dual bus architecture
  - Concurrently operating SuperSpeed and Full Speed bus
- Dual simplex signaling
  - 2 differential pairs
- Four link states for power management
  - U0 - Operation, U1 - idle/fast exit, U2 - idle/slow exit, U3 - suspend
- Multiple command on a pipe and out of order completion

Challenges:

- Integrating high speed 6Gbps PHY
- Update Firmware and Driver for power management
- Backward compatibility
- Compliance and Interoperability



ONFi 3.0
Design Consideration

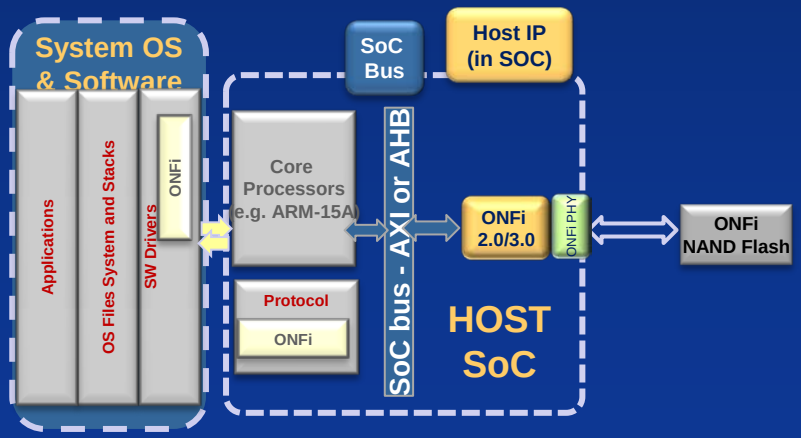
ONFi 3.0 NAND Specification

- Published in March 2011
- Backwards compatible with ONFi 2.0
- Up to 400 MB/s

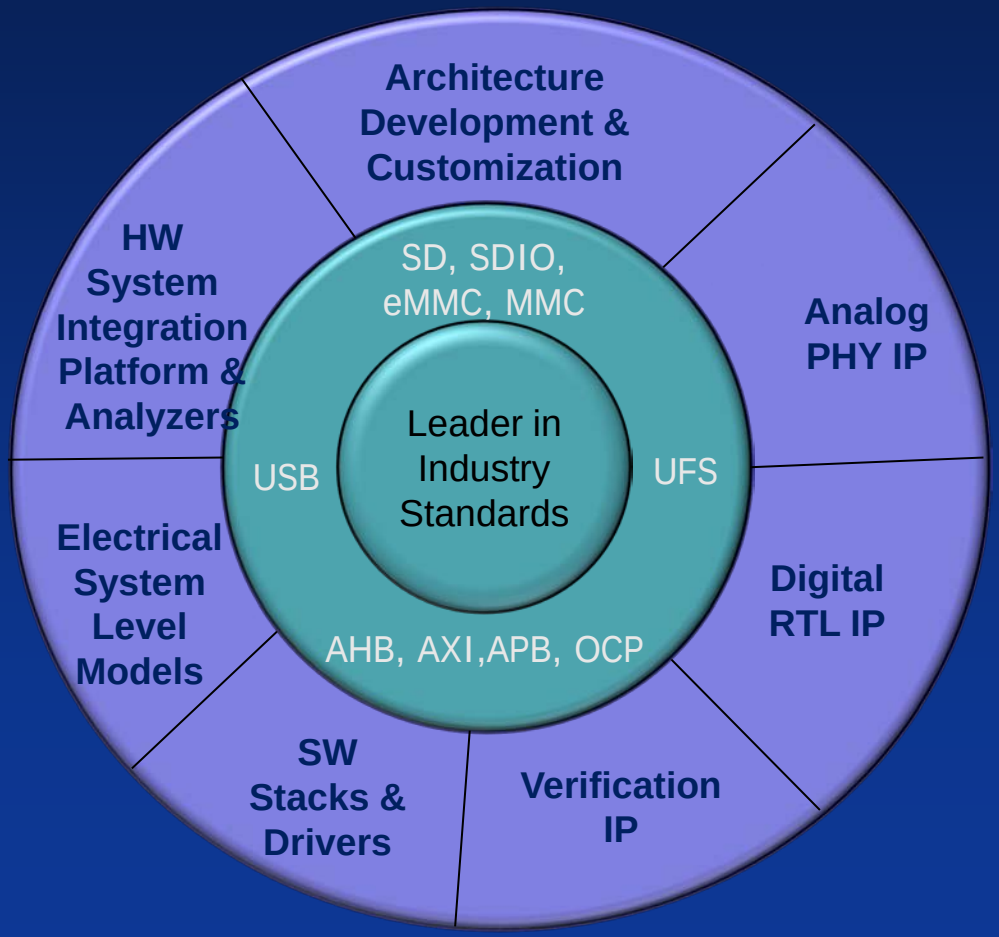
- Differential signaling on clock and data lines
- DDR-2 Transfers
  - True and Complement Data Strobes
  - SDR, NV-DDR and NV-DDR2
- Single and Dual data bus discovery
- Page sizes up to 8K
- ECC up to 64 bits
  - Dynamically configurable ECC width

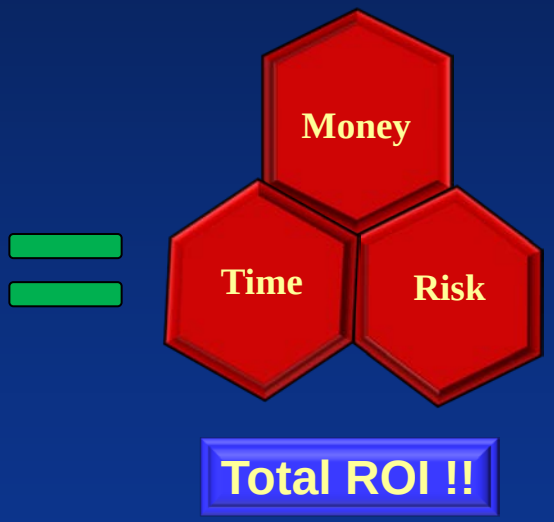
Challenges:

- Backward compatibility
- Compliance and Interoperability



Total IP Solution Satisfying Total Compliance and Compatibility





Santa Clara, CA
August 2011

Thank You !

- **Yuping Chung**

- **Product Marketing Manager**
- **yuping.chung@arasan.com**

- **Arasan Chip Systems**
- **San Jose, CA 95131**