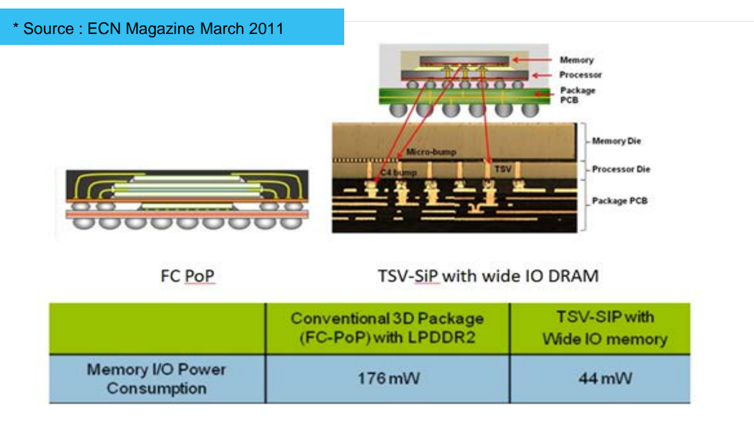
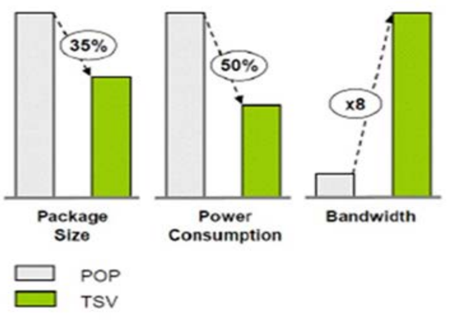
3D-IC is Now Real: Wide-IO is Driving 3D-IC TSV

Samta Bansal, Cadence
Flash Memory Summit
August, 2012

What the fuss is all about …



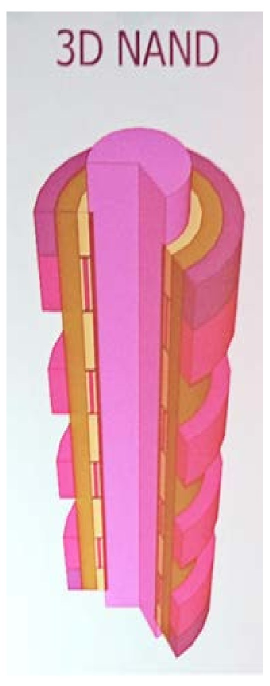
	Conventional 3D Package (FC-PoP) with LPDDR2	TSV-SIP with Wide IO memory
Memory I/O Power Consumption	176 mW	44 mW



Comparison of package performance: wire-bonding PoP vs wide IO interface with TSV (Courtesy of Samsung)

TSV connections
DRAM Layer
Logic Layer
Package Substrate

* Source : Tech Spot Feb 2011 & Flash Memory Summit August 2011



Samsung Wide-IO Memory for Mobile Products - A Deeper Look

Micron develops "Hyper Memory Cube" 3DIC technology

Faster, Denser, Low-power Chips Using 3D-IC TSVs

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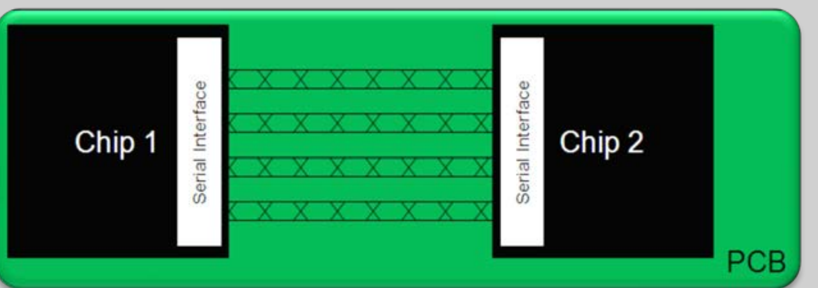
CPU to DRAM

Existing inter-die connection methods



Parallel Connection across a PCB

- Most common CPU/SoC-to-DRAM connection today
- Well understood and extensible
- Many pins required for high bandwidth
  - ~60 signal pins for a 32-bit LPDDR2 interface (2012 low-mid range smartphone)
  - ~120 signal pins for a 2-channel LPDDR2 interface (2012 mid-high end smartphone)
  - ~300 signal pins for a 3-channel 64-bit DDR3 interface (2012 PC)

Serial Connection Across a PCB

- Fewer pins than parallel connection
- Common for PCIe and other SerDes-based standards
- Can provide data transfer over longer physical distances if needed
- Potential latency and power considerations
- Not commonly used for DRAM at present; future solution?

Pin Count, Power, Latency Concerns?

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New inter-die connection method - TSV

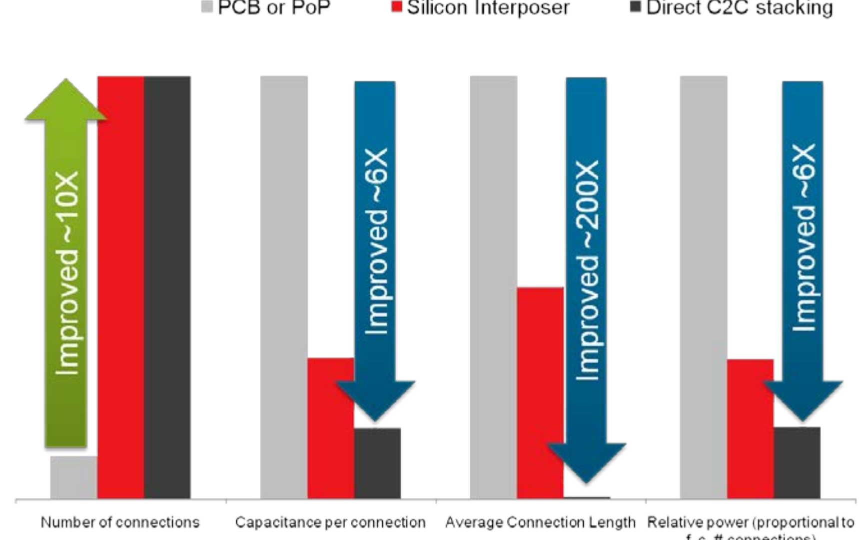
Topside and backside metal layers
Device layer
SiP substrate
Chip substrate
Circuit board

Through-silicon vias (TSVs)
Die #1
Die #2
Micro-bumps (diameter~10um pitch~10um)
Flip-chip bumps (diameter~100um pitch~100um)
Silicon interposer
Package bumps

Silicon Interposer Method

Die #2
Die #1
Micro-bumps (diameter~10um pitch~10um)
Flip-chip bumps (diameter~100um pitch~100um)
Package bumps

Direct Chip-to-Chip Stacking



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What is Wide-IO DRAM?

Bandwidth

Possible Future Standard
- 2Tbit/s bandwidth

Possible Future Standard
- 4 128-bit channels
- Total 512bits to DRAM
- 1066MHz DDR (2133MT/s)
- 1Tbit/s bandwidth

Possible Future Standard
- 4-8 64-128-bit channels
- 256-512bits to DRAM
- DDR Interface
- 200-400Gbit/s bandwidth

Current Standard
- 4 128-bit channels
- Total 512bits to DRAM
- 200MHz SDR
- 100Gbit/s bandwidth

Possible time of introduction

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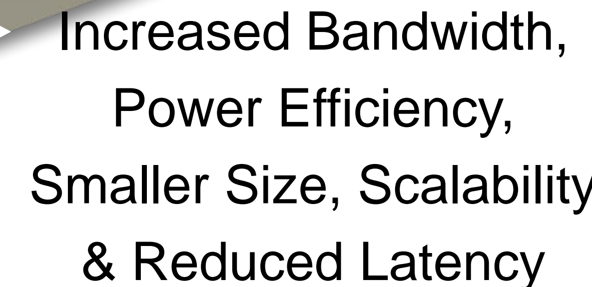
What is HMC Architecture?

Abstracted Memory Management	Through-Silicon Via (TSV) Assembly
Memory Vaults Versus DRAM Arrays	Innovative Design & Process Flow
Logic Base Controller	Advanced Package Assembly



- Increased Bandwidth, Power Efficiency, Smaller Size, Scalability & Reduced Latency

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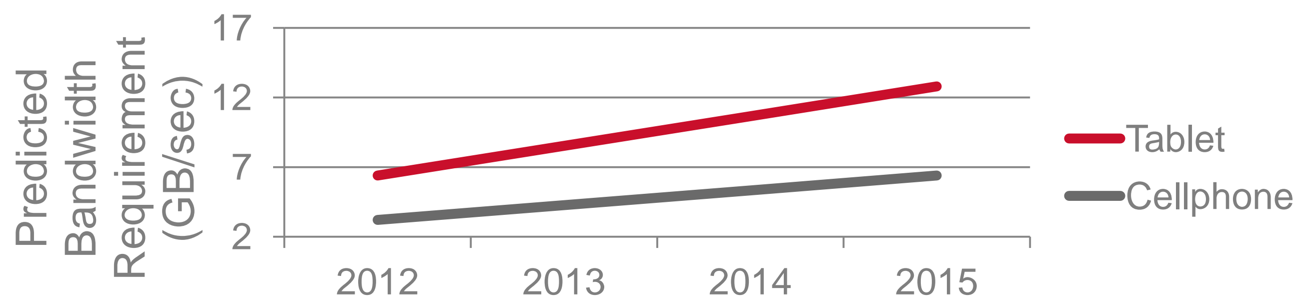
Why do you need Wide-IO DRAM?



Solutions	LPDDR2 533 MHz		LPDDR3 800 MHz		WideIO 200 MHz	
	Single Channel	Dual Channel	Single Channel	Dual Channel	Single die + LPDDR2	Cube
Density (2014)	2x 4 Gb	4 x 4 Gb	2 x 8 Gb	4 x 8 Gb	2 x 8 Gb	4 x 8 Gb
Bandwidth	4.25 GBy/s	8.5 GBy/s	6.4 GBy/s	12.8 GBy/s	17.1 GBy/s	12.8 GBy/s
Power (burst read)	330 mW	660 mW	430 mW	860 mW	730 mW	540 mW
Power / Bandwidth	78 mW/GByps		67 mW/GByps		43 mW/GByps	42 mW/GByps
Cost (2014)	N/R	1	N/R	1.1	1.2	1.4

→ WideIO provides 2x power efficiency compared to LPDDR2/3

- The initial JEDEC proposal is providing 12.8GBytess bandwidth. Increasing DRAM frequency to 266MHz and implementing dual data rate transfers will provide eventually more than 34GBytes/s.

RTI Conference – 13th Dec 2011
A Three-Layers 3D-IC Stack including WideIO and 3D NoC
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Why Wide-IO is driving TSV

DRAM is the ideal candidate to drive TSV technology

- Usually manufactured on a non-logic process
- Requires high bandwidth connection between CPU and DRAM
- Uneconomic or impossible to place large capacity (Gbits) of DRAM on same die as CPU
- Low power connection between dies desirable
- Possibility of different memory configurations using the same CPU die

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Cadence Wide-IO DRAM controller

Challenges	Solutions
Merge existing and new technology	• Start with extensible, high performance, low-power base architecture (Supports DDR1, DDR2, DDR3, LPDDR1, LPDDR2 and now DDR4) • Re-add SDR support • Add new Wide IO feature support • Create DFI extensions for Controller-PHY connection
New testing requirements	• Extend BIST engine to test for new classes of error
Verification	• Create memory model of Wide-IO device in Cadence VIP tools • Extend existing configurable verification environment for Wide IO

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Real chip, real examples

Wioming test chip program

Same SoC addressing several schemes of 3D integration

Wioming

High speed CMOS techno
70mm²
2000 TSVs
1000 bumps
500 balls

	Proof of concept for:		
	Technology	Architecture	Design Flow
Wide IO demonstrator: DRAM on Wioming	❑ Die to Die ❑ Face to Back ❑ TSV middle ❑ Cu Pillar bumps and micro-bumps	❑ Wide memory data bus (512-bit) ❑ High bandwidth (>10GBps) memory interface ❑ Multi-channel memory controller ❑ Test for 3D Memory interconnect	❑ 3D floorplanning ❑ 3D routing (signal & power) ❑ 3D Test ❑ Verification ❑ Power analysis ❑ Thermal analysis
3D NoC demonstrator: Wioming on Wioming	❑ Die to Die ❑ Face to Back ❑ TSV middle ❑ Cu Pillar bumps and micro-bumps	❑ 3D NoC router ❑ 3D serial link ❑ Test for 3D NoC interconnect ❑ TSV Fault Tolerance scheme	
3 Layer demonstrator: DRAM on Wioming on Wioming	Combination of all above techniques		

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A Three-Layers 3D-IC Stack including WideIO and 3D NoC 8

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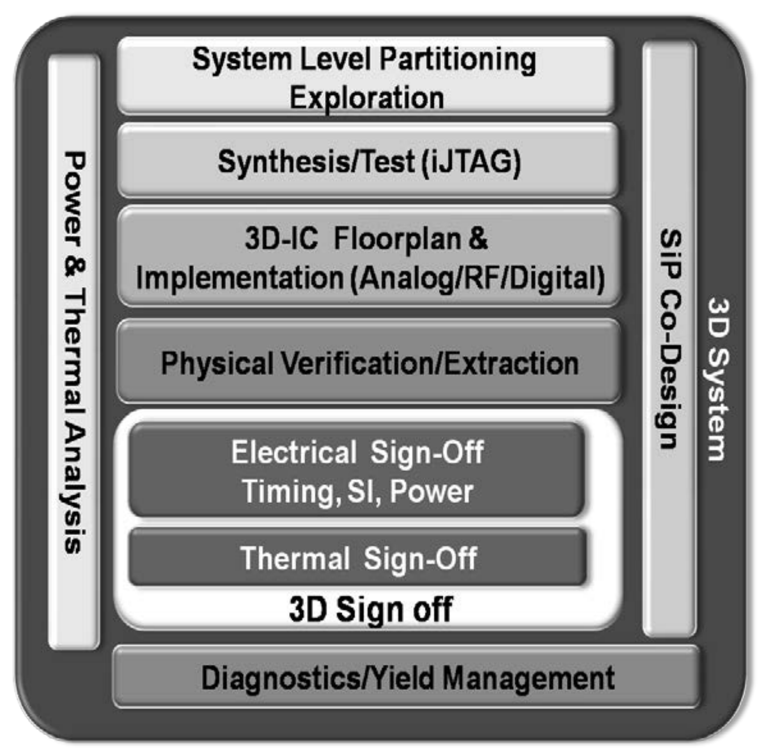
Cadence silicon-proven 3D-IC solution

Plan➔ implement ➔test ➔verify

- Allows heterogeneous integration to offer power, performance in smallest form factor
- **Cadence is technology leader providing complete and integrated 3D-IC solution**
  - Plan->implement->test->verify
  - 1st to market wide I/O memory controller
- **Developed in close partner-collaboration** for past 5 years with leading foundries and customers
- **Multiple 3D-IC tapeouts**
  - Multiple testchip experience: Memory over logic (28 nm), logic over analog, logic over Logic, 3-stack dies
  - Production design tapeout in mid-2010



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Several challenges with TSV technology

- Manufacturing Wide-IO DRAM and assembly
  - Test memory wafer after production using FC bumps
  - Thin the wafer to ~50-100um thickness
  - Form TSVs and fill with metal : Requires elevated temperatures
  - No opportunity to test here
    - Backside metal bump pitch too fine for most tester heads
  - Handle dies while avoiding mechanical damage
    - They are now the approximate aspect ratio of a postage stamp
  - Attach dies (and interposers, if present) together
  - Does it still work?
- Thermal Issues
  - Where does the heat go?
- Ecosystem Issues:
  - How many parties involved in stack production?
  - How are responsibilities divided?
  - How are liabilities divided?

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Conclusion

- Wide-IO and TSV are real
- Cadence believes that Wide-IO DRAM is the technology that will drive adoption of TSV
- Cadence stands ready with EDA tools and IP to enable your TSV designs with real experiences and partnerships with ~8 testchips and 1 production chip already completed.

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