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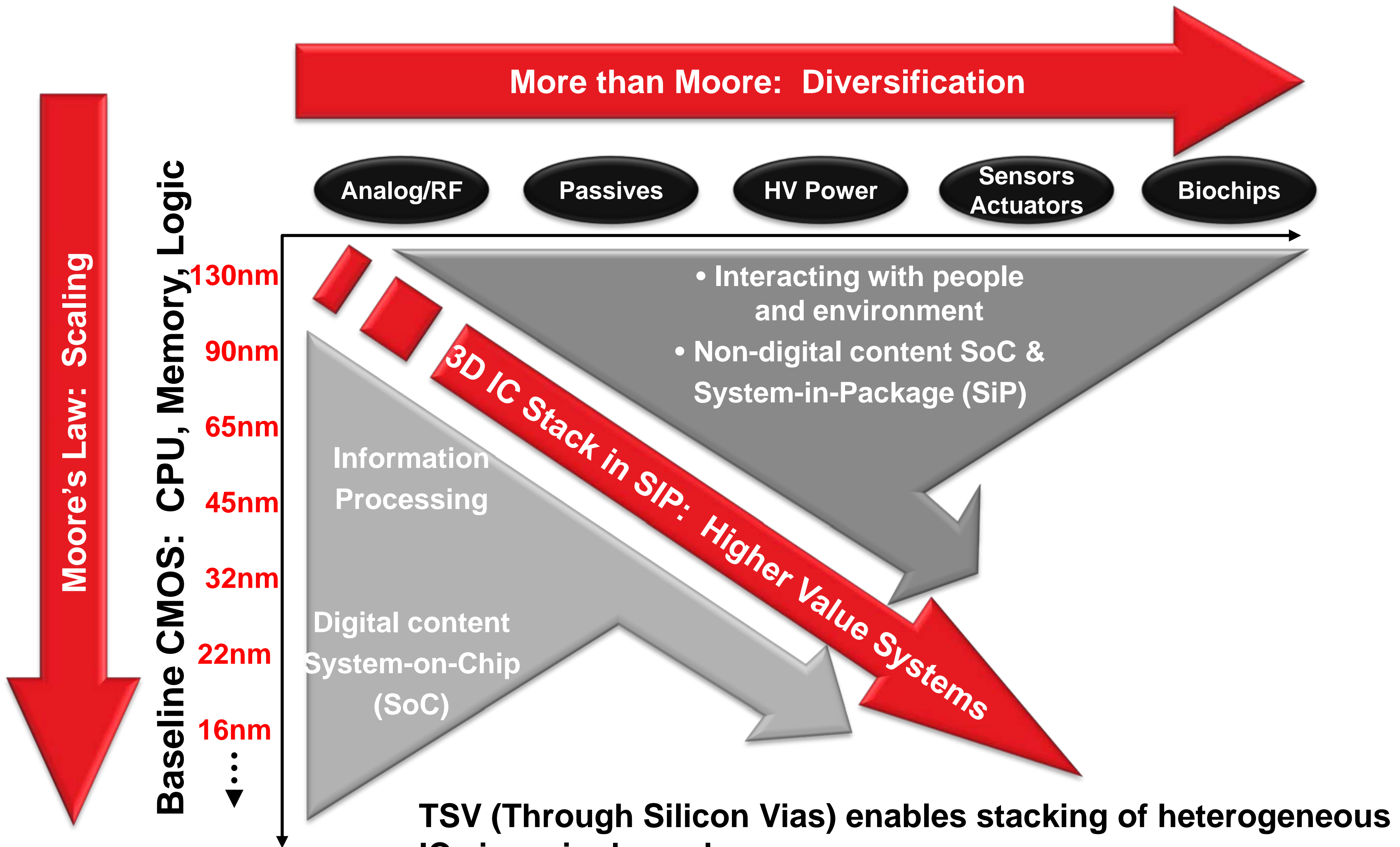
INVENTIVE

DFT-3D: What it means to “Design For 3DIC Test”?

Sanjiv Taneja
Vice President, R&D
Silicon Realization Group

Moore's Law & More : Tall And Thin



TSV (Through Silicon Vias) enables stacking of heterogeneous ICs in a single package

- Co-design & test across digital, analog, package

Source : ITRS

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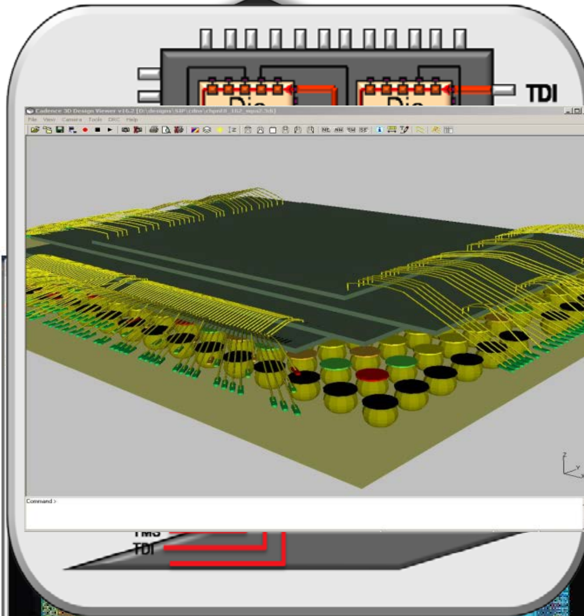
3DIC Design Flow Challenges

New 3DIC Design Flow Challenges

Block Selection e.g. DDR



System Level Exploration

3D Floorplan – Optimized power Plan and TSV/Bump locations

Implementation
Placement, Optimization and Routing

Extraction and Analysis
Manage Power, Thermal and SI

DFT for 3DIC Stack & Diagnostics

Silicon Package Co-Design/Test

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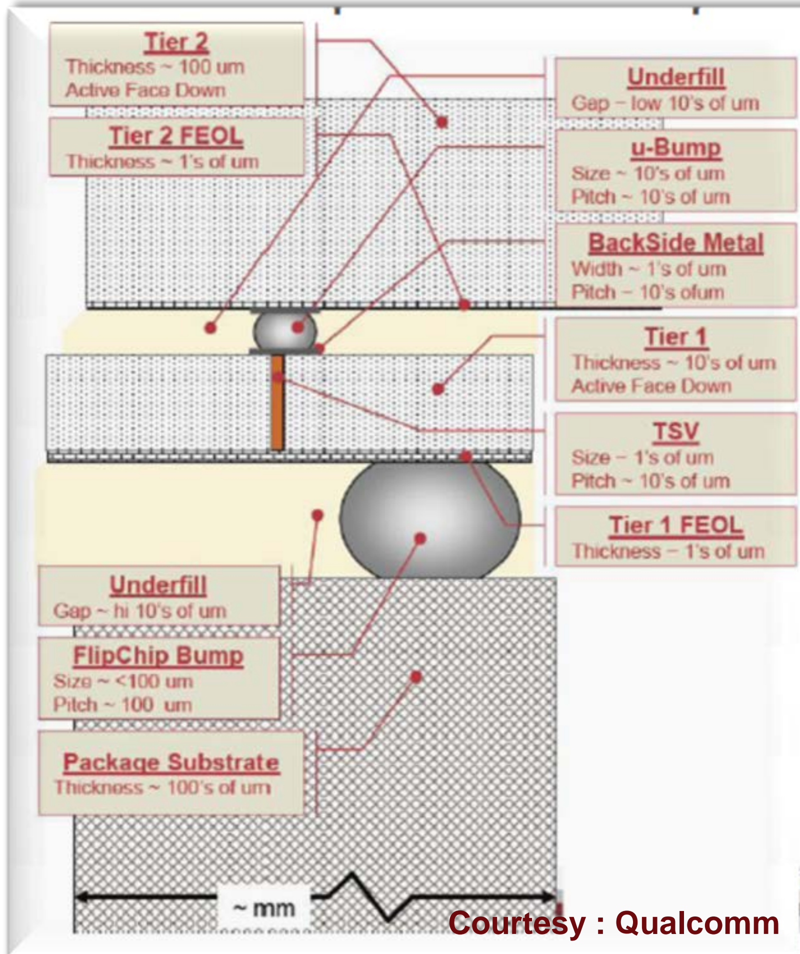
So what changes with 3DIC in EDA tools?

Revamped EDA requirements



- **New Layout Rules** (e.g. alignments)
- **New Layout Layer** (e.g. Back Side RDL)
- **New Layout/Electrical Feature** (TSV)
- **New Floorplanning/blockage rules**
- **Thermal & mechanical**
- **New Models, Rules**
- **New level of design/test integration**
- **New level of co-design and test**
- **3D DFT Architecture**
- **3D Test & DFT Standardization**

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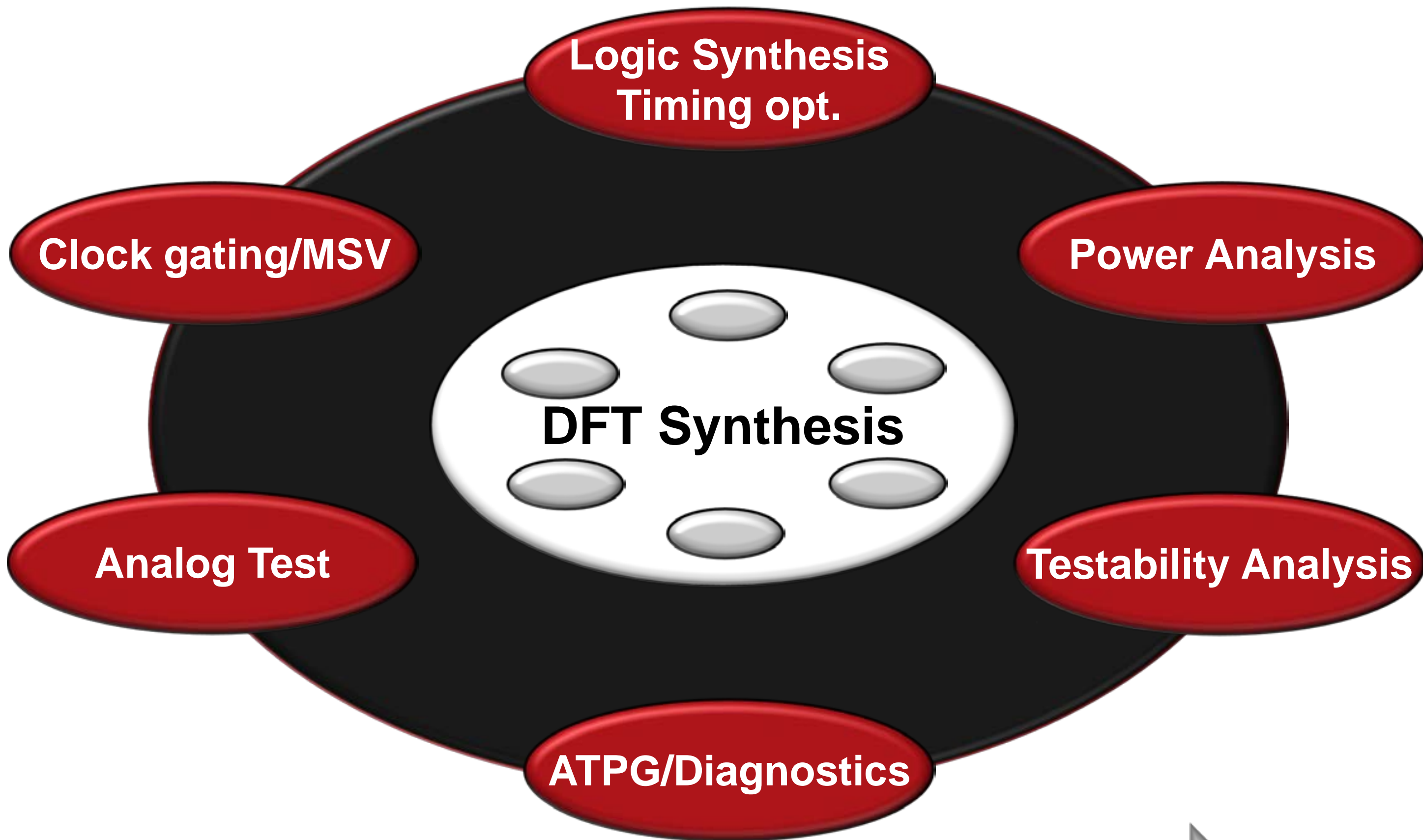
New level of integration and co-design

Multiple interacting requirements and features



From 'Design-For-Test' → 'Design-With-Test'

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DWT: Design-With-Test

Integration between design and test is key

- Integration between **design and test** becomes even more significant for 3DIC

Complexity of inter-die effects

Requires Concurrent optimization
Enabled by deeply integrated technologies
Across the entire flow

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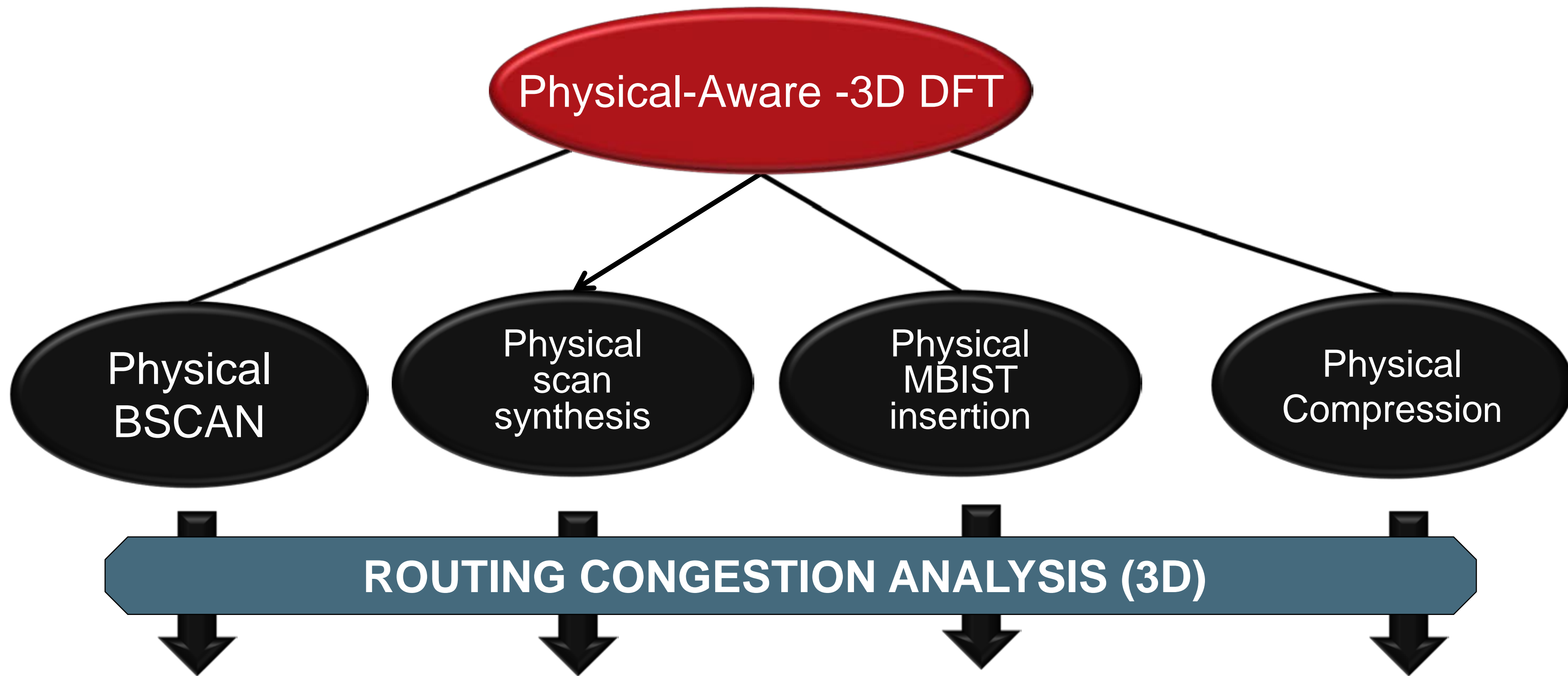
DWT Example: Physical-aware 3DIC



Concurrent optimization across PPA (power, perf., area) and Test constraints essential for predictability and test cost reduction of 3DIC

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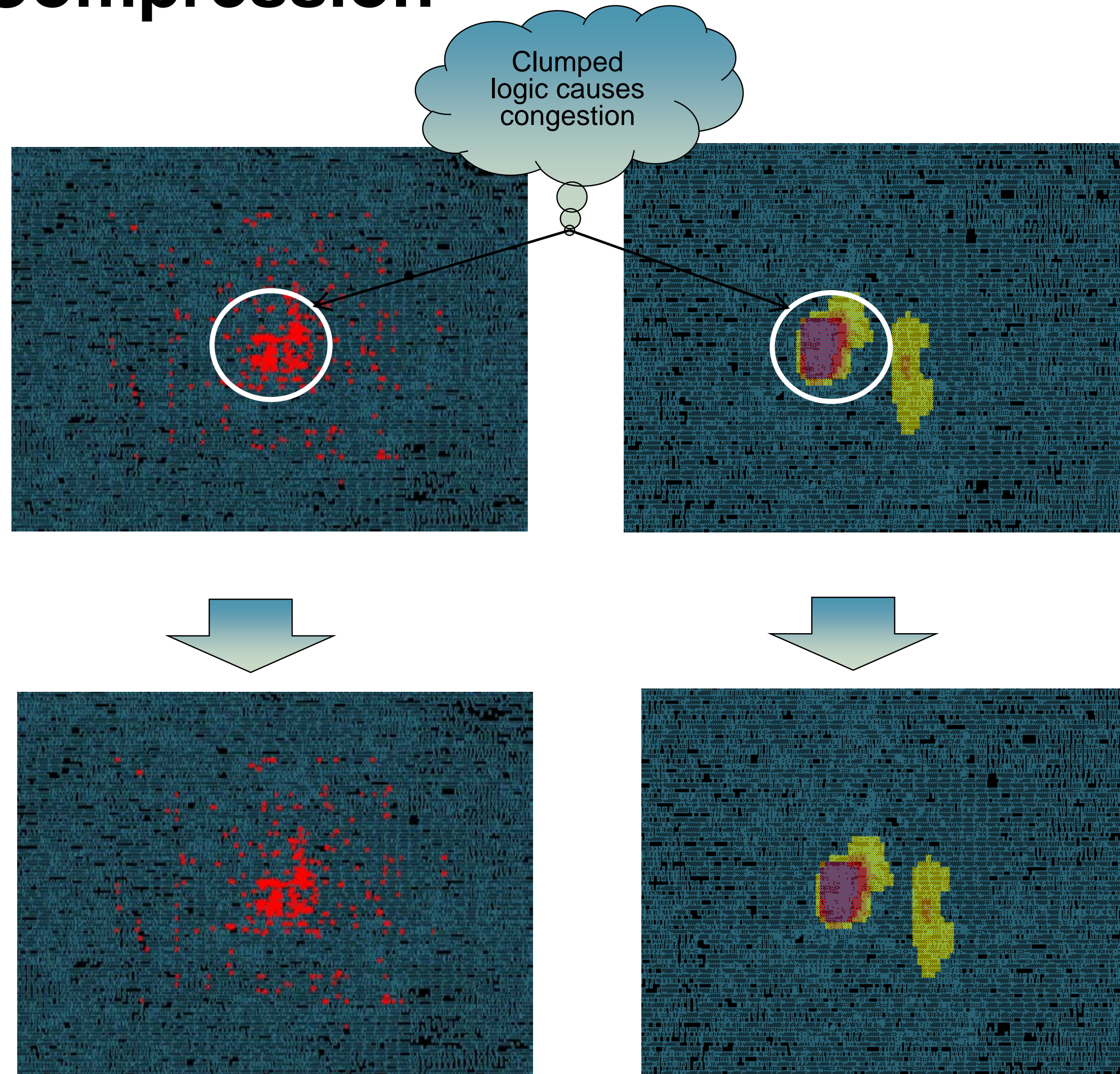
Physical-Aware Compression

Challenges:

- Due to dense connectivity standard placement algorithms can “clump” compression logic causing local congestion Routing congestion

Solution:

- Specialized DFT aware congestion driven placement algorithms can mitigate congestion without disturbing signal path placement



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3D Test requirements drive DFT architecture

- Limited test access with challenges similar to SiP
- New defect types (defects due to thinning, TSVs)
- TSV Interconnect defects
- Redundancy and repair of TSVs
- Key Technical Requirements
  - Ultra-low pin count compression
  - Reduced Pin Count Test
  - Pattern Fault model
  - 1149.1/1500 support
  - Creation of KGD after wafer test
  - A means to test the TSV interconnect between stacked die
  - A means to test inside the die of the stack

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DFT Architecture for 3D-IC

Leverage existing (and emerging) standards: 1149.1/.6, 1500, P1687 (iJTAG)

Functional Design

- ≥2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins

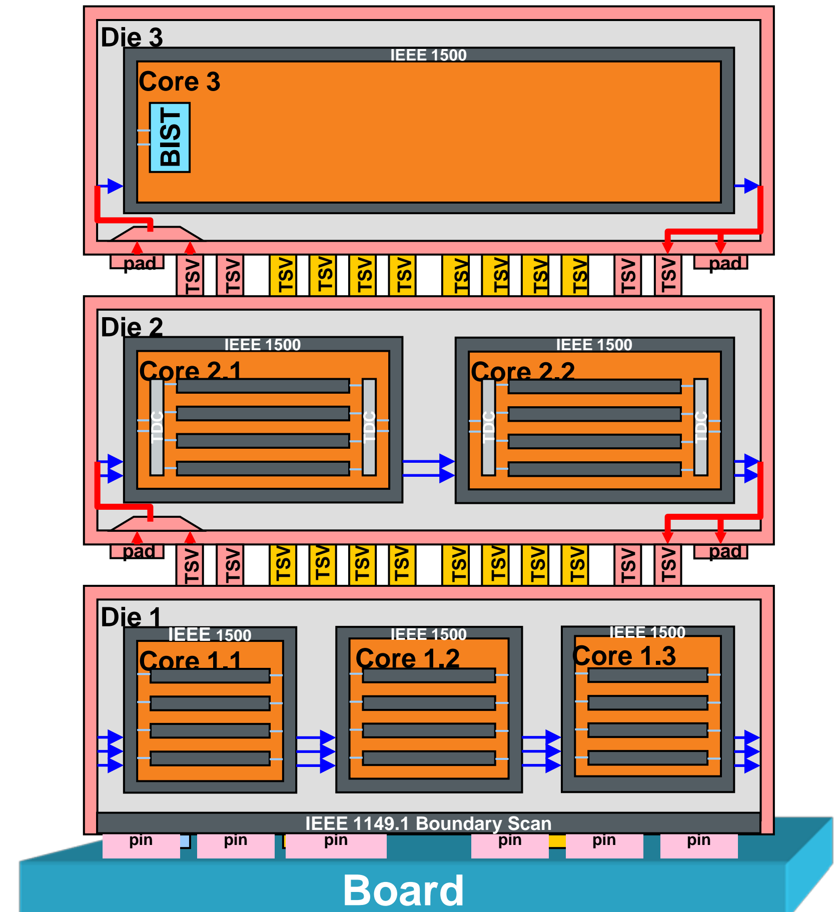
Existing Design-for-Test

- Core: internal scan, TDC, LBIST, MBIST, IEEE 1500 wrappers, TAMs
- Stack product: IEEE Std 1149.1

3D DfT Architecture

Test wrapper per die

- Based on IEEE 1149.1 or 1500
- Two entry/exit points per die:
  1. Pre-bond : extra probe pads
  2. Post-bond : extra TSVs



[Marinissen et al. – VTS'10 / 3DIC'10]

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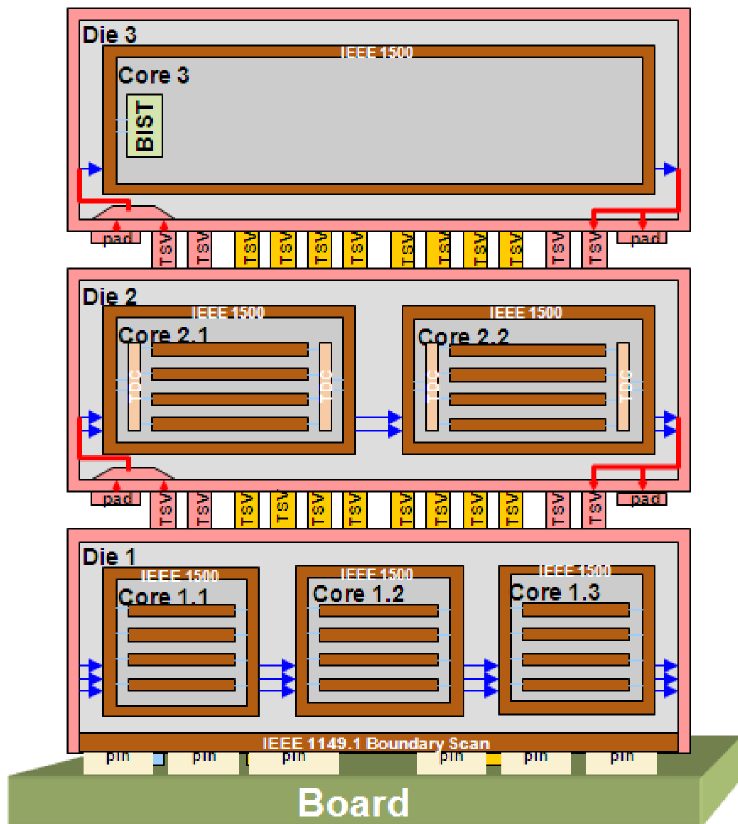
Test Generation for 3D-IC

Supports Silicon Interposer Flow



3D DFT on Die-Level
- Insertion of 3D wrapper
- Creating Test patterns
- Verification and Simulation

Testing Die Interconnects
- ATPG for die interconnects

Testing Die in a stack
- Modular Test approach
- ATPG-on-top test approach

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3-D Test and DFT Standardization

- 59 participants from companies/institutes around the globe
  - Chair: Erik Jan Marinissen (IMEC)

6. Standardization

Standardization Study Group

- **Organizational Infrastructure**
  - Active per January 2010, weekly WebEx calls
  - Public web site:
    http://grouper.ieee.org/groups/3Dtest/
  - Private web site and e-mail reflector for internal communication
- **Technical Topics**
  - *Die and Stack Test*
    1. Test access architecture : PAR ready to be filed
    2. Wafer probe interface : Under discussion
  - *Access for Board-Level Users*
    3. Board-level interconnect test : Under discussion
    4. Access to embedded instruments : Under discussion
  - *Test Data Formats*
    5. Wafer map and device tracking : Handled, SEMI E142
    6. Standard Test Data Format (STDF) : On STDF agenda

Source:
Erik Jan Marinessen (IMEC)

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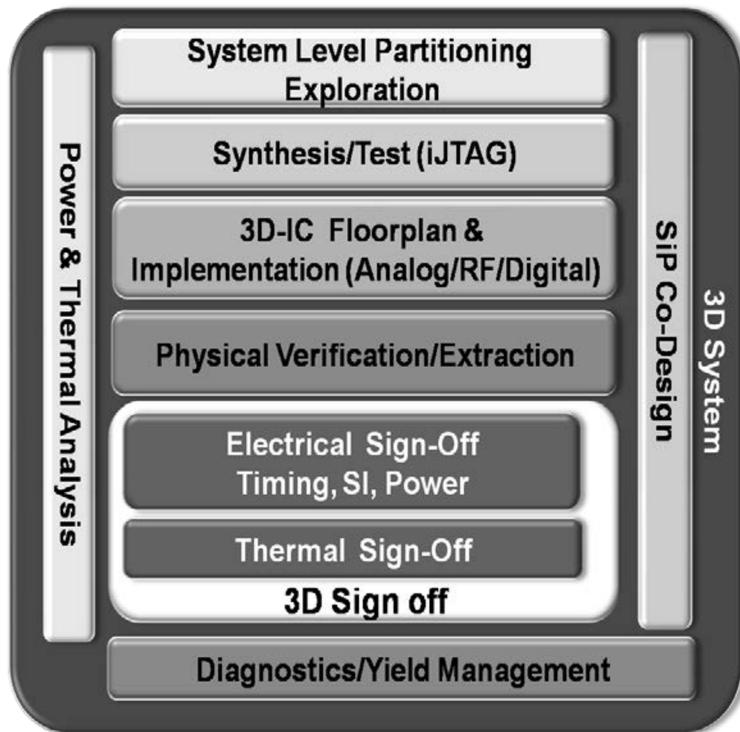
Cadence Silicon-Proven 3D-IC Solution

Plan➔ Implement ➔Test ➔Verify



- **Allows heterogeneous integration to offer power, performance in smallest form factor**
- **Cadence is technology leader providing Complete & Integrated 3D-IC solution**
  - Plan->Implement->Test->Verify
  - 1st to market *wide I/O memory controller*
- **Developed in close partner-collaboration for past 3 years with** Leading foundries and customers
- **Multiple 3D-IC tapeouts**
  - Multiple test chips: Memory over logic (28 nm), logic over analog, logic over Logic, 3-stack dies
  - Production design tape-out in mid-2010

Riko Radojcic, Qualcomm

> Collaborative partnerships are a crucial part of Qualcomm's work on 3D ICs. For example, Qualcomm is working with Cadence on thermal solutions, and Radojcic said the Cadence collaboration and Qualcomm's use of the Encounter Digital Implementation System helped Qualcomm produce its first TSS test silicon.

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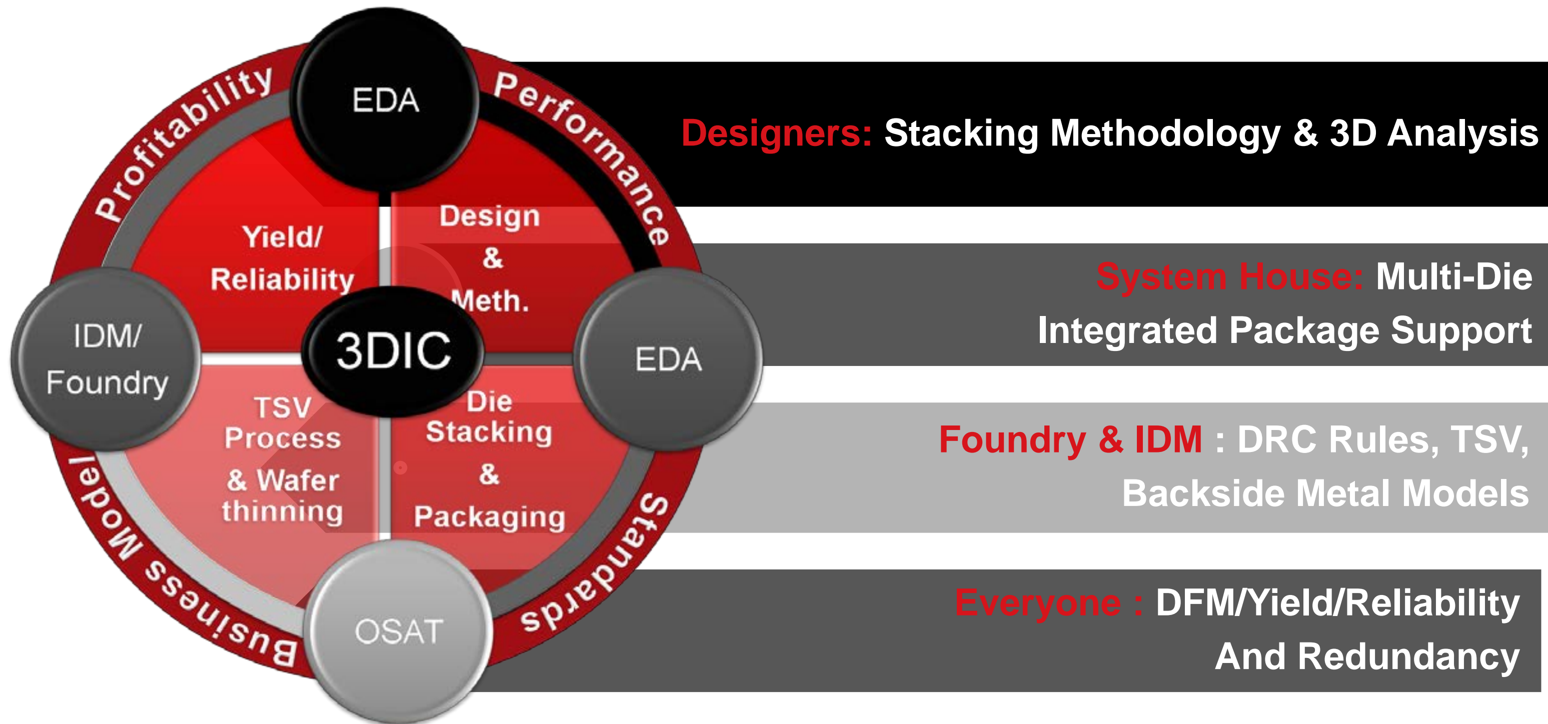
3D-IC Test Collaboration in the Ecosystem



EDA DFT + ATE company

Prove 3D solution on Tester

Build awareness of the current state-of-the-art
Support standardization effort

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Questions to ponder ?

New failure mode with TSV

Failures due to Thermal and Mechanical stress

Cost Management of 3D-IC system

Lowest cost point : additional silicon area for DFT versus tester time

Over heating or failed IC : Parallel testing, High-speed testing

How to avoid costly failures