# Ultra-Low Power System Design for Ultrabooks™

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# Agenda

- Link Power Management
  - HIPM, DIPM and DevSleep
- Device Power Management
  - Idle, Standby, Sleep, RTD3
- Windows 8 - Connected Standby
- PCIe Power Management

# SSD Interfaces

- In PCs (excluding Tablet) SATA is ~100% market share today
- Vast Majority of new PC shipments are 6Gb
- Majority of Channel/Upgrades are 6Gb but many go into 3Gb sockets
- Transition to PCIe will begin in 2013
- PCIe could be the dominant interface in 2015 new PC shipments

# Link Power Management

- SATA Standard and Most advanced chipsets support:
  - 2 low power states
    - Active – PHY ready and on, full power, no wake up latency
    - Partial – moderate power savings, fast wake up latency
      - Unlikely to be combined with core power management
    - Standby – greater power savings, slower wake up latency
      - Likely to be combined with core power management
  - 2 ways to enter
    - HIPM – Host Initiated Power Management
      - Chipset or Driver detecting drive not in use
    - DIPM – Device Initiated Power Management
      - Typically timed period of inactivity
- SATA Standard and Future chipsets add:
  - 1 more lower power state
    - Device Sleep – zero PHY power, even slower wake up latency
      - Likely to be combined with core power management

# Core Power Management

- SATA Standard Power Management supports 4 states:
  - Active, Idle, Standby, Sleep
    - Entry through command or timer set by host
- Device may employ different strategies to lower power with different entry and exit latency profiles:
  - Reduced Frequency
  - Clock Gate, shut down circuitry
  - Remove power to peripherals
  - Lower voltage supply
- Device may enter low power state in Active mode
  - Must guess when host can tolerate longer wake up latencies
    - Don't want to incur latencies when host is likely to be active on drive
  - Cue off Link Power Management Commands
  - Timed period of inactivity

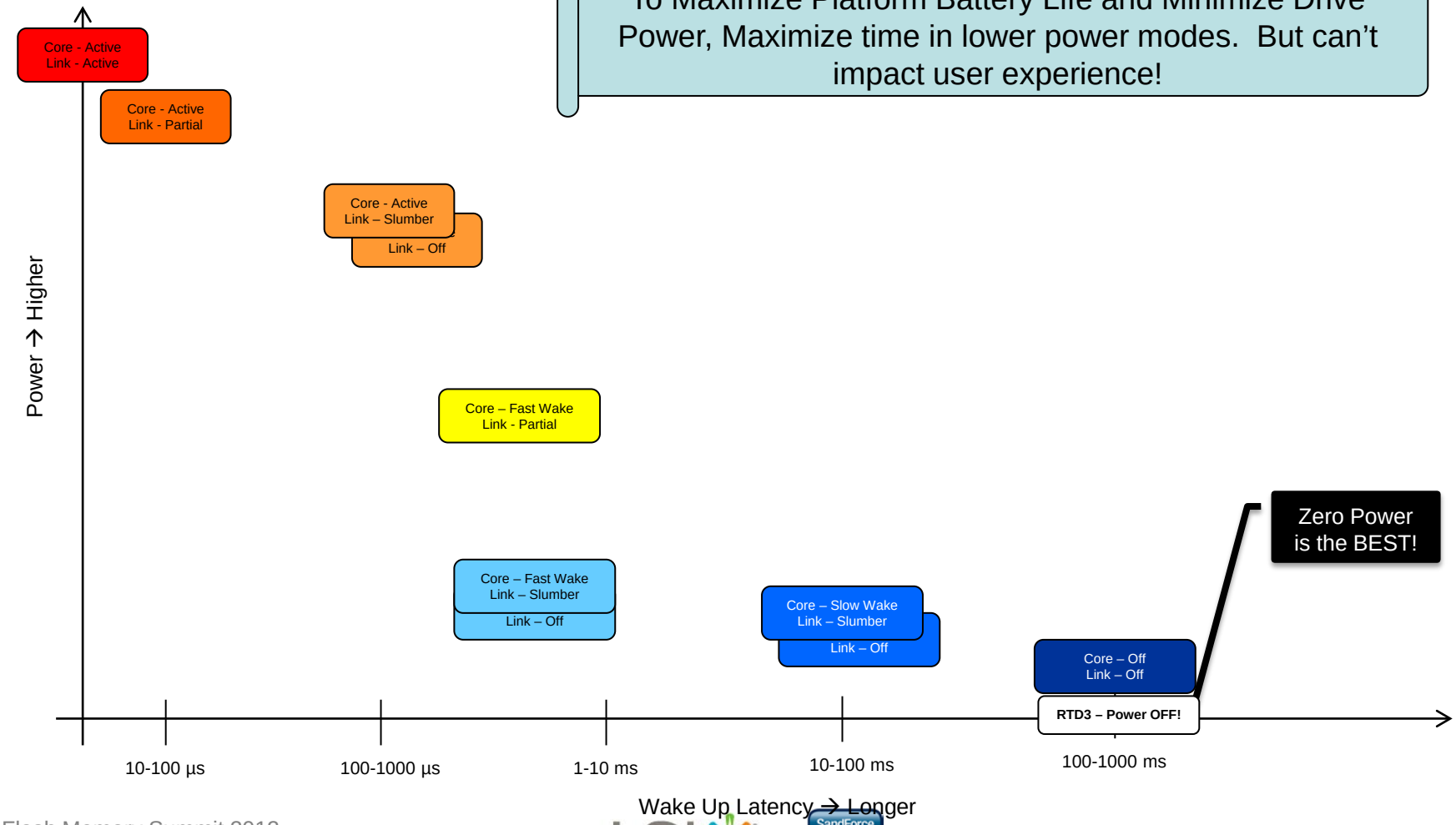
# Total SSD Power Consumption

**Total Power ≈ Regulator Efficiency * (Link Power + Core Power + Peripheral Power)**

- In DevSleep Link Power = 0
- In Run Time D3 “RTD3” Total Power = 0 !!!
- Core Power depends on design
- Minimize peripheral power by gating voltage to Flash, LEDs, etc or put Flash in standby

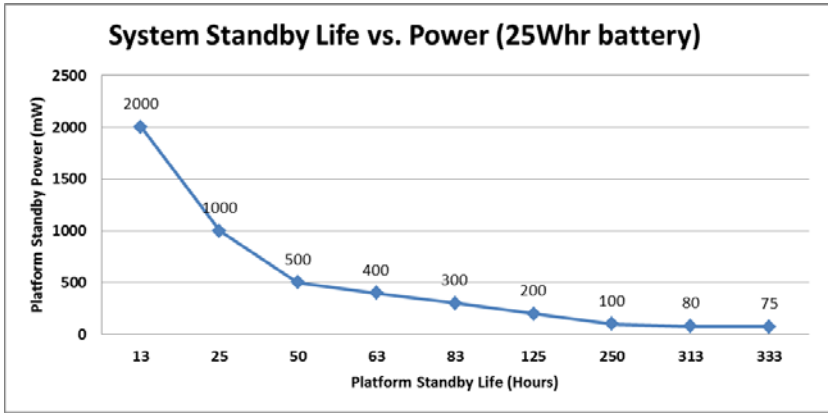
# Relative Power and Latency Chart

To Maximize Platform Battery Life and Minimize Drive Power, Maximize time in lower power modes. But can't impact user experience!



# Windows 8 Connected Standby

- Connected standby is the scenario of having your PC be *always on and always connected* in the new connected standby state without excessively draining your battery, so that you have access to your important and up-to-date information whenever you need it. When your Windows RT PC is not in use, it will move into a new low-power mode that allows it to keep your data fresh and current while also not requiring a battery charge for days. And when you need your system, it will turn on in less than a second at the touch of a button, which is a mobile phone experience but in a full PC.
- Early production Range 320hrs to 409hrs with 25 Whr to 42Whr battery
  - Source: MSDN Blog: Mike Angiulo, VP of Ecostystem and Planning team http://blogs.msdn.com/b/b8/archive/2012/08/13/collaborating-to-deliver-windows-rt-pcs.aspx
- Do the Math
  - 25Whr/320hrs <80 mW standby power for the entire PC
- What is the budget for storage
  - Industry sources say <5 mW budget!
  - Target for DevSleep = 5mW
  - RunTime D3 = 0mW = >20hrs more battery life



# PCIe Adoption into Ultra thin and light Notebook category

- PCIe connected SSDs provide great promise for the next round of innovation and enable further performance gains
- PCIe and the NVMe protocol do have robust inherent capabilities but the industry must iterate to optimally utilize them in systems
- Challenges still exist
  - Link Power Management not as proven implementation
  - Multiple links drive more power (Shut down lanes dynamically?)
  - Dev Sleep equivalent still needs some detailed definition

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