Increase Controller Performance & Energy Efficiency

Without sacrificing programmability

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Who is Tensilica?

Leading supplier of processor cores and SW for “data-plane”

Business Model – Semiconductor IP licensing

- **Processor IP for the data plane**
  - Deeply embedded control, DSP, application-specific accelerators
- **Shipping in over 20 application areas**
  - Storage, Audio, Baseband, Printers, Cameras, Network infrastructure/access…
- **Licensed by several major flash controller companies**

Market

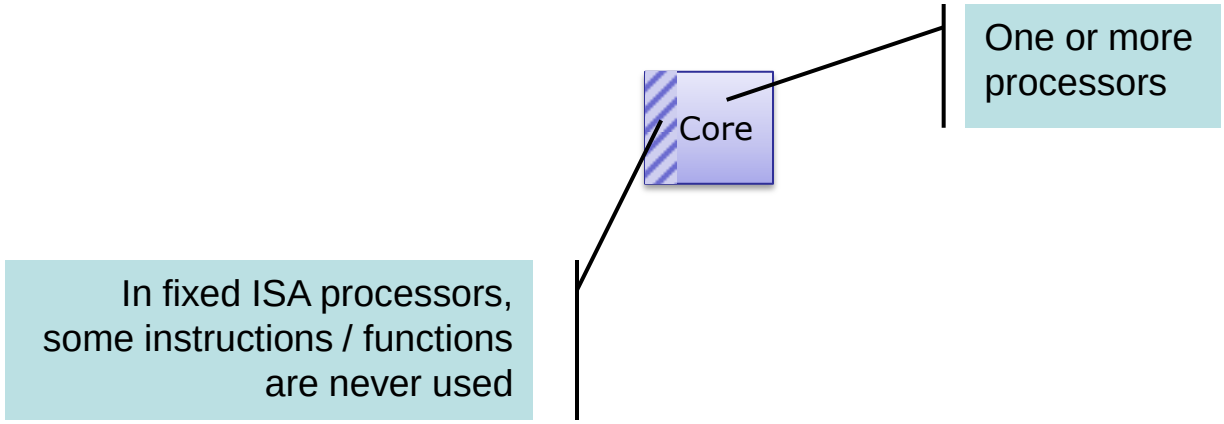
- **Nearly 2 Billion cores shipped!**
  - Run-rate approaching 1B cores/yr
- **190+ Licensees worldwide**
  - By 8 of the top 12 semiconductor manufacturers
  - In 7 of the top 12 Smartphone manufacturers’ products

Company Facts

- **Privately held. Venture backed. Profitable, cash positive for many years.**
- **Headquarters and major operations in Santa Clara, CA**
- **Sales offices worldwide (US, UK, Japan, Korea, China, Taiwan)**

Increase Performance & Energy Efficiency

Your current design has one or more processor cores…



…you need 2x more processing in the next design, but energy consumption & programmability are also important.

What are your options…

Increase Performance & Energy Efficiency

Eg: 2x faster in next design – what are the options?

Run the core at 2x clock frequency

May not be possible

Benefits

Easy development

Costs

Lower energy efficiency

Pushing process limits results in a proportionally larger & higher power core.

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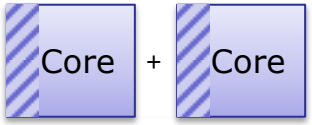
Eg: 2x faster in next design – what are the options?

Add more cores



Benefits

Manageable hardware changes.

Familiar development environment.

Costs

Software partitioning work.

Coherency management
in Hardware and/or Software

Similar energy efficiency
A little worse from management overhead

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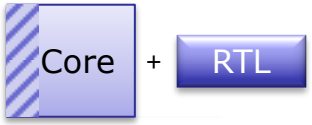
Eg: 2x faster in next design – what are the options?

Offload bottlenecks with RTL



Benefits

Higher energy & area efficiency.

Small software changes.

Costs

RTL development and significant verification.

Lose programmability in RTL state machine.

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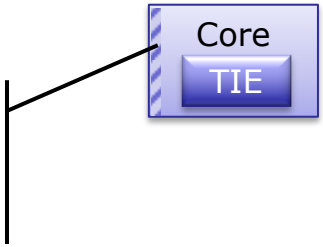
Eg: 2x faster in next design – what are the options?

Offload bottlenecks with Xtensa using TIE

Xtensa is configurable.
Do not include instructions / functions that are never used



Benefits

Higher energy & area efficiency.

Dramatically less verification.

Small software changes.

Costs

Modest TIE hardware development.

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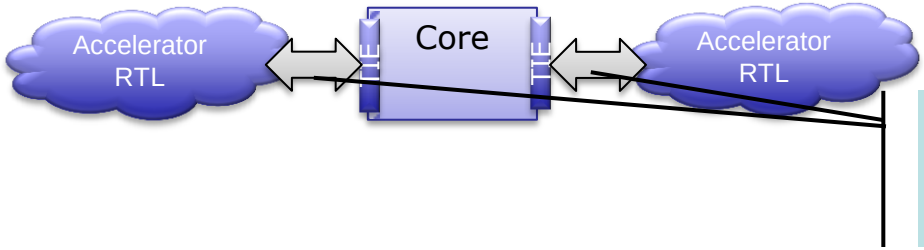
Eg: 2x faster in next design – what are the options?

Directly interface to accelerators for faster I/O



Up to 1024 bits wide.
Multiple connections.
GPIO, FIFO, Memory

Benefits

Multi high bandwidth interfaces.
Up to 1024 bits each, simultaneously.

Avoids system bus.
No arbitration, frees up bandwidth.

Predictable latency.

Costs

Add simple TIE instructions
to define interfaces.

Small software changes.
Instruction controlled interface rather than memory mapped.

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Eg: 2x faster in next design

Summary of development options

Option		Δ Size	Δ Energy Efficiency	Δ Software	Δ Hardware
Core	Current design	-	-	-	-
Core	2x MHz If possible	~<2x	<1x	0 ☑	0 ☑
Core + Core	Multiple Cores	~2x	~1x	Large Coherence, Partitioning	Small Resource arbitration ☑
With identifiable bottlenecks…					
Core + RTL	Offload Cycle reduction	<<2x ☑	>>1x ☑	Small Interfacing	Very Large RTL Design + Verification
Core TIE	Xtensa Cycle reduction	<<2x ☑	>>1x ☑	Very Small Add intrinsics ☑	Small[1] TIE Design ☑

[1] Typically small, can scale with desired performance improvement

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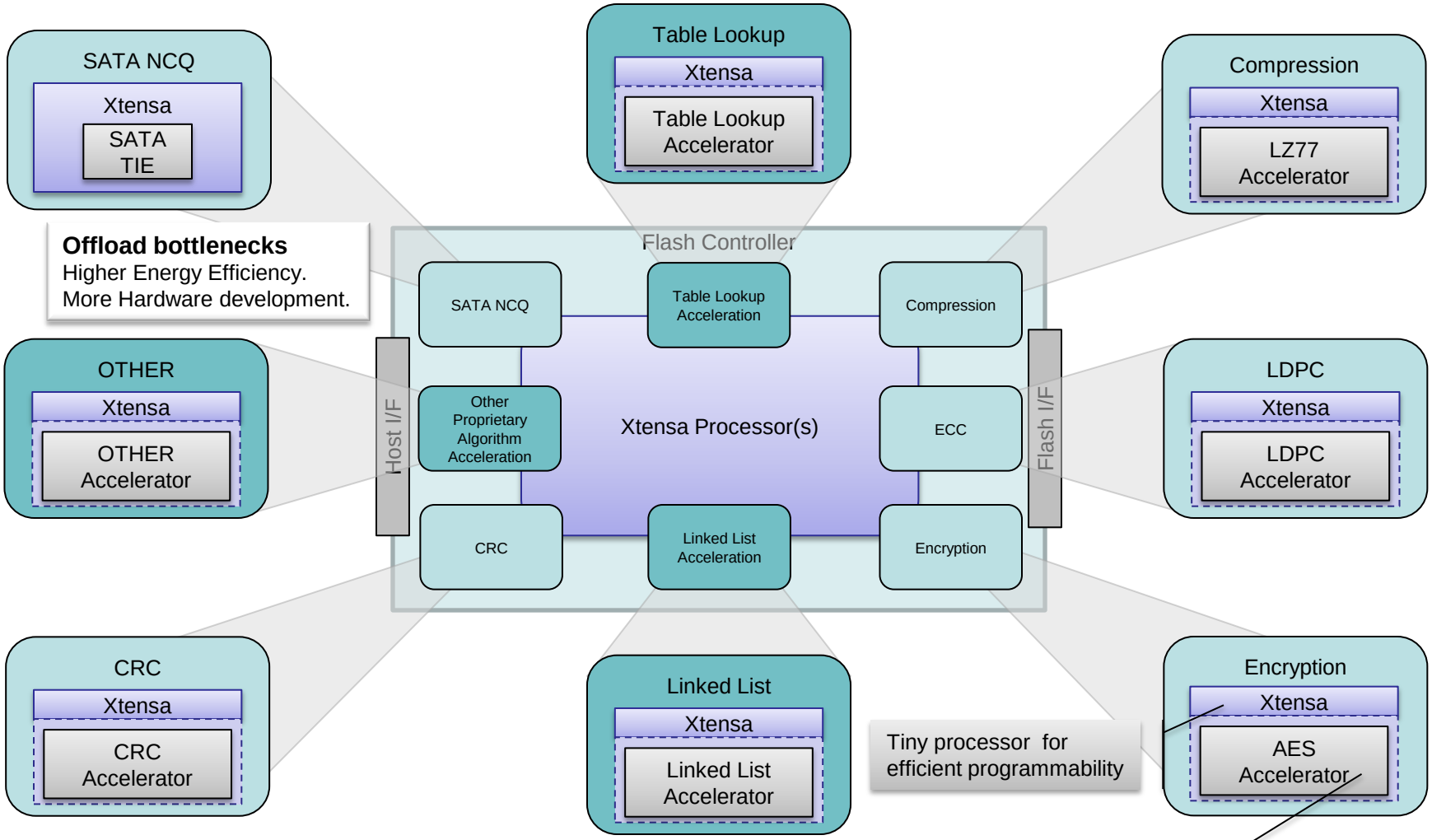
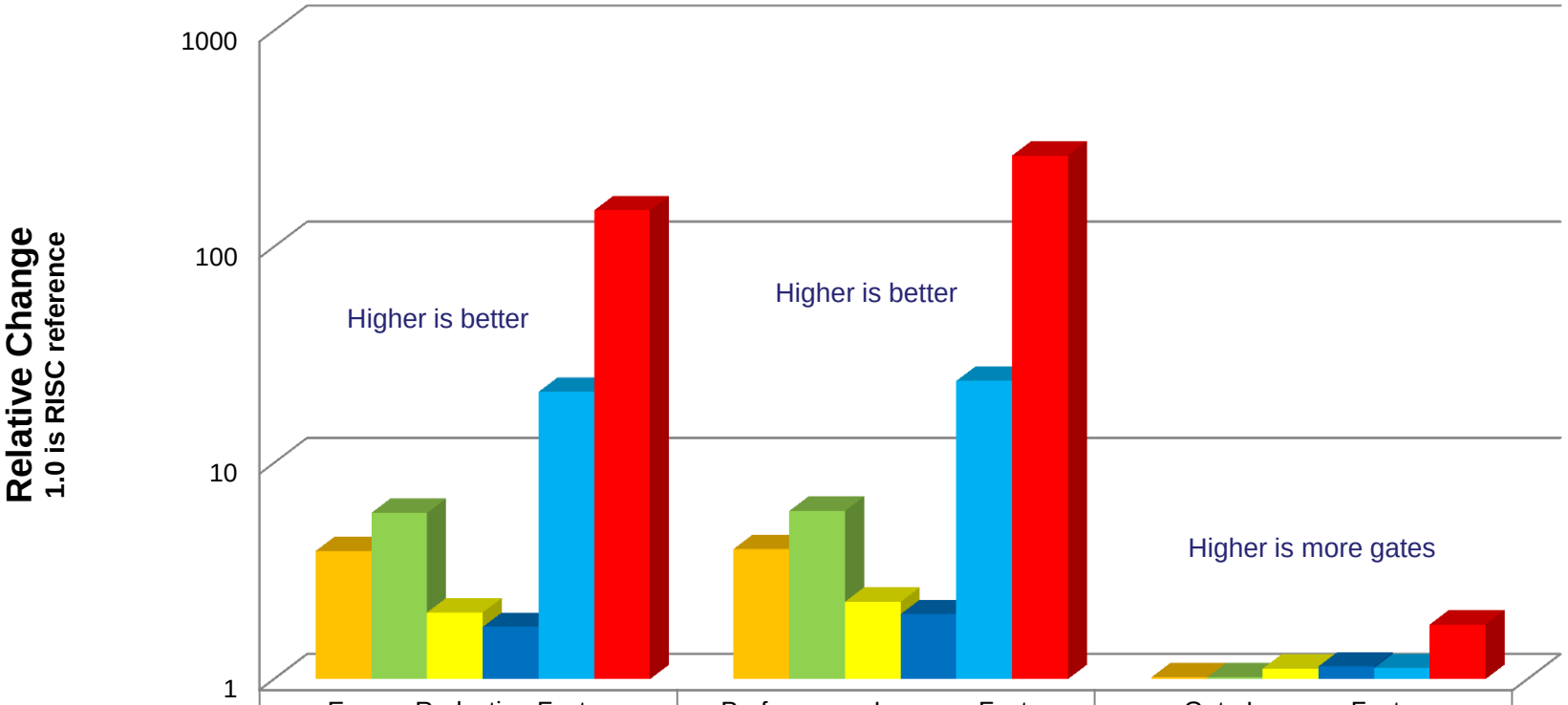
… with programmability in your flash controller



Flash Controller Offload

Summary of real Xtensa examples



	Energy Reduction Factor	Performance Increase Factor	Gate Increase Factor
Linked List Search	4	4	1.02
Table Lookup	6	6	1.02
LZ77 Compression	2	2	1.12
CRC16 Table	2	2	1.15
CRC16 HW	21	24	1.13
AES-XTC 256	148	265	1.79

For more information

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