Advanced Flash Technology Status, Scaling Trends & Implications to Enterprise SSD Technology Enablement

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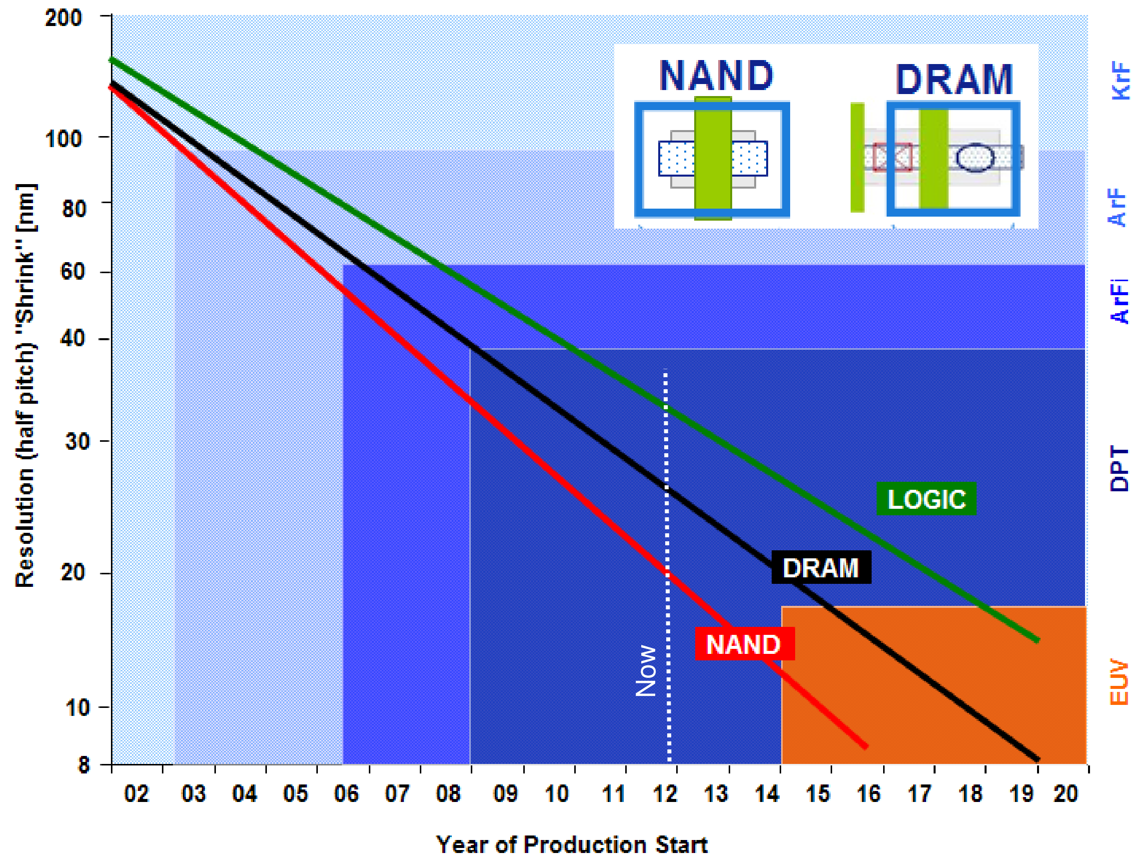
Outline

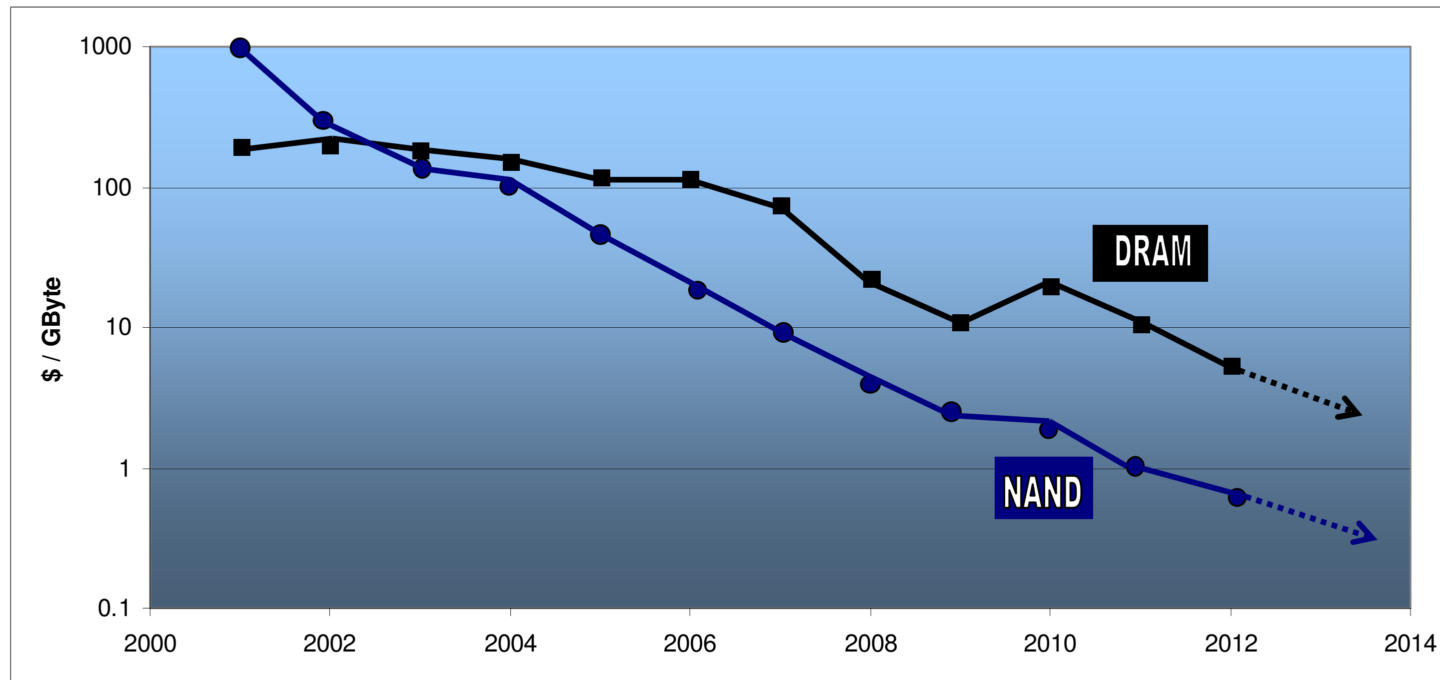
- Si Technology scaling trends – Flash, DRAM & Logic
- Flash Technology scaling challenges
    - Floating Gate Si Process Integration challenges
- NAND reliability challenges @ sub 20 nm
- Cell Architecture & 3D NAND key directions
- Signal Processing & Implications to SSD Technology Enablement
- Manufacturing, Fab Technology & Quality
- Die & Package Cost Analysis
- Packaging Technology
- Summary

Si Technology Scaling Trends & Outlook



- NAND continue to drive Si minimum feature scaling – 2H12 NAND @ 1xnm and DRAM @ 2xnm node in mass production
- NAND Floating gate scaling expected to extend to 1y nm in 2012-2013 > transition to 3D NAND cell in 2014-2015 timeframe enabling path for ‘Effective Sub10nm’ scaling

NAND & DRAM Cost per GB Trend*

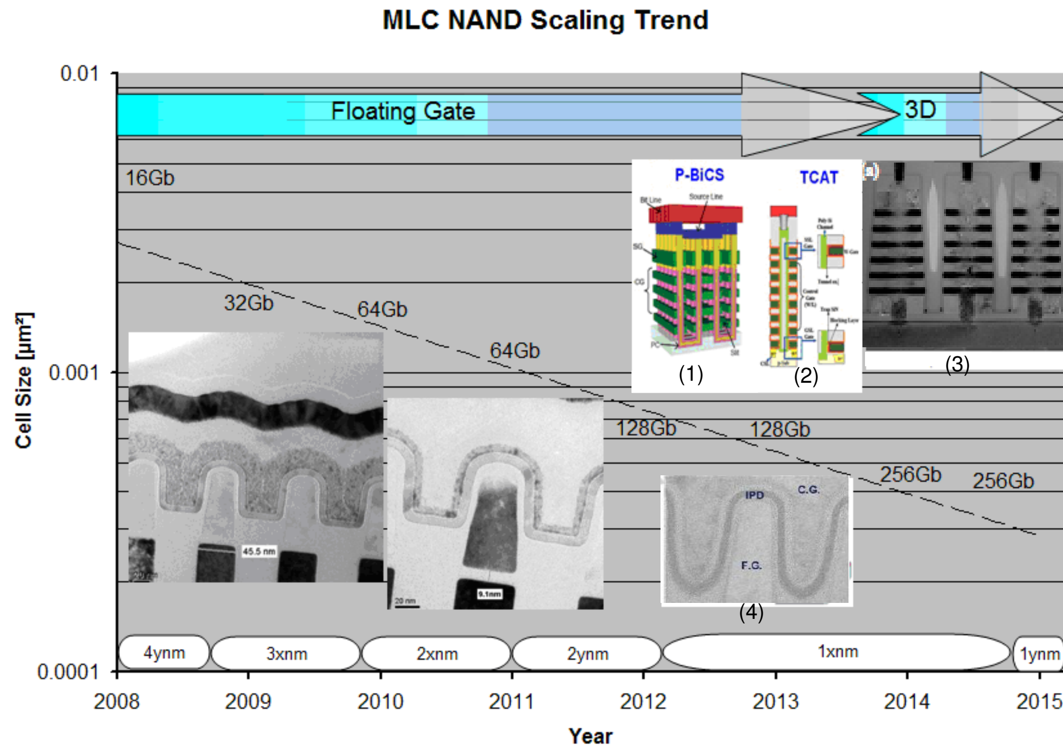


* Commercial grade
NAND/DRAM pricing

Source = DRAM Exchange/IDC/ASML

- *NAND & DRAM market driven by cost per bit – scaling fueled by die cost reduction opportunities*
- *NAND flash cost slope fueled by Consumer & SSD applications in 2008-2014 timeframe*
  - *SSD cost reduction driven by NAND scaling - SSD @ ~$4/GB (vs HDD @ ~$0.4/GB) in 2H12*

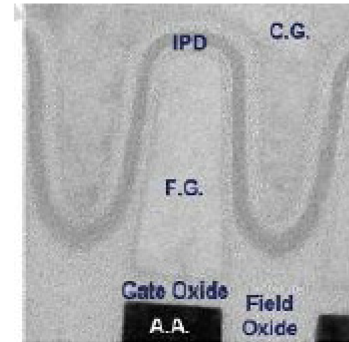
NAND Scaling Status & Future Directions



	2009	2010	2011	2012	2013	2014	2015
Technology (nm)	3x	3x	2x	2y /1x	1x /1y	1y/1z	1z
Cell Architecture	Floating Gate	Floating Gate	Floating Gate	Floating Gate	Floating Gate	3D NAND/ Floating Gate	3D NAND
ECC/Signal Processing	BCH	BCH	BCH/Read Retry	BCH/Read Retry/LDPC	BCH/Read Retry/LDPC	Advanced Signal Processing	Advanced Signal Processing
MLC Density (Gb)	32	64	64	128	128	256	256

1. M. Ishiduki et al., IEDM2009-626, 27.3.1-4
2. J. Jang et al., VLSI 2009, pp192-193
3. Y. Noh et al., VLSI 2012, pp19-20
4. A. Fazio, IEDM 2009 27.7.1-4

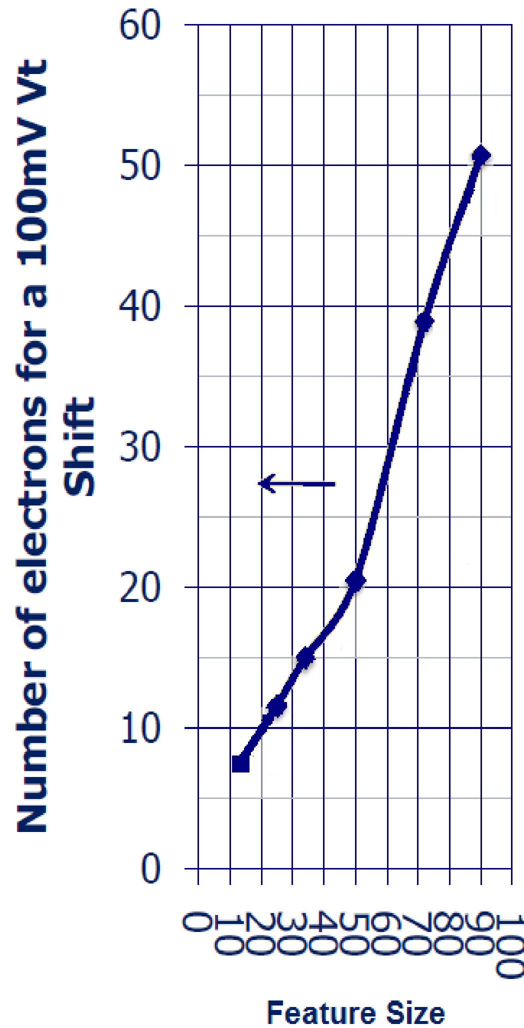
NAND Technology – Scaling Challenges



A. Fazio, IEDM 2009 27.7.1-4

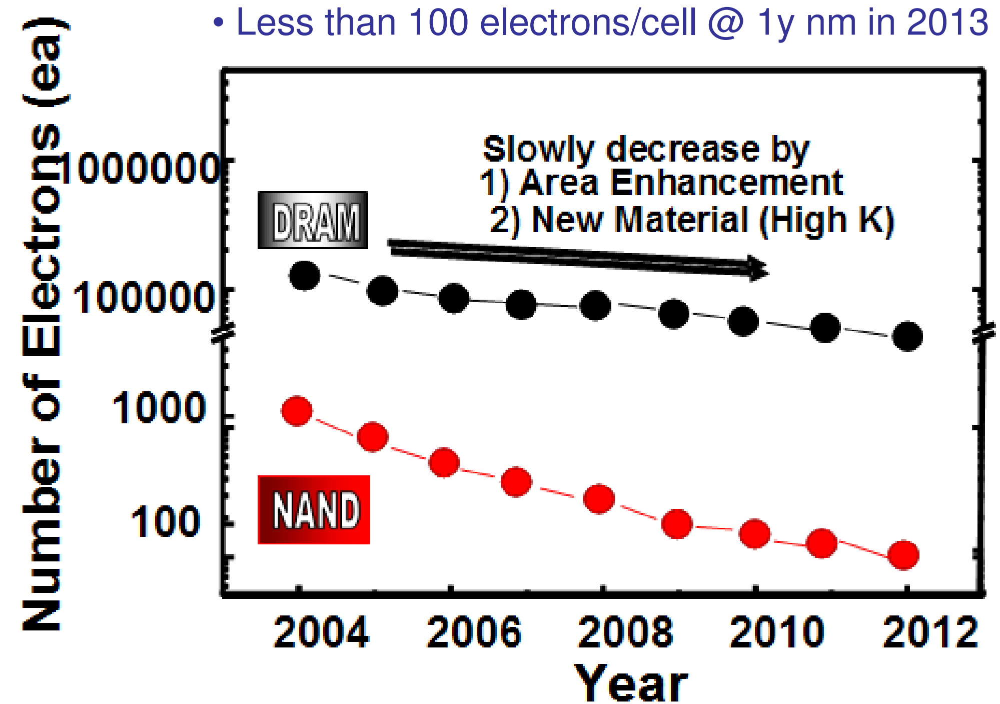
- As Floating Gate geometry shrinks, the same amount of charge loss causes larger Vt shifts – **causing endurance & data retention degradation with NAND scaling.**
- FG-FG capacitive coupling and interference.
  - 3D NAND Charge Trap Flash- potential workaround for this limitation (1z nm node in 2014-2015)
- Narrow FG-FG space doesn't leave enough room for the two inter-poly dielectric layers.
  - Floating gate scaling challenge @ sub 2xnm NAND
  - Planar floating gate cell with High-K Metal gate at sub 20nm – maintain control to floating gate coupling ration with smaller area
- Main challenge is cell endurance, data retention. Cell operation window and Program Disturb due to High program fields
- Commercial grade MLC @ sub 20nm targeted at ~3K endurance/1 Year data retention target spec – with Process Technology, Design innovations and Signal processing

NAND Scaling Challenges – Floating Gate Charge

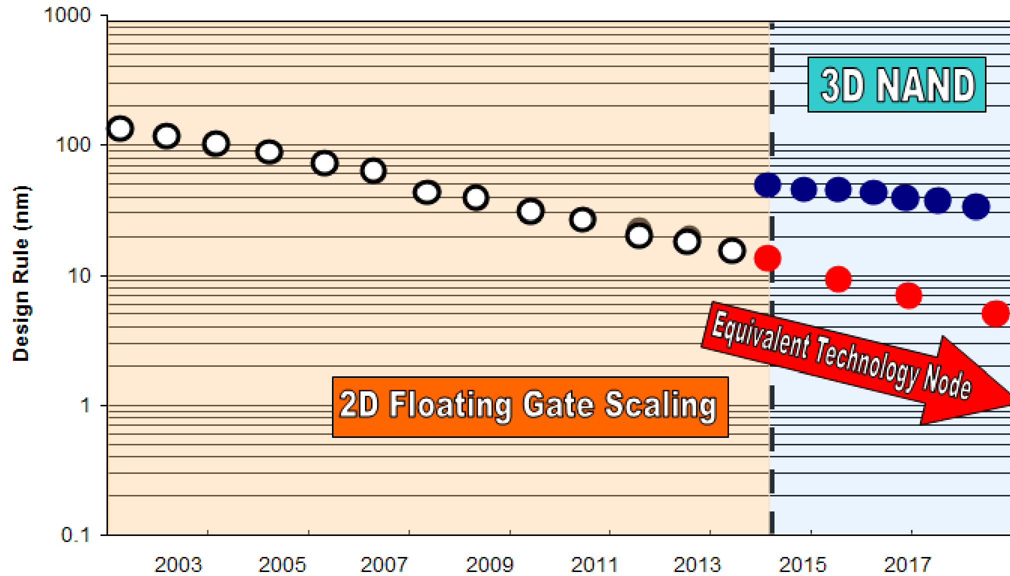


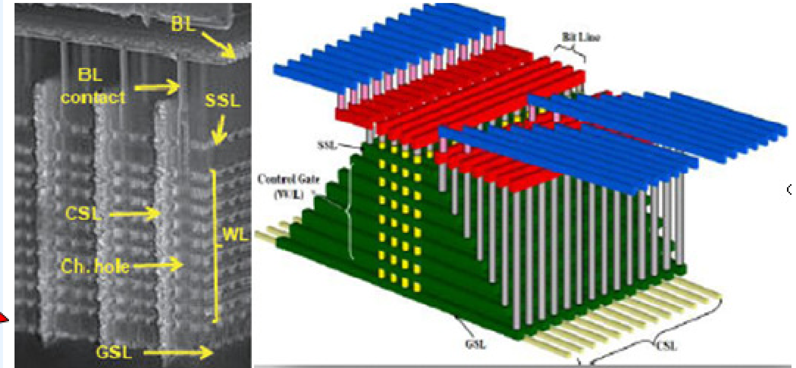
As NAND Technology node is scaled down, the number of electron/cell decreases. A small number of electrons (charge loss/gain) can result in dramatic effects on Vt.

- Less than 100 electrons/cell @ 1y nm in 2013



NAND Scaling Outlook

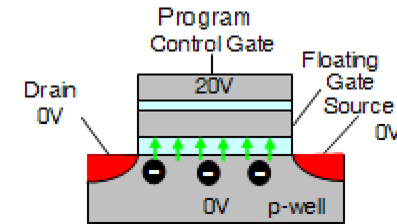




J. Choi et. al., VLSI Tech Digest, pp178-179, 2011

- 2D Floating Gate Flash expected to face significant scaling challenges at '1z nm' (10-13 nm) Technology Node in 2014-2015 timeframe
- 2D scaling challenges driven by significantly degrading reliability and cell-to-cell interference effects causing degradation in operating window at sub 20nm node
- 3D NAND will allow 'Effective Flash scaling' into sub 10nm with 3D cell architecture
  - 3D-NAND cell based on charge trap technology, cMLC Target Reliability @ 3K endurance
    - Investigate opportunities for reliability improvements with 3D/Charge trap
  - 3D-NAND offers cost effective path for sub 10nm Flash scaling – non EUV based solution, # of litho layers
  - Manufacturing, Yield & Quality critical learning must occur in 2013-2014 timeframe
  - 3D-NAND long term scalability may be challenging for >45 stack cells
- RRAM is lead candidate as potential 3D-NAND replacement in the 2017+ timeframe

NAND Reliability



• **Endurance** - Number of Program/Erase cycles a cell is expected to be able to withstand.
Failure mechanism is caused by charge trapping in gate oxide. Commercial MLC NAND at 2x –1x nm sustained @ 3K endurance

• **Data Retention** - Charge is lost on the floating gate over time. Block can be erased and reprogrammed. C-MLC spec'd @ 1year, E-MLC @ 3month with max pre-cycled condition

Affected mainly by three mechanisms.
* High temperature accelerates rate of charge loss.
  - Charge de-trapping can occur.
* Stress Induced Leakage Current (SILC)
  - Degradation caused by P/E cycles
  - Voltage accelerated
* Cell Disturb
  - Activity on adjacent pages or cells can cause gradual buildup of charge on floating gate

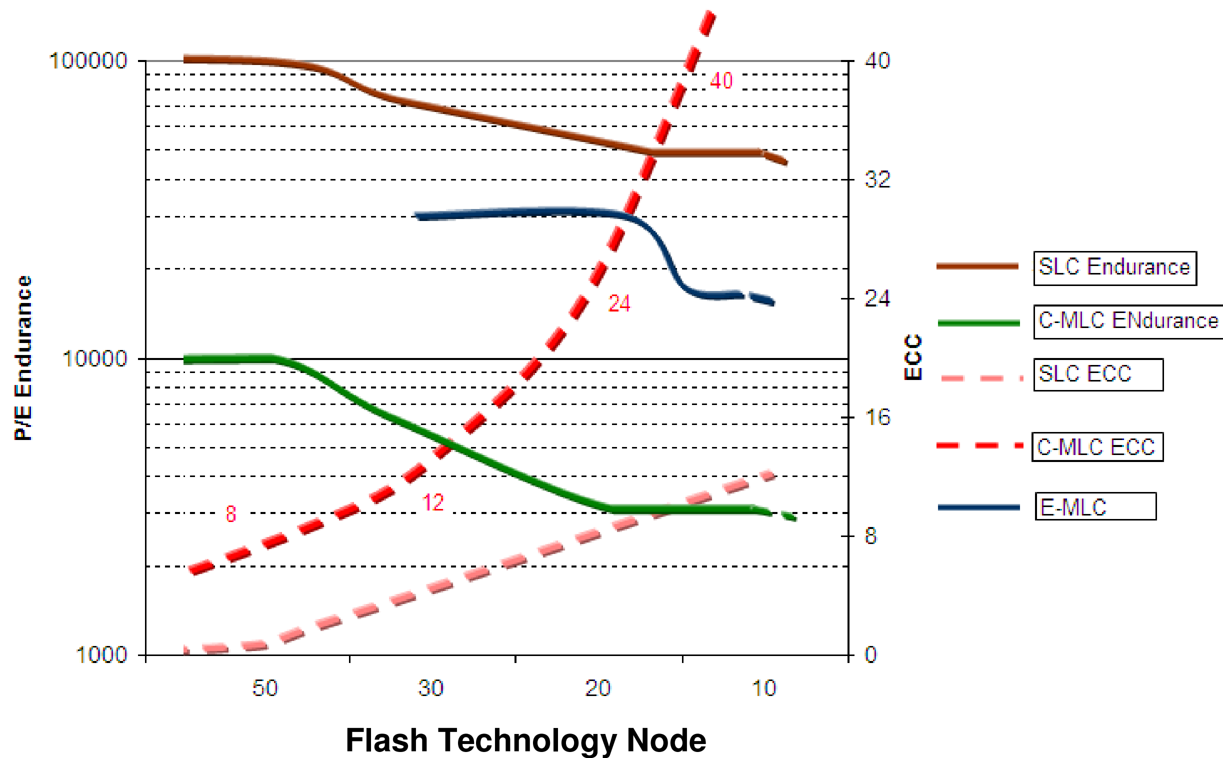
• **Program Disturb** – Charge collects on floating gate causing the cell to appear to be weakly programmed. Partial page programming accelerates disturbance

• **Read Disturb** – Pages not selected for read see elevated voltage stress. If enough charge collects on floating gate, cells can appear to be charged, causing a flipped bit

*** as geometry shrinks, the same amount of charge loss causes larger Vt shifts – challenge to endurance & data retention for sub 2x nm Floating Gate MLC NAND*

• **Temperature effect** - i) Effect on Charge Trap/De-trap kinetics (Data Retention/Endurance) and ii) Intrinsic Failure Modes vs Temperature with typical exponential dependency

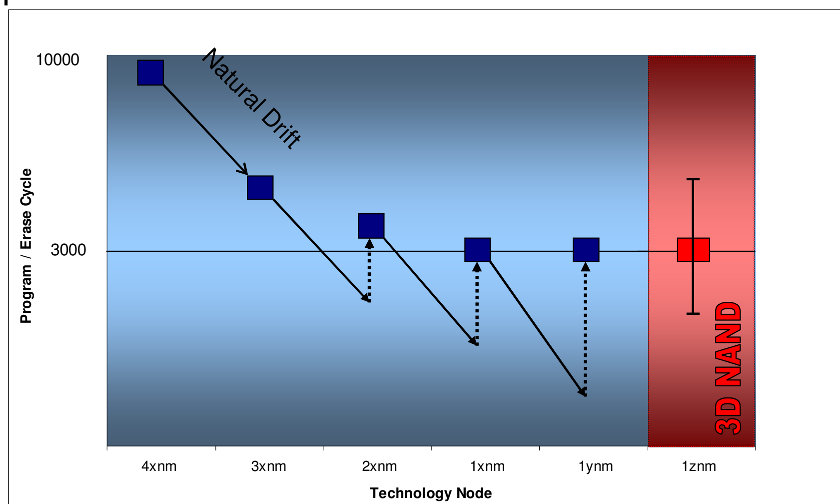
NAND (cMLC, eMLC, SLC) Endurance & ECC Trends



- Endurance & Data Retention cycles has been decreasing with process shrinks – 5x ~ 1xnm node
- ECC requirements increasing exponentially with process shrinks
- Advanced ECC algorithms, signal processing techniques critical for Enterprise SSD enablement in 2012-2015 timeframe (using sub 20nm MLC flash)

NAND Reliability Outlook

- **cMLC** Floating gate & 3D-NAND Endurance Target will be maintained @ 3K thru 2xnm>1xnm>1ynm transitions in 2012-2014 – driven by consumer cMLC reliability requirements
  - 1x/1y nm scaling will require process technology innovations & usage of advanced signal processing
  - Advanced Signal processing will be key in SSD enablement based on sub 1x nm cMLC (Floating gate & 3D NAND) Flash
  - Need to explore cMLC extended endurance capability with relaxed data retention (3 month @ 40C) requirement



Maintain 3K endurance vs NAND scaling via:

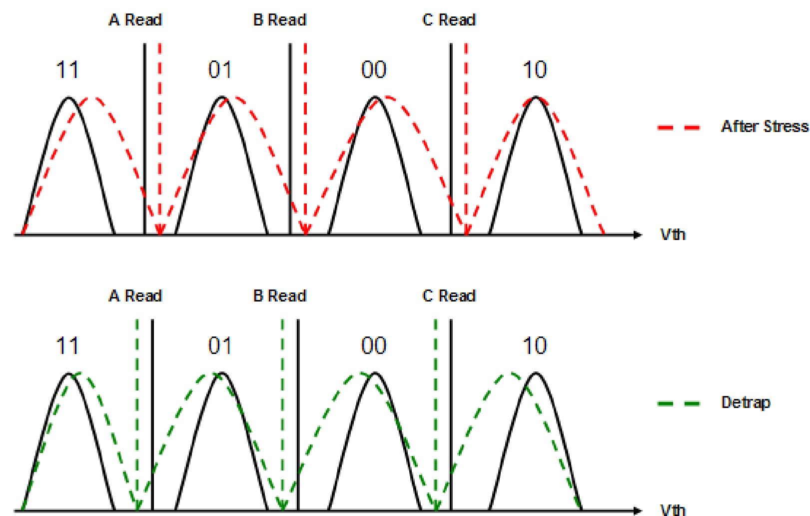
- **Process Technology Innovation**
  - Air Gap
  - High-K/metal gate
  - Advanced FG cell process architecture & design
- **Signal Processing**
  - Read Retry
  - Strong ECC, LDPC

- **eMLC** 30K/3month reliability @ 3x -2x nm – enabler for current industry Enterprise SSD
  - eMLC price premium over cMLC - key factor in future Enterprise SSD directions

Flash signal processing – Implications to SSD Technology Enablement

NAND scaling vs Vt distribution widening – mitigation via signal processing

- Vt distribution widening due to i) reduced # of electrons per cell and ii) adjacent cell interference with 2D NAND scaling
- Read Retry needed starting @ 2xnm eMLC & cMLC
- Advanced DSP techniques including FG coupling compensated read, LDPC, Soft Data Algorithms needed @ 2y/sub 1x nm nodes
    - Latency increase at device end of life must be evaluated

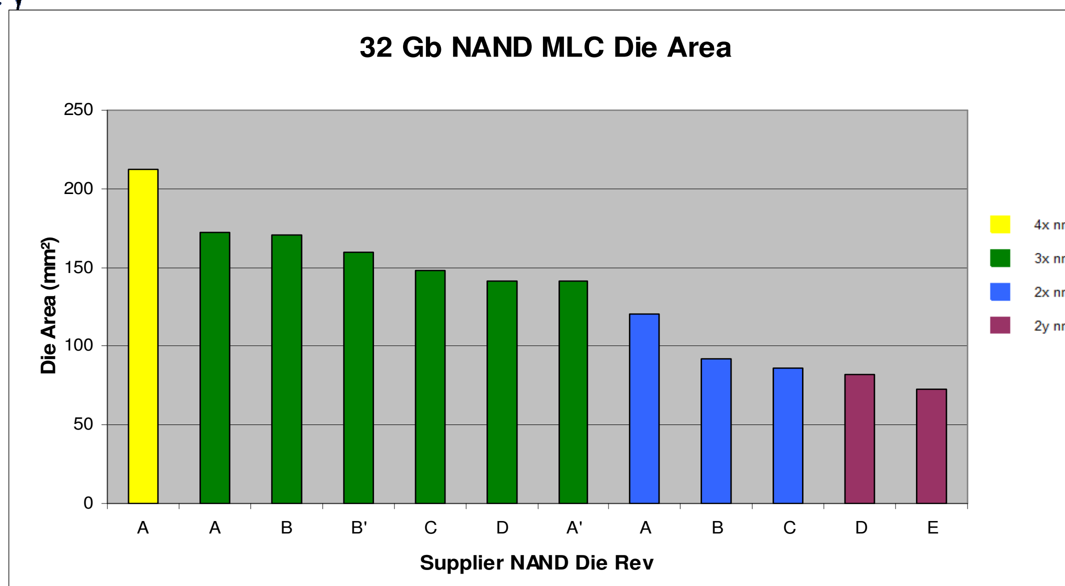


➢ ***Advanced Signal Processing critical in 1x /1y nm Flash usage for Enterprise SSD applications – Understanding of Flash/Controller reliability capabilities & latency impact to SSD End of Life is key***

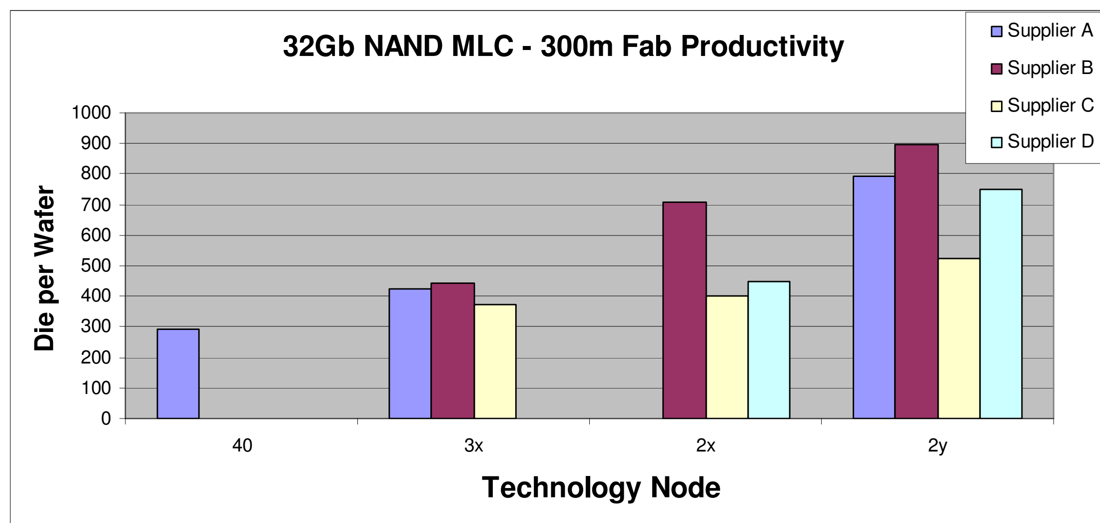
Advanced Memory Manufacturing & Quality

- Leading edge 300mm NAND/DRAM fab manufacturing – driven by productivity, efficient, yield and quality requirements, typical fab capacity @ 100-150K WPM, Mostly dedicated NAND/DRAM fab strategy
- Fully integrated MES (Manufacturing Execution System) – integrates various sub-data/control systems in ensuring robust quality system
- Focus on SPC/APC based process controls & small drift controls – 'nano' scale process window control requirements needed for robust quality
- FDC (Fault Detection Control) methodologies critical for sub 30nm NAND & DRAM manufacturing quality control
- Rigorous & thorough equivalency practices required – across multiple fab locations spread out in widely different geo's
- DFM (Design for Manufacturing) critical in areas of lithography OPC, Design rules, layout and pattern density effects

Flash Die Size/Cost Factors

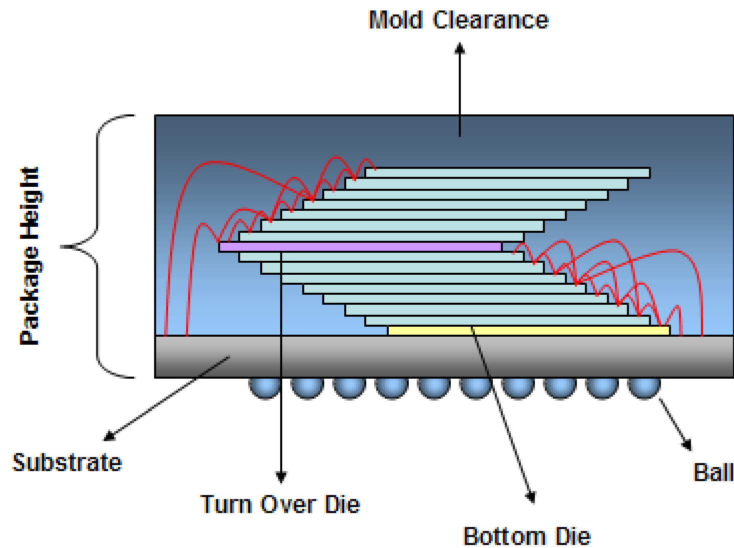


- Flash Die Cost reduction enabled by Lithography node transition
- NAND Flash Productivity (i.e., Die cost reduction) strongly driven by advanced Si technology enablement

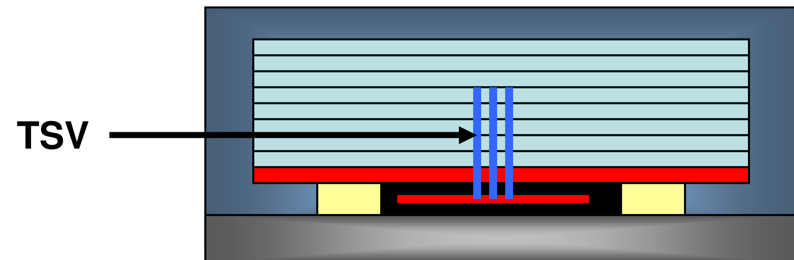


Flash Packaging Technology – Key Directions

- High reliance on stacked packaging – currently at 8DP, stacked package development focused on 16DP+ & TSV (Thru Si Via) stacked package
- 8DP/16DP stacked packaging – Enabling 1-2Tera Bit Flash package (using 128Gb MLC Flash die @ 20nm node)
- Focus on TSV Stacked Flash package – driven by power consumption & performance gain



Flash 16DP package



Flash TSV package

Summary

• Flash market driven by cost per bit – scaling fueled by die cost reduction opportunities. Competition for smallest die size will continue thru lithography scaling, cell architecture, and design innovations – advanced lithography technology key factor in speed of NAND cost reduction

• NAND floating gate scaling expected to reach significant challenges at 1y /1z nm technology node. 3D NAND provides path for 'sub 10nm effective scaling' thru 3D Cell stacking in the 2014-2016 timeframe

• Signal Processing Technology & Strong ECC critical in meeting enterprise SSD reliability requirements with 1x /1y/ 1z nm NAND flash

•300mm NAND manufacturing & quality systems key in memory quality & reliability – focus on SPC/APC based process controls, FDC, DFM, equivalency and particle reduction needed

• Flash has been driving force for Advanced Stacked Packaging Technology – 8DP BGA current mainstream, development focus on 16DP+ stacking & TSV

• sub 20nm NAND scaling & Advanced signal processing critical in meeting Enterprise SSD enablement in 2012-2016 timeframe