THE DEMISE OF SLC IN THE ENTERPRISE

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INTRODUCTION

- SLC is no longer the best solution for write intensive SSDs
- There are emerging MLC solutions with better specs and lower cost
- Will show how to compare SLC and MLC solutions and quantify the MLC advantage
- Similar analysis suggests that TLC will replace MLC for entry level SSDs



IT'S ALL ABOUT DENSITY!

• It's the density, stupid!

• MLC density is driving innovation to displace SLC



HISTORICAL PERSPECTIVE

- Decades of innovations to increase the density of storage
- Not all innovations are readily accepted
- Ultimately the higher density solutions tend to prevail



HISTORICAL PERSPECTIVE (2)

	nited S	States Patent [19]	[11]] [45]]		
[54]		EMENT FOR ENCODING AND	Primary Exc		
	DECODIN	Attorney, Ag			
[75]	Inventors:	Bernardo Rub, Marlborough; Lih J. Weng, Lexington, both of Mass.	Cefalo; Ron [57]		
[73]	Assignee:	Digital Equipment Corporation, Maynard, Mass.	The present which in on		
[21]	Appl. No.:	375,931	length data use with a means, such in another m words to dat such that in a		
[22]	Filed:	May 7, 1982			
[51] [52] [58]	U.S. Cl	G11B 5/09 			
[56]		References Cited	bits of a th		
	U.S.	PATENT DOCUMENTS	same binary data word,		
	4,020,282 4/ 4,032,979 6/	1977 Halpern 360/40 X 1977 Rice 360/40	second and tively have		
	OT	HER PUBLICATIONS	fourth bits		
Hori	guchi et al.,	An Optimization of Modulation Codes	represents.		

Horiguchi et al., An Optimization of Modulation Codes in Digital Recording, IEEE Transactions on Magnetics, vol. MAG-12, No. 6, 11/1976, pp. 740-742.

]	Date of Patent:	Mar. 5, 198
]	Patent Number:	4,503,420

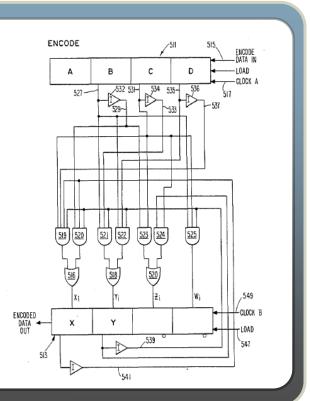
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Primary Examiner—T. J. Sloyan Attorney, Agent, or Firm—Vincenzo Pitruzzella; Albert Cefalo; Ronald Reiling

ABSTRACT

The present invention provides translation circuitry, which in one mode of operation acts to encode variable length data words into fixed rate data coded words for use with a communication channel, or a recording means, such as a magnetic recording medium and which in another mode of operation acts to decode the coded words to data words. The translation circuitry functions such that in an encoding operation, the second and third bits of a three-bit coded word respectively have the same binary values as the first and second bits of the data word, which the coded word represents and the second and sixth bits of a six-bit coded word respectively have the same binary values as the third and fourth bits of the data word which the coded word represents.

11 Claims, 10 Drawing Figures



1,7 RLL boosts density by 33%

• Deemed complex in 1982 \rightarrow 8 Flip-Flops, 10 gates



HISTORICAL PERSPECTIVE (3)

Constant Density Recording Boosts Capacity by 30% to 40%

- Electronic Design, November 13, 1986 (Mark Young):
- ...constant-density recording has been little used because of its high cost and the difficulty of putting it to work.
- Among those difficulties are the requirement for a phaselocked loop (PLL) capable of operating at any one of several different frequencies...



LESSONS LEARNED

 Not surprisingly, it didn't take long for 1,7 RLL Codes and Constant Density Recording to become widely adopted

• Lessons Learned:

- Tremendous innovation to store data more efficiently and increase storage density
- More efficient solutions usually prevail, even if they appear complex initially
- Complex today \rightarrow simple tomorrow



EARLY ADOPTION OF SLC MAKES SENSE

- SLC has been the media of choice for write intensive applications
- SLC spec advantages appear compelling:
 - x33 Endurance: 100K vs. 3K
 - x3 Program Speed: Tprog = 0.5ms vs. 1.5ms
- But history suggests that the denser solution will prevail
- How?



ANALYSIS OF WRITE CAPABILITY

- Drive Writes Per Day (DWPD)
 - Amount of writing that can be sustained over the entire product life
 - Normalized to Drive Capacity
 - Assume random writes uniformly distributed over entire logical address space. This is much more stringent than sequential writing
- Typical SSD specs:
 - SLC: 25 DPWD
 - MLC: <1 DWPD



DRIVE WRITES PER DAY



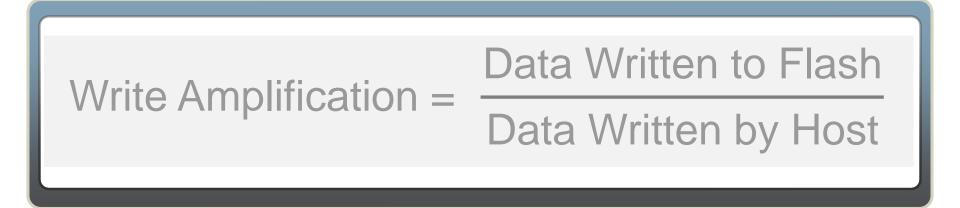
$OP = Overprovisioning = \frac{Physical Capacity}{Logical Capacity}$

WA = Write Amplification



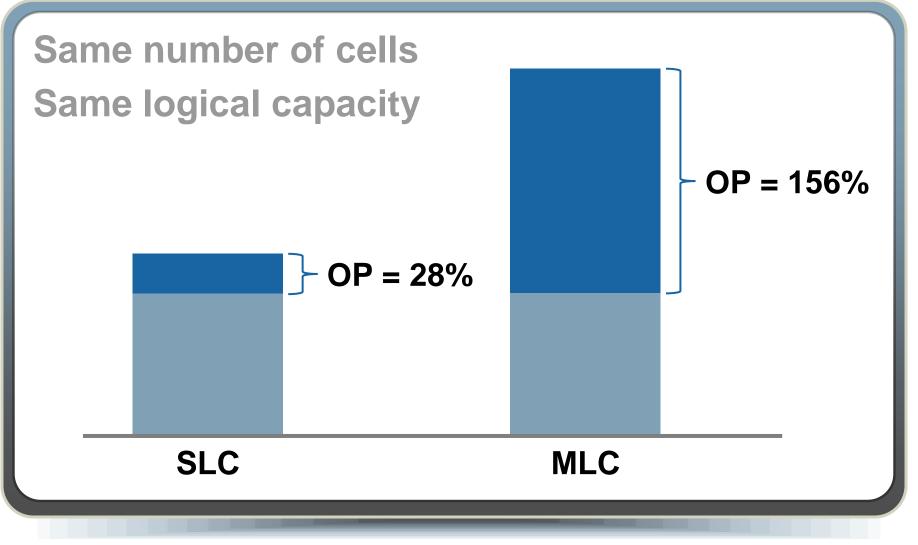
WRITE AMPLIFICATION

- Write Amplification is a measure of the extra writing required for garbage collection and other flash management functions
- Expressed as a ratio of the amount of data written to flash to the amount of data written by the host



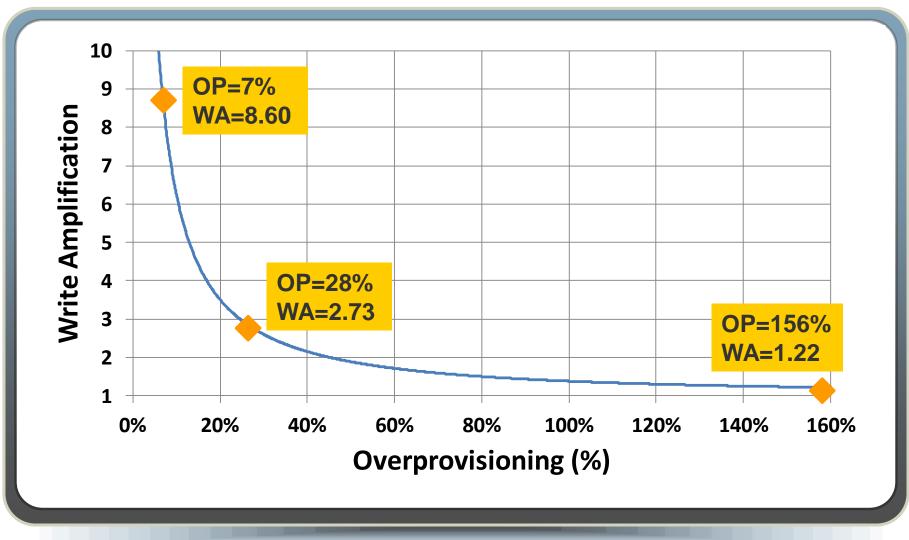


DENSITY ENABLES MUCH HIGHER OP





WRITE AMPLIFICATION VS. OP





COMBINED BENEFIT OF OP AND WA

DWPD = -		+ OP) WA			
	SLC	,	MLC		
1+OP	1.28		2.56		
WA	2.73		1.22		
(1+OP) / WA	0.47		2.10		
X 4.5					

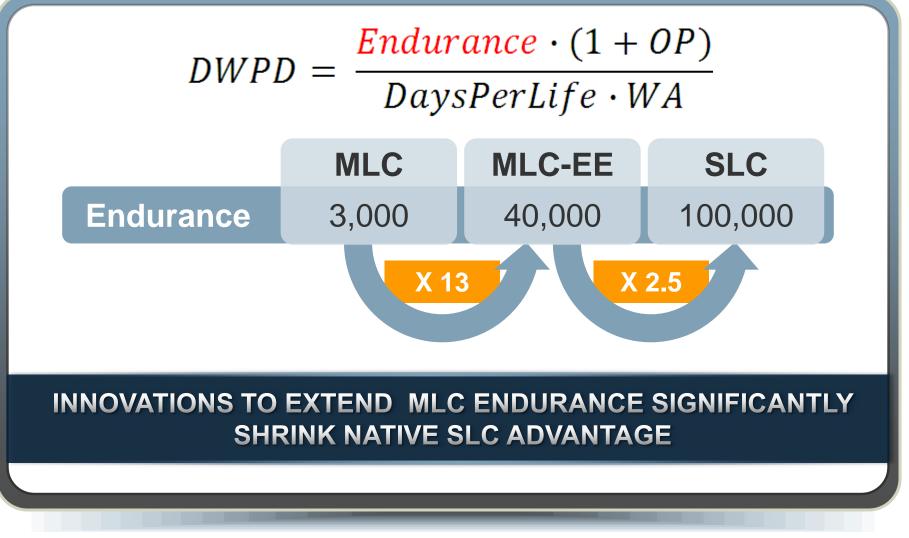


MLC ENDURANCE ENHANCEMENTS

- The gains from Overprovisioning and Write Amplification are not sufficient to bridge the gap between SLC and MLC
- However, the advent of technology to extend the endurance of MLC is a game changer
- For example, technology that won the "Best-of-Show" award at FMS 2011 for extending the endurance of MLC from 3K to 40K PE cycles
- We refer to Endurance Enhanced MLC as MLC-EE

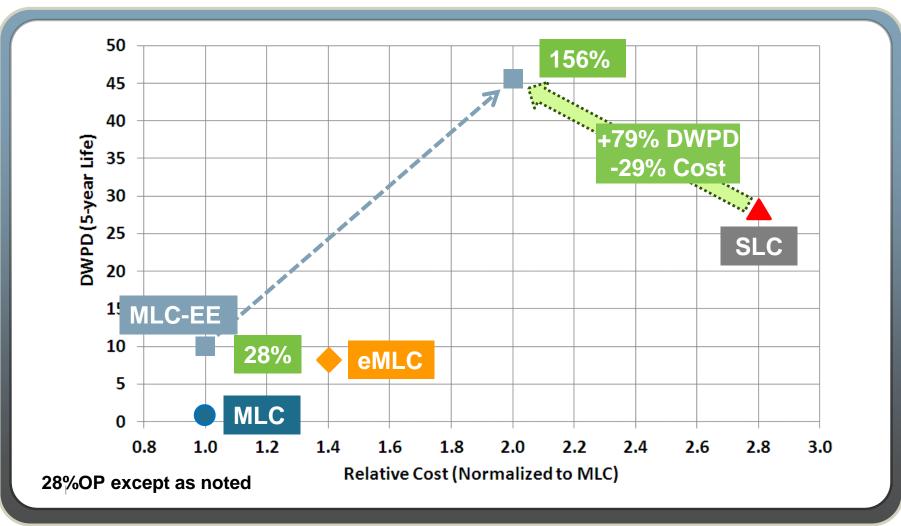


BENEFIT OF MLC ENDURANCE ENHANCEMENT TECHNOLOGY





CHANGING LANDSCAPE





IT'S NOT ALL ABOUT DENSITY!

• It's the density, stupid!

And endurance enhancements too!



MLC DELIVERS ONE-TWO PUNCH







29% Cost Savings

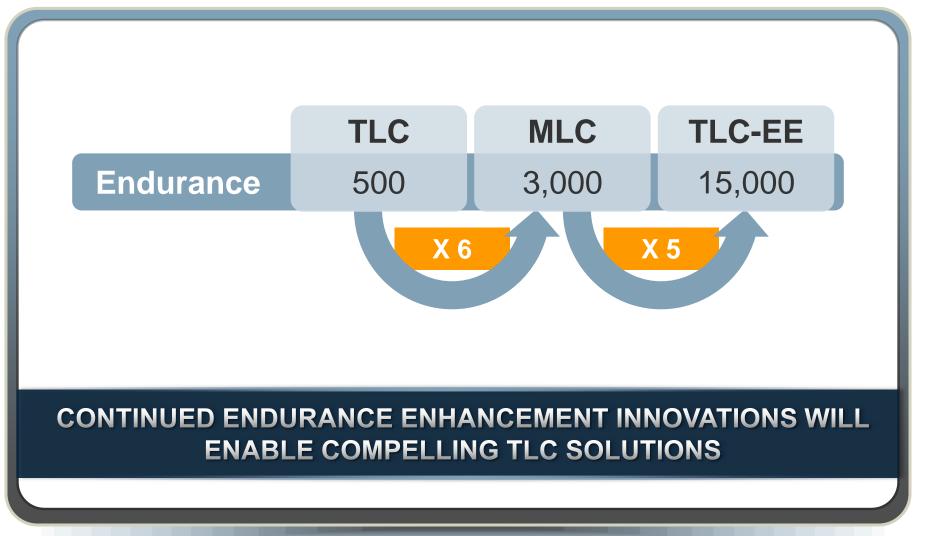


WHAT'S NEXT?

- Continued innovation will push endurance enhancements even higher
- Line of sight for additional factor of 2-3 resulting in endurance gains 25x to 40x
- Opportunities to migrate to denser solutions
- TLC?
- Likely to displace MLC in entry level applications

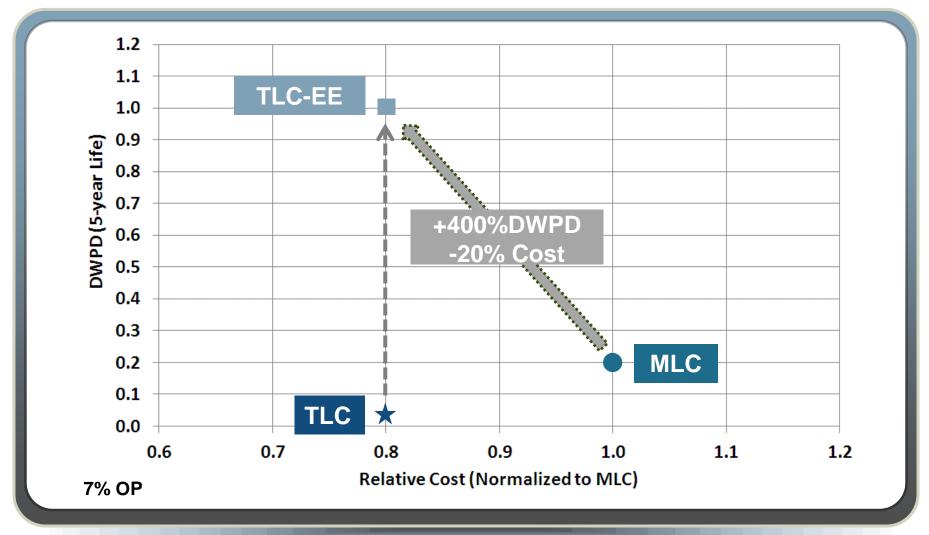


EVOLUTION OF ENTRY LEVEL SSDS



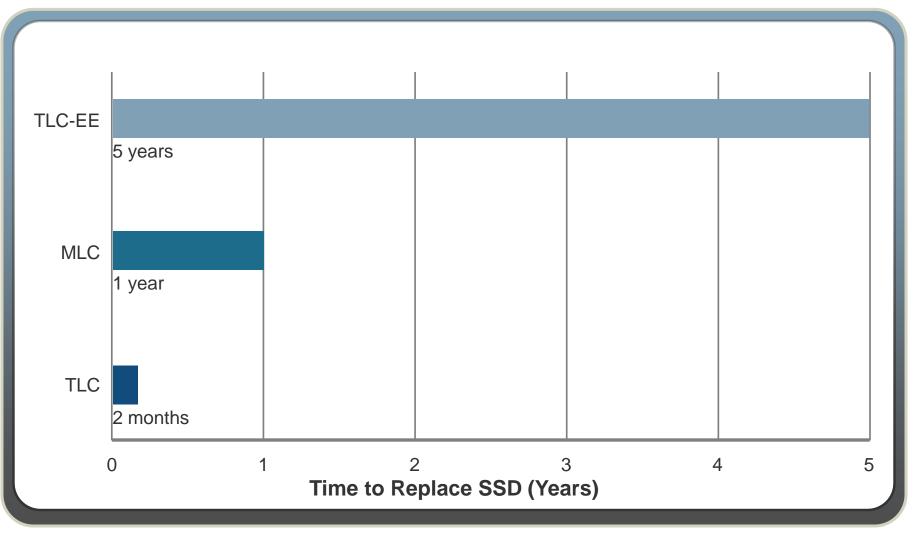


ENTRY LEVEL PRODUCTS MOSTLY READ WORKLOADS





CONSUMPTION MODEL TIME TO REPLACE SSD @ 1.0 DWPD





SUMMARY

- SLC is no longer the best solution for write intensive SSDs
- Compelling MLC advantage when combining endurance enhancements and higher overprovisioning
 - +79% Drive Writes per Day
 - -29% Cost
- Future endurance enhancements will enable TLC products vastly superior to today's MLC-based value SSDs

THANK YOU



Making NAND Better