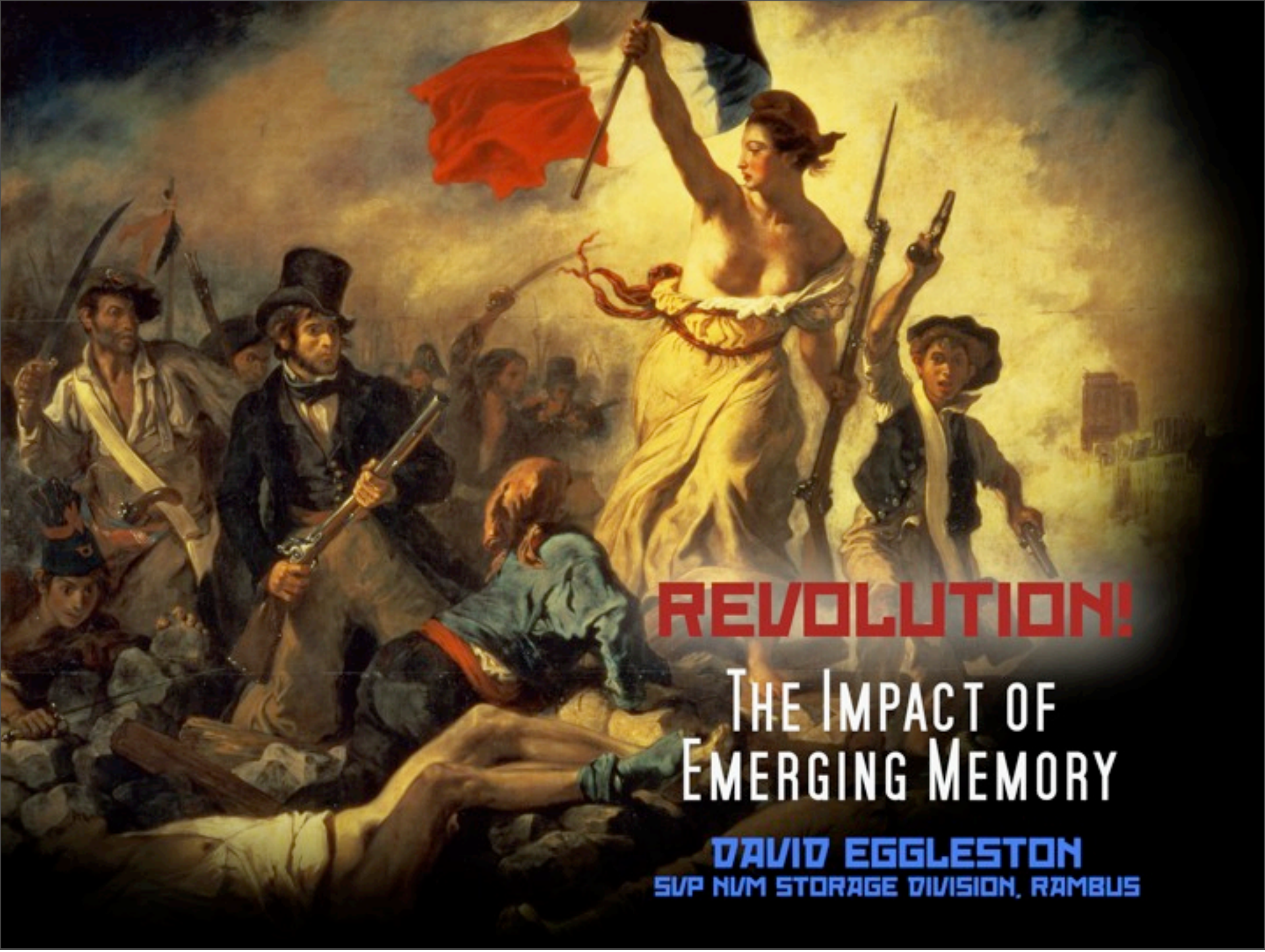
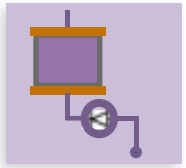

REVOLUTION!
THE IMPACT OF
EMERGING MEMORY
DAVID EGGLESTON
SVP NVM STORAGE DIVISION, RAMBUS

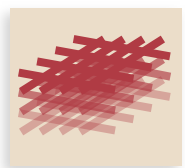
The Opportunity

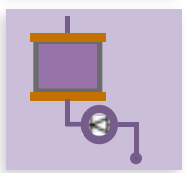
The Opportunity

The Opportunity



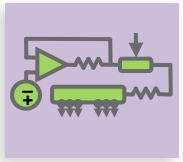
NVM Bitcell

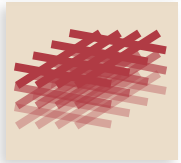


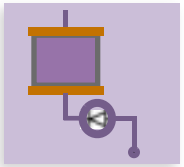


Design & Architecture

NVM Bitcell



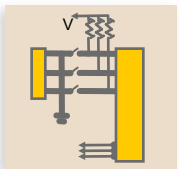


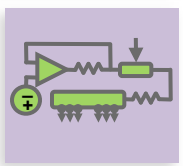


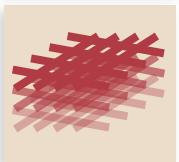
NVM Interface

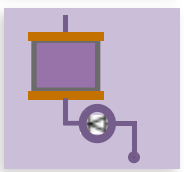
Design & Architecture

NVM Bitcell







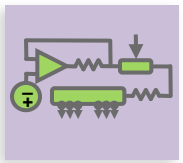


NVM Handling

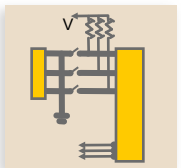
NVM Interface

Design & Architecture

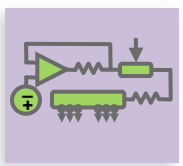
NVM Bitcell



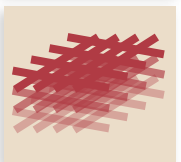
Storage Interface



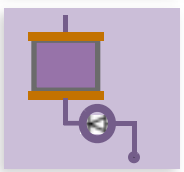
NVM Handling



NVM Interface

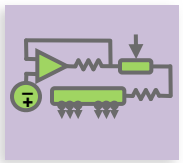


Design & Architecture

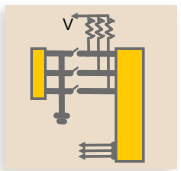


NVM Bitcell

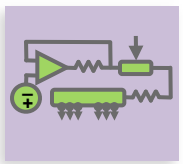
Virtualization



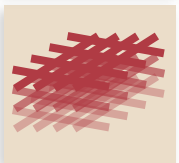
Storage Interface



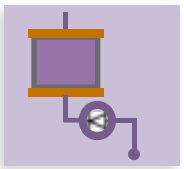
NVM Handling



NVM Interface

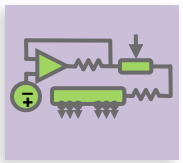


Design & Architecture

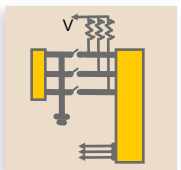


NVM Bitcell

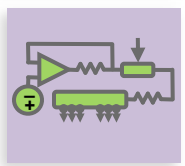
Virtualization



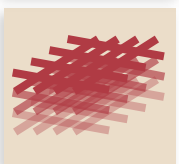
Storage Interface



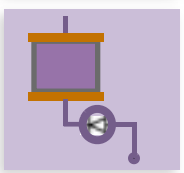
NVM Handling



NVM Interface



Design & Architecture



NVM Bitcell

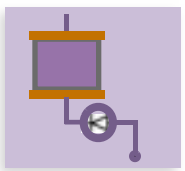
Storage Interface

NVM Handling

NVM Interface

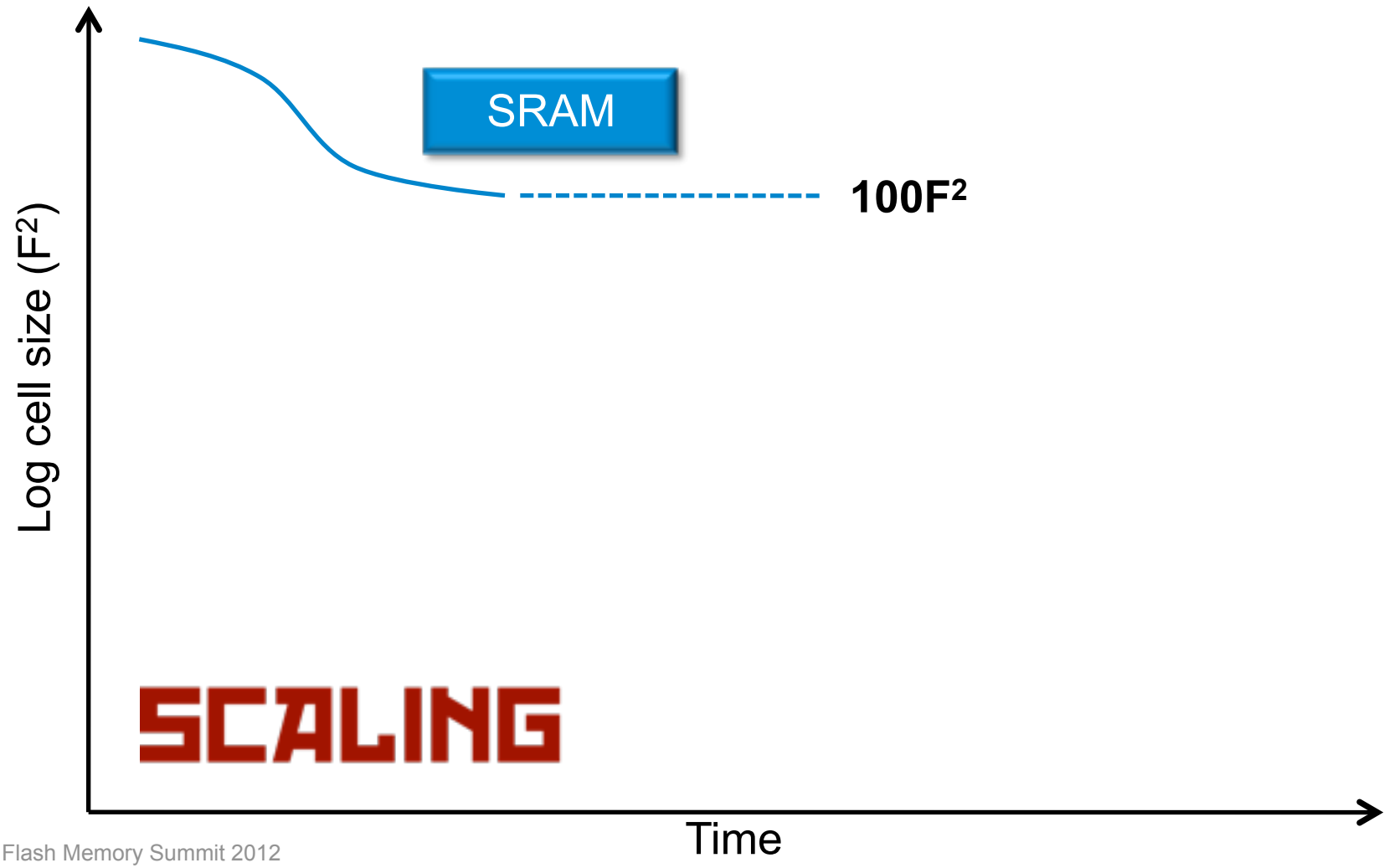
Design & Architecture

NVM Bitcell



Memory Bitcell

Memory Bitcell



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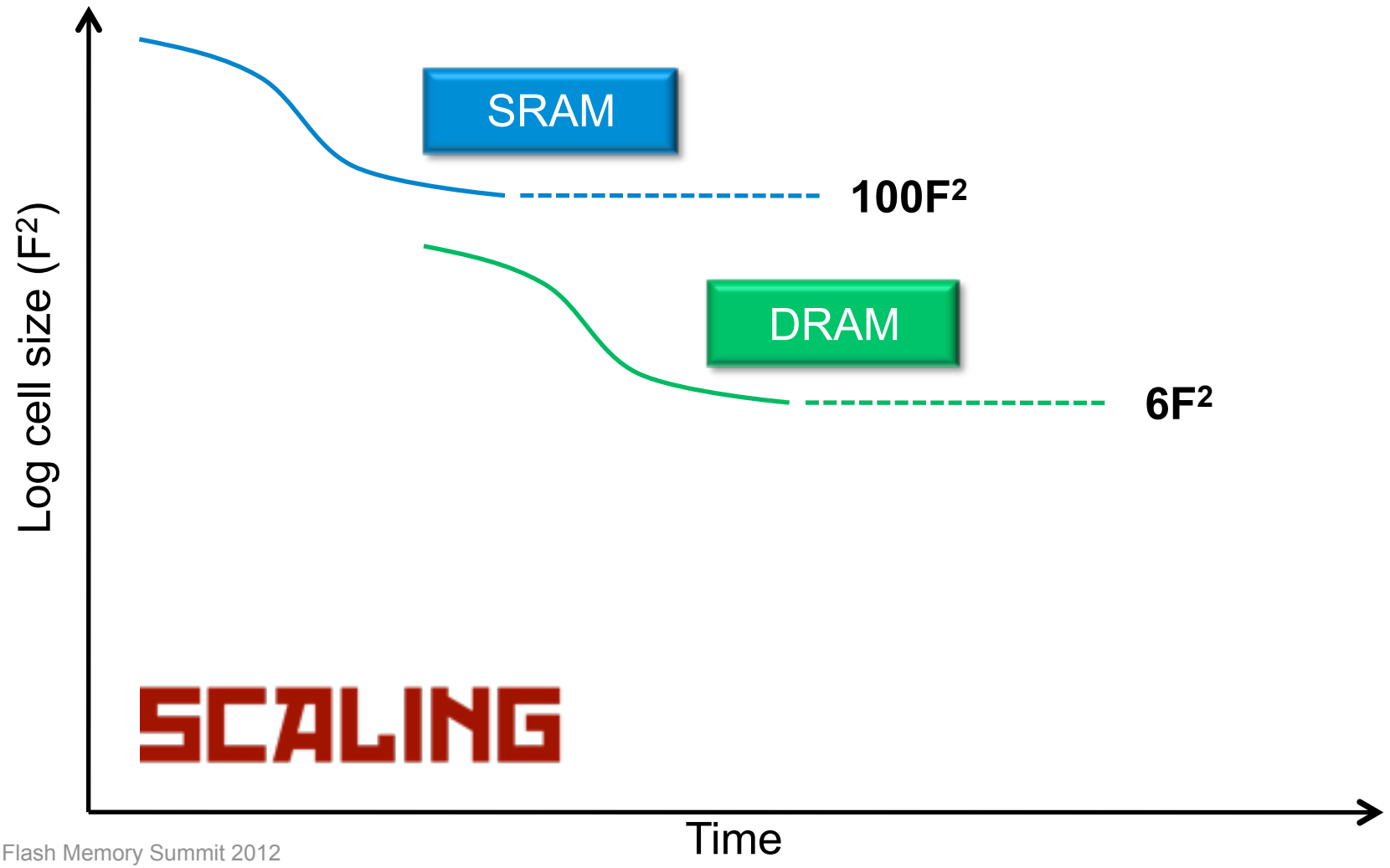
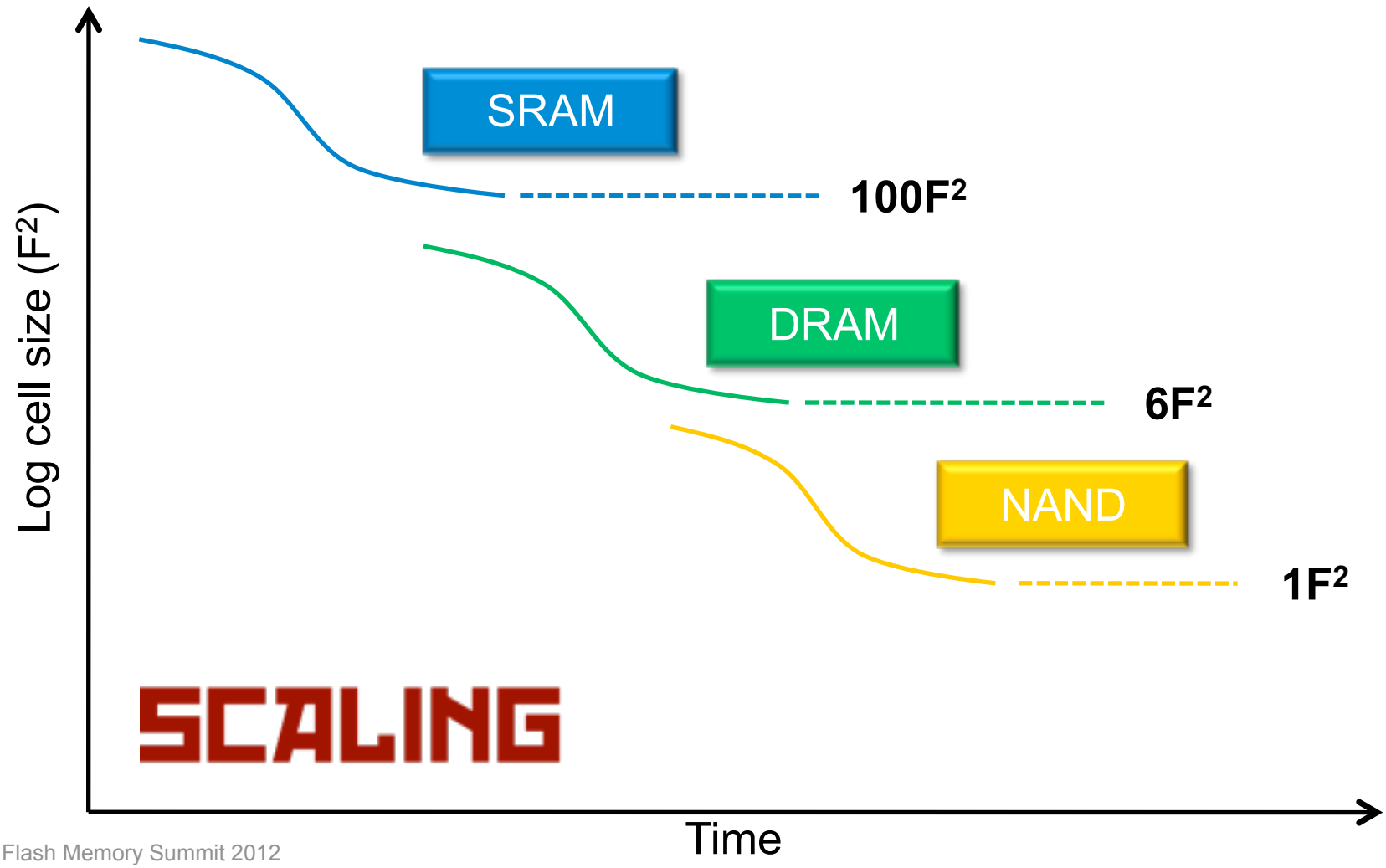
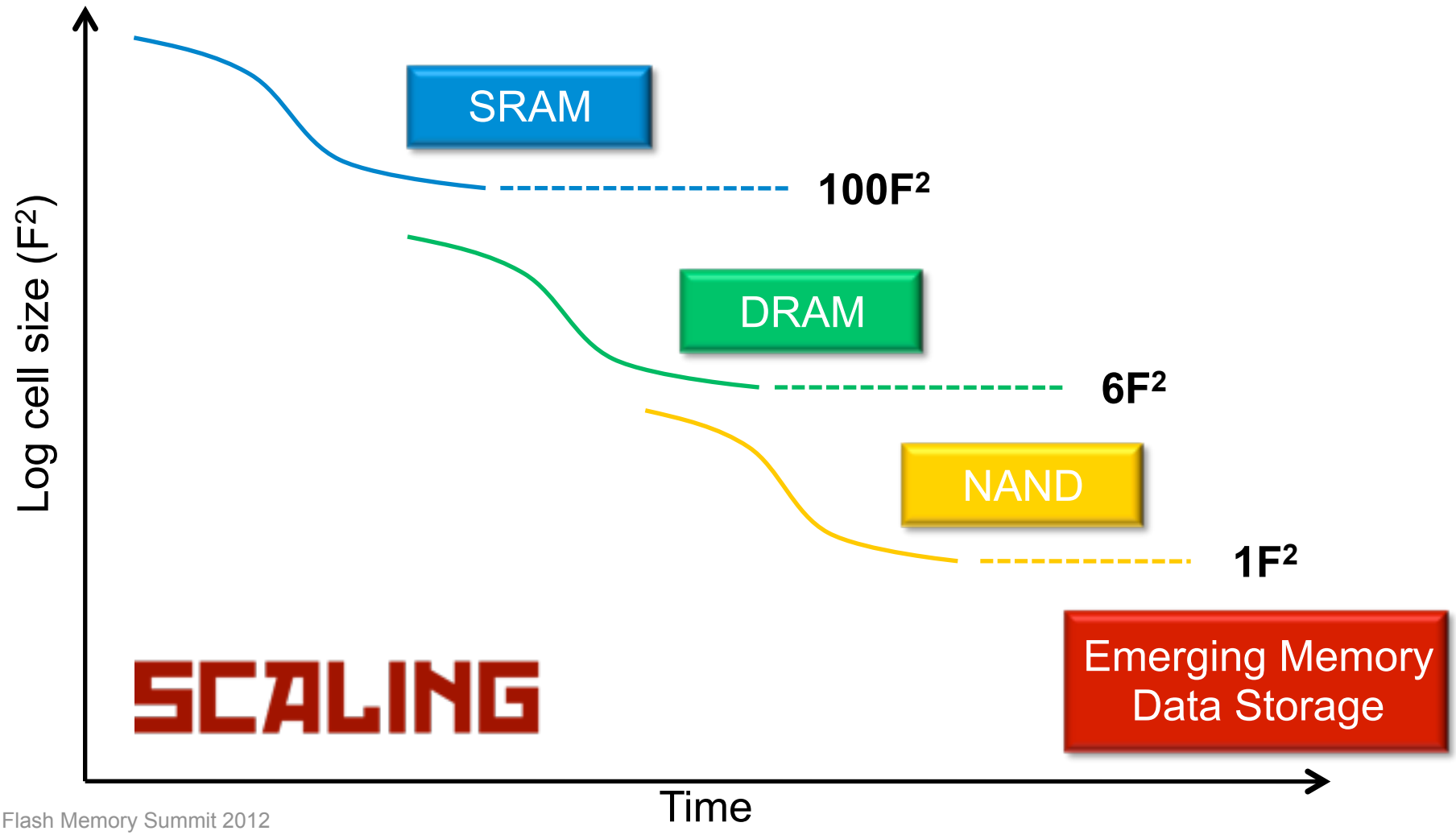


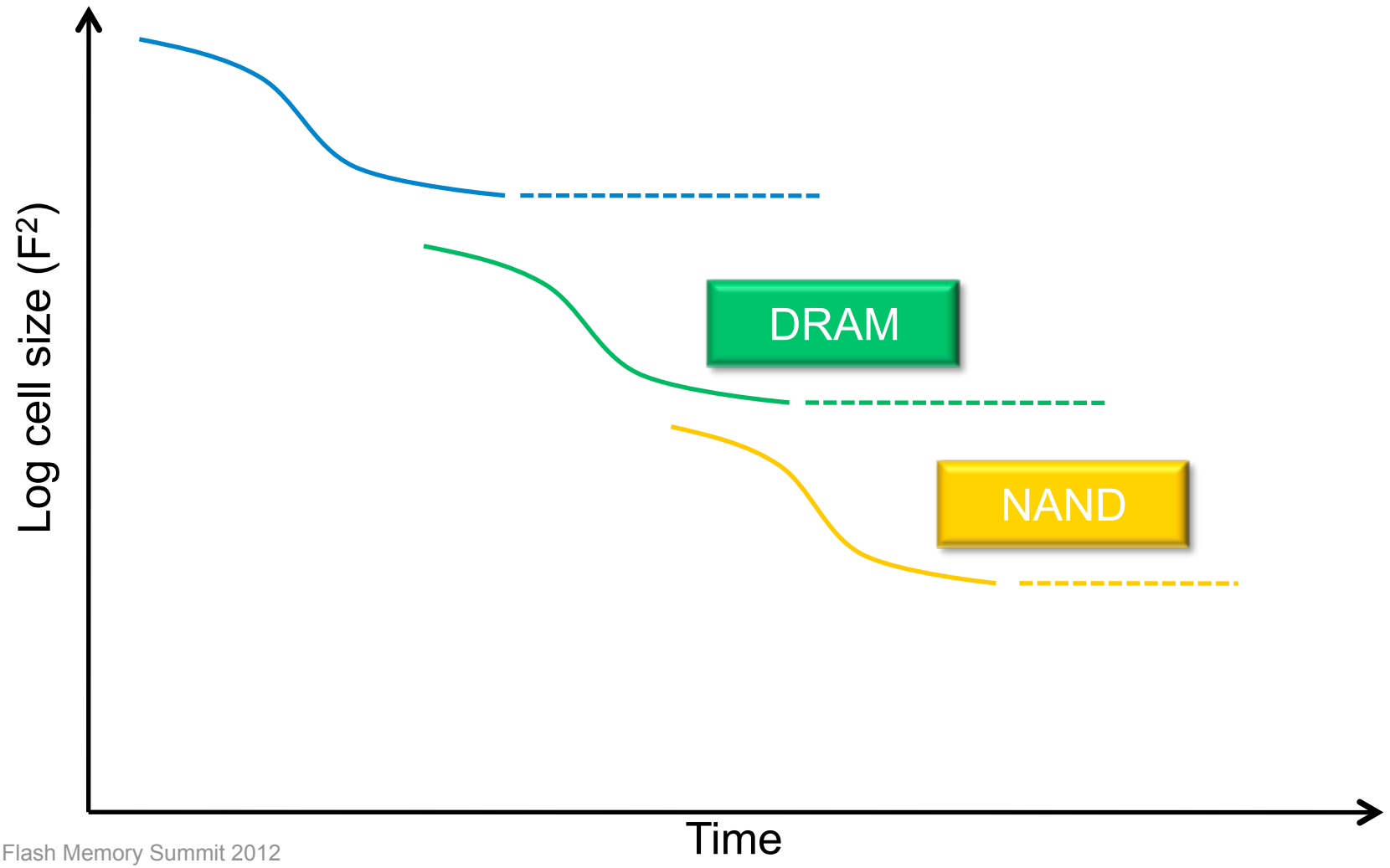
Memory Bitcell



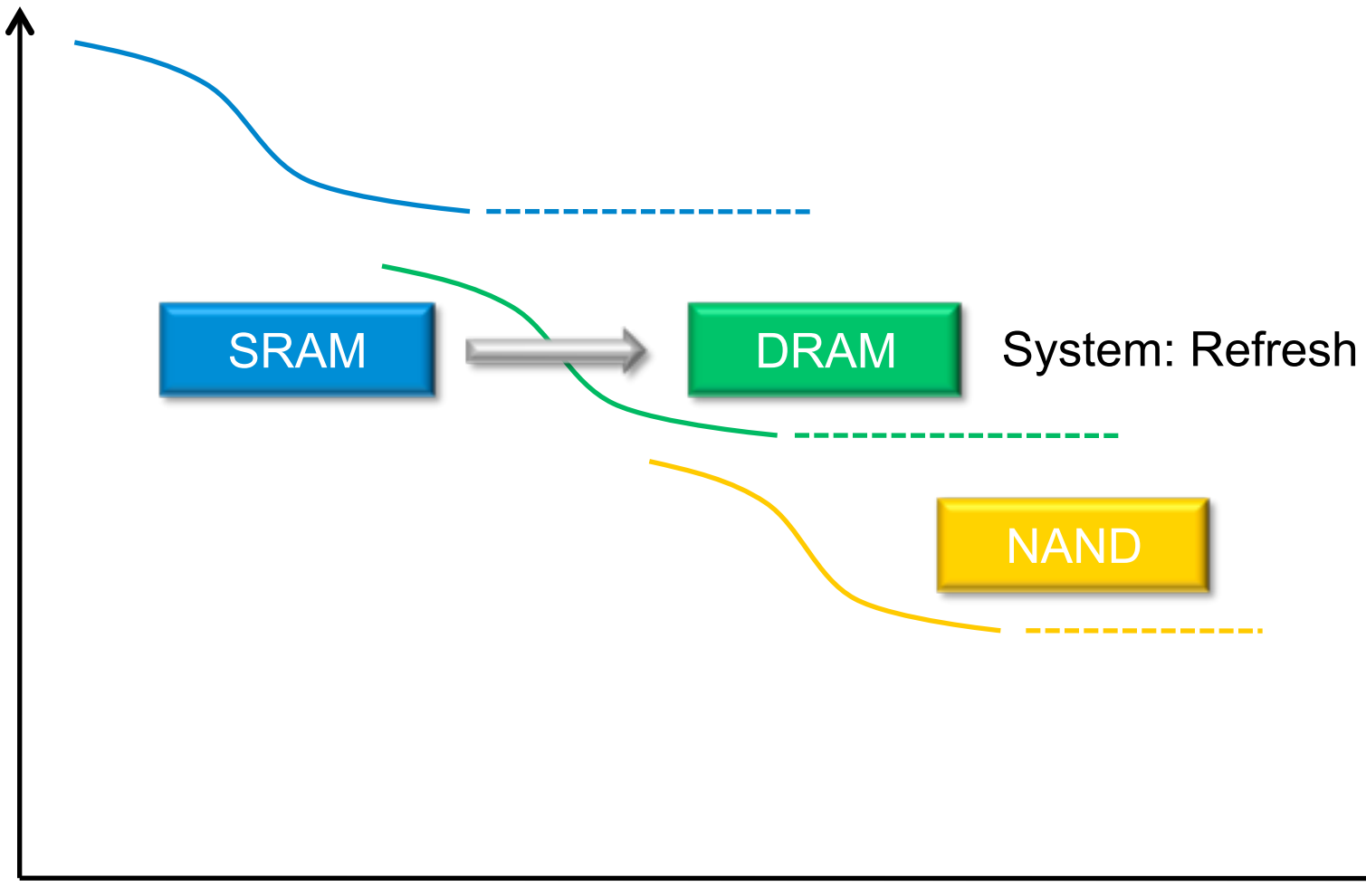
Memory Bitcell



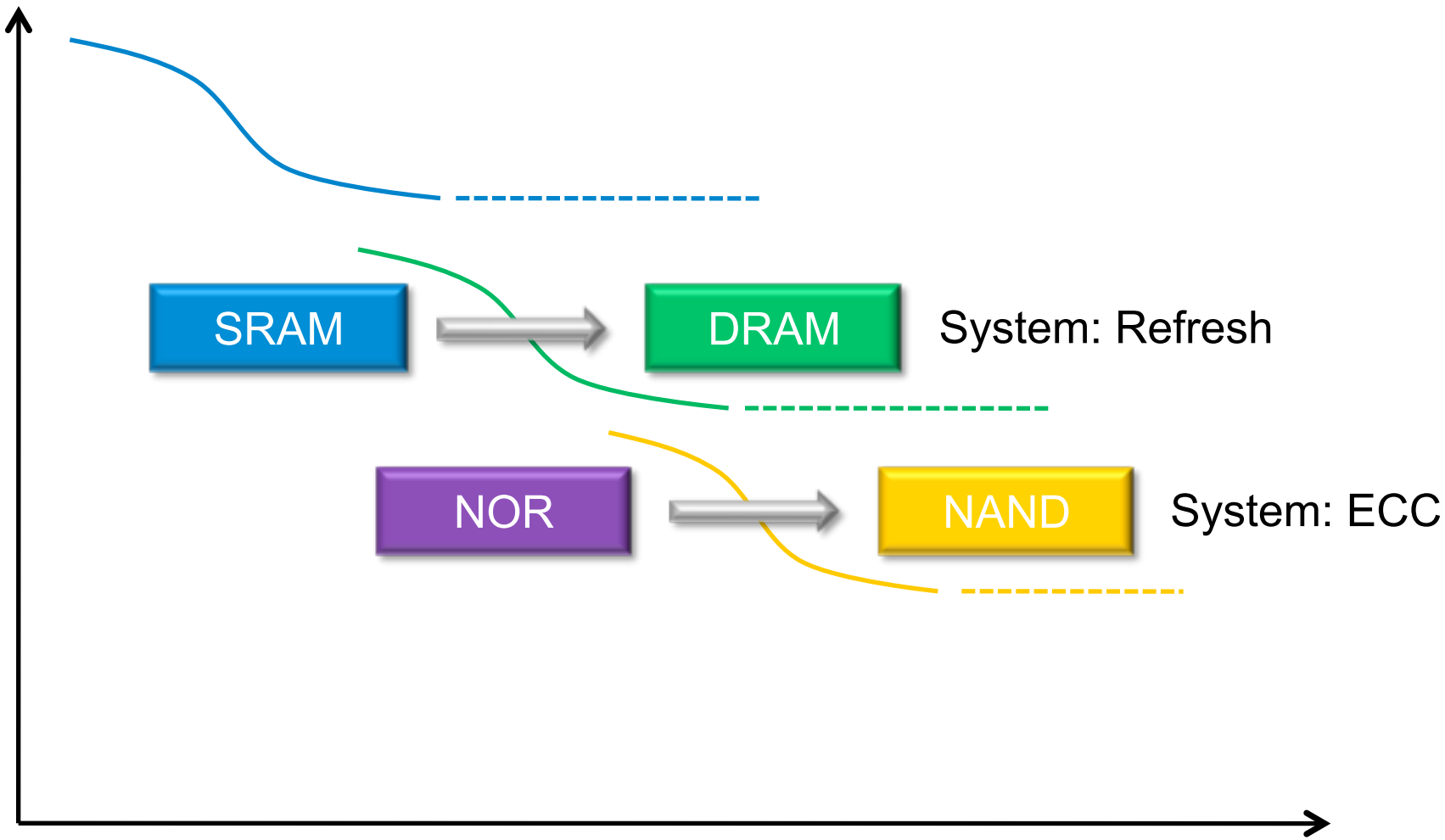
Memory Bitcell: System



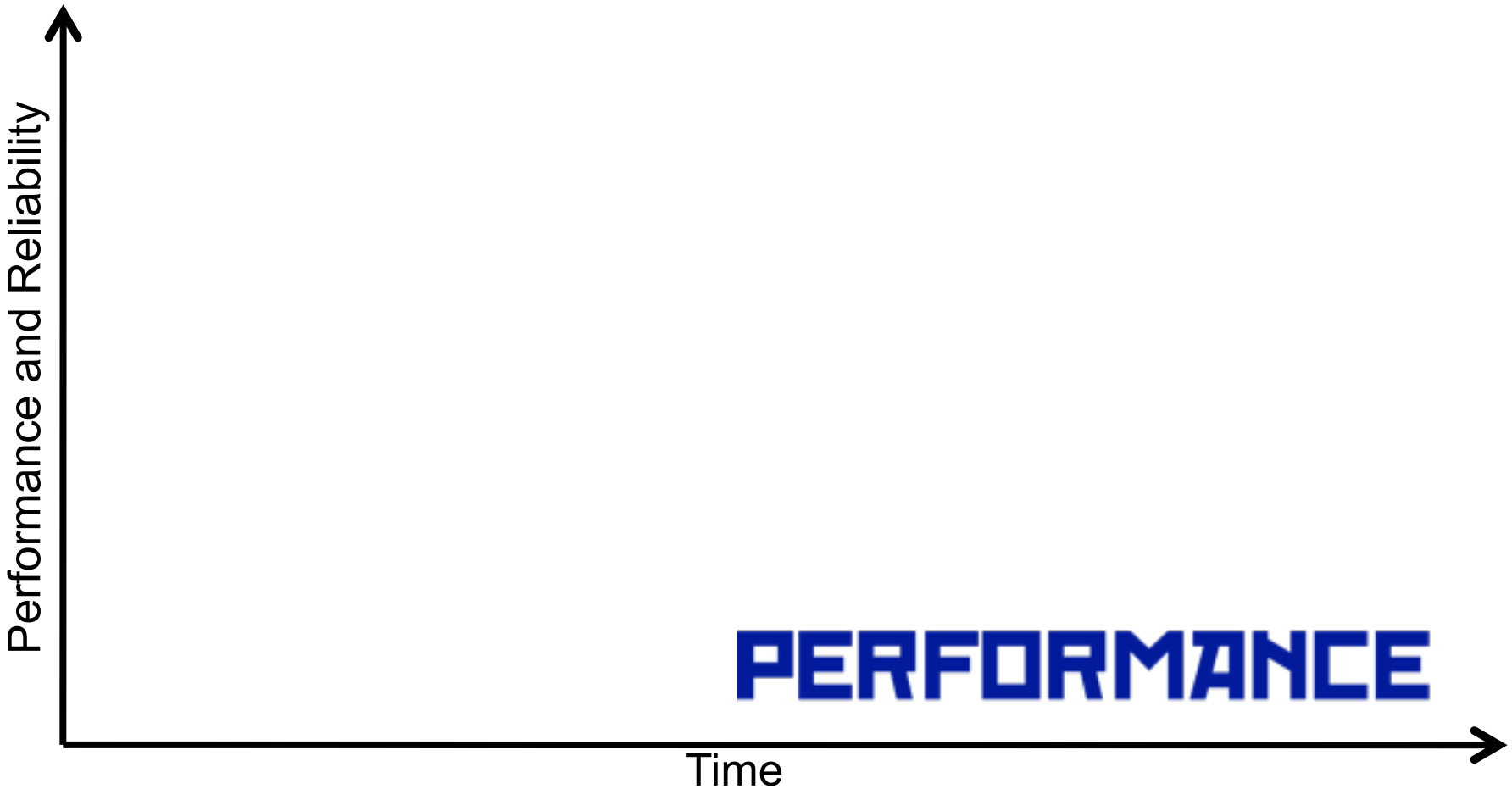
Memory Bitcell: System



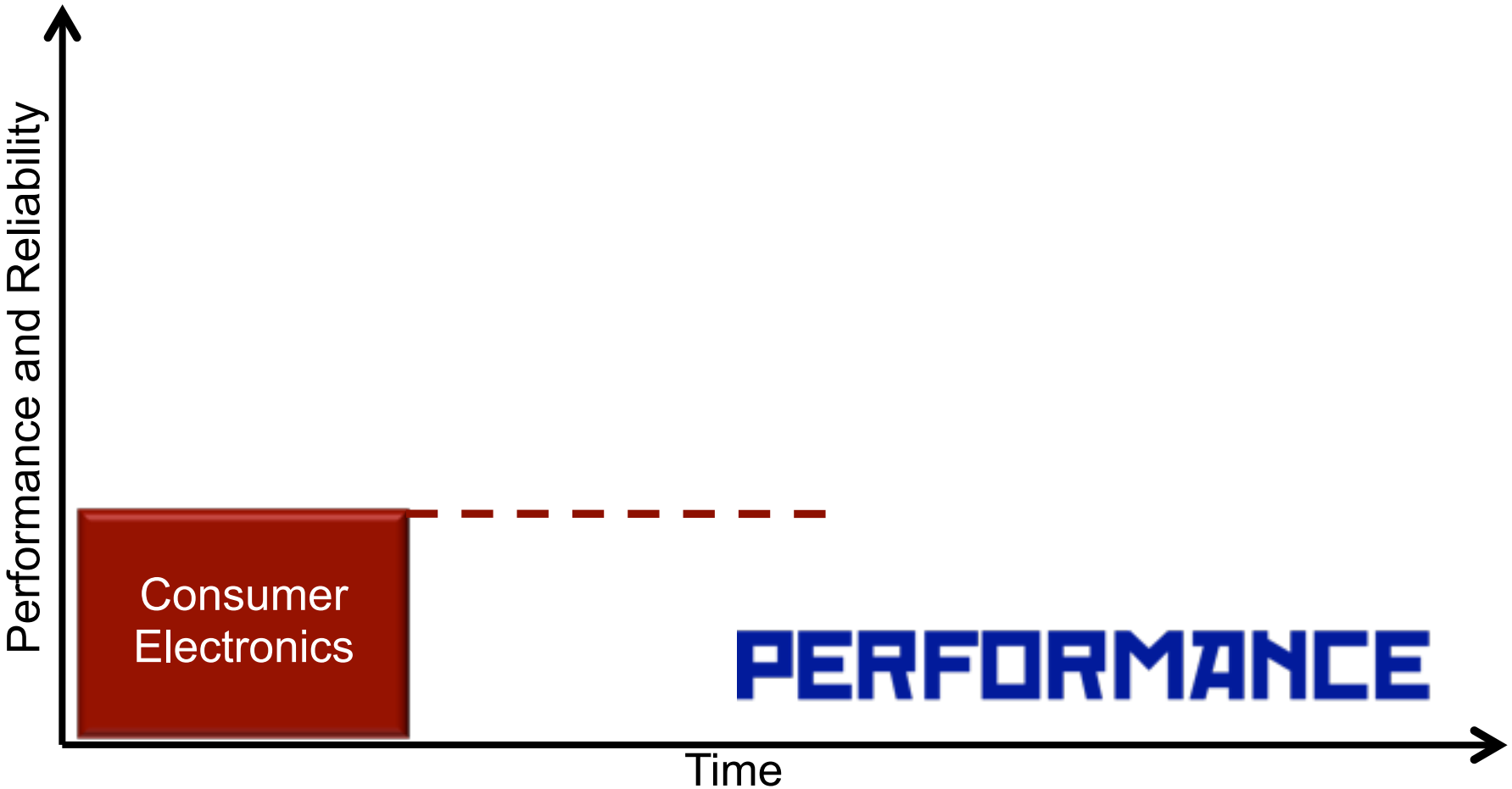
Memory Bitcell: System



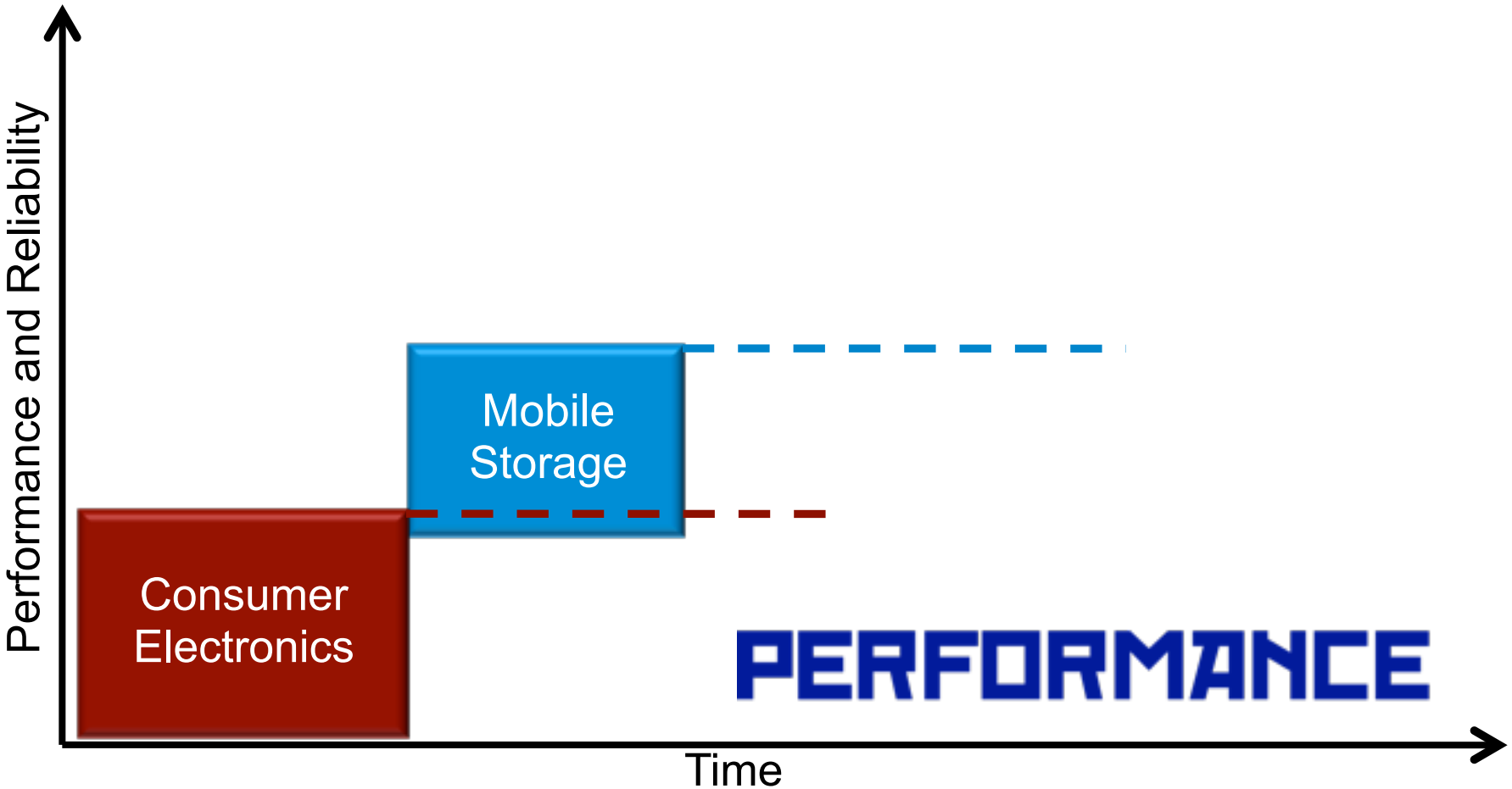
NAND Bitcell vs. Requirements



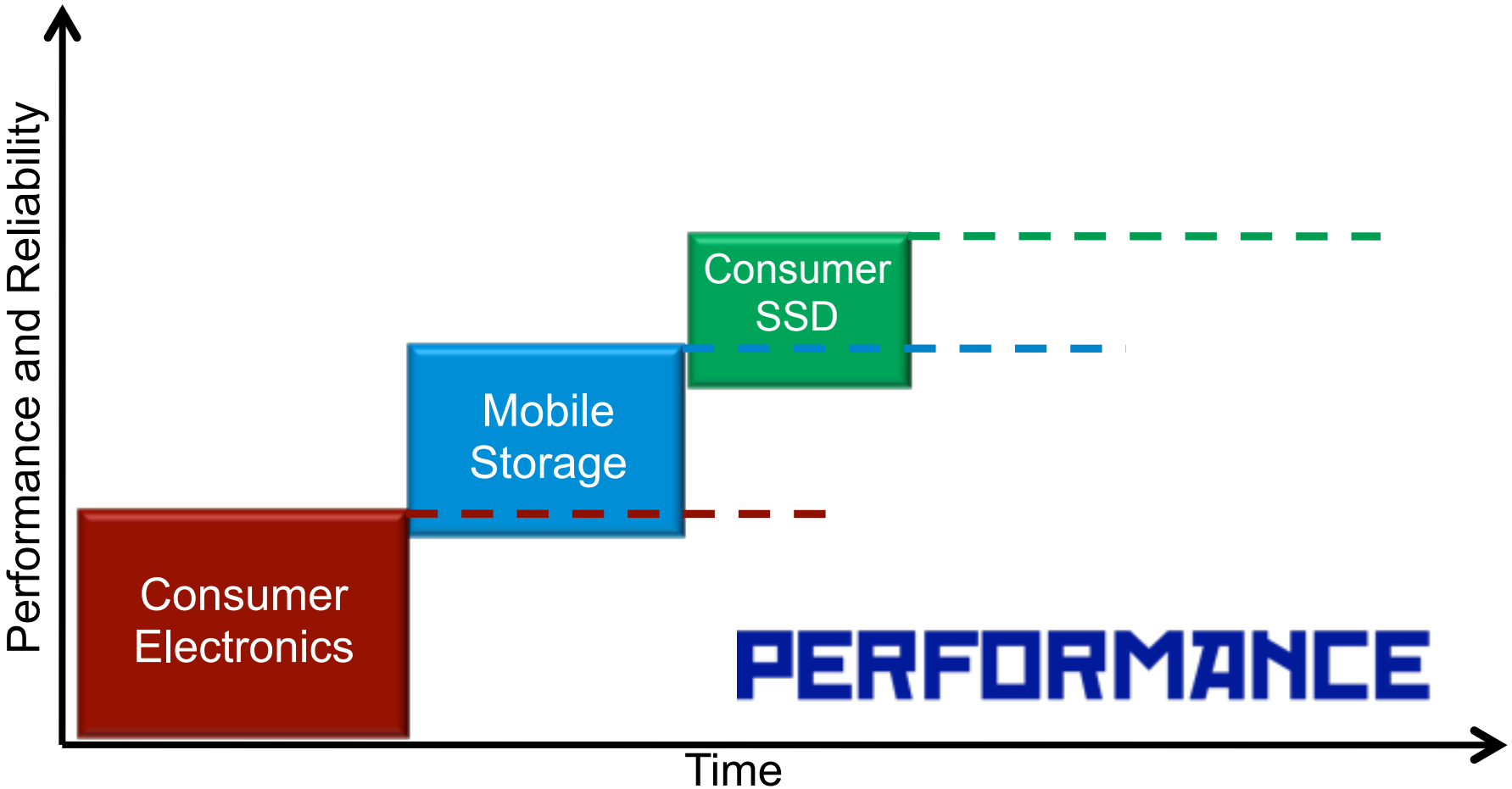
NAND Bitcell vs. Requirements



NAND Bitcell vs. Requirements



NAND Bitcell vs. Requirements



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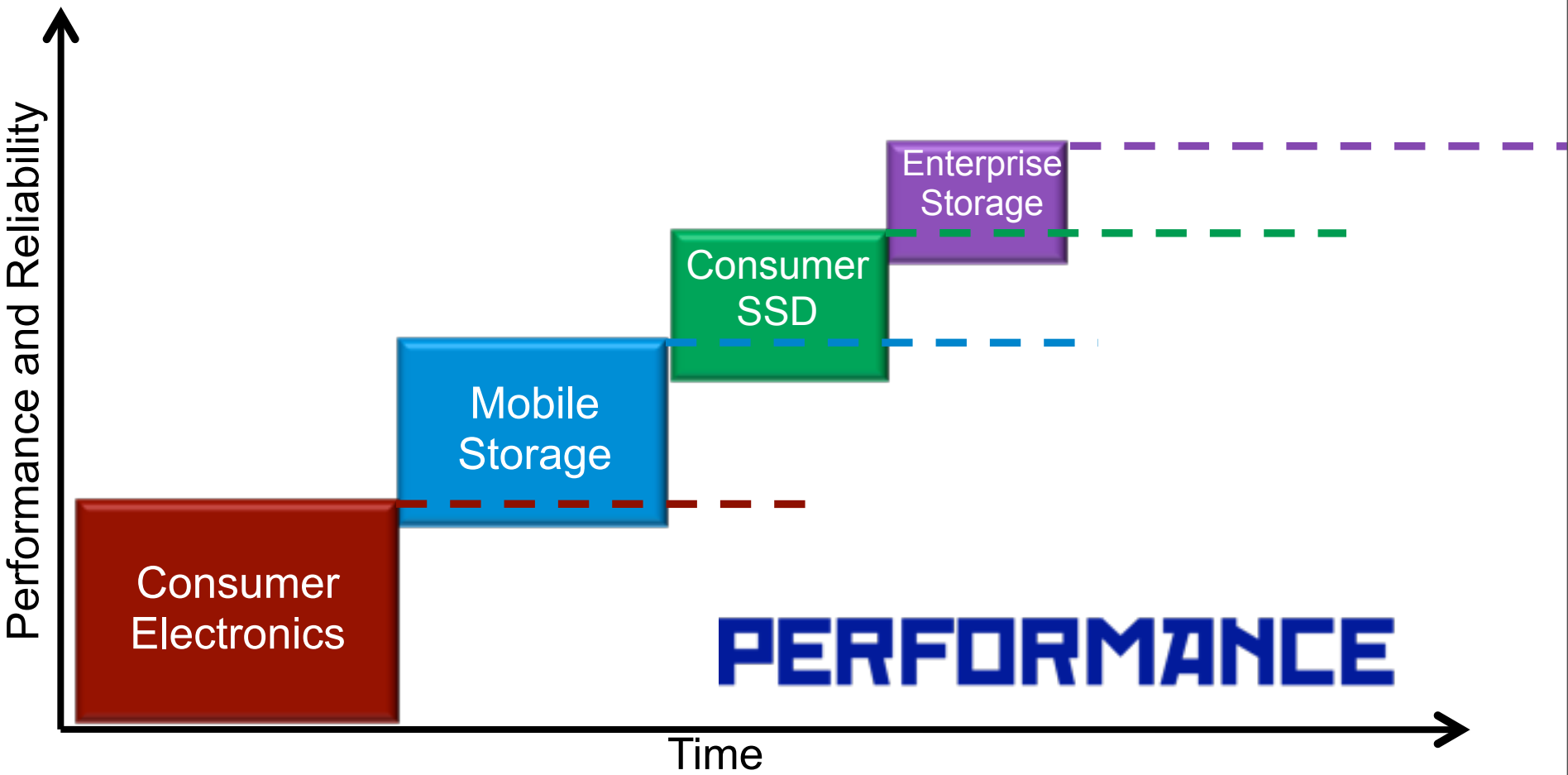

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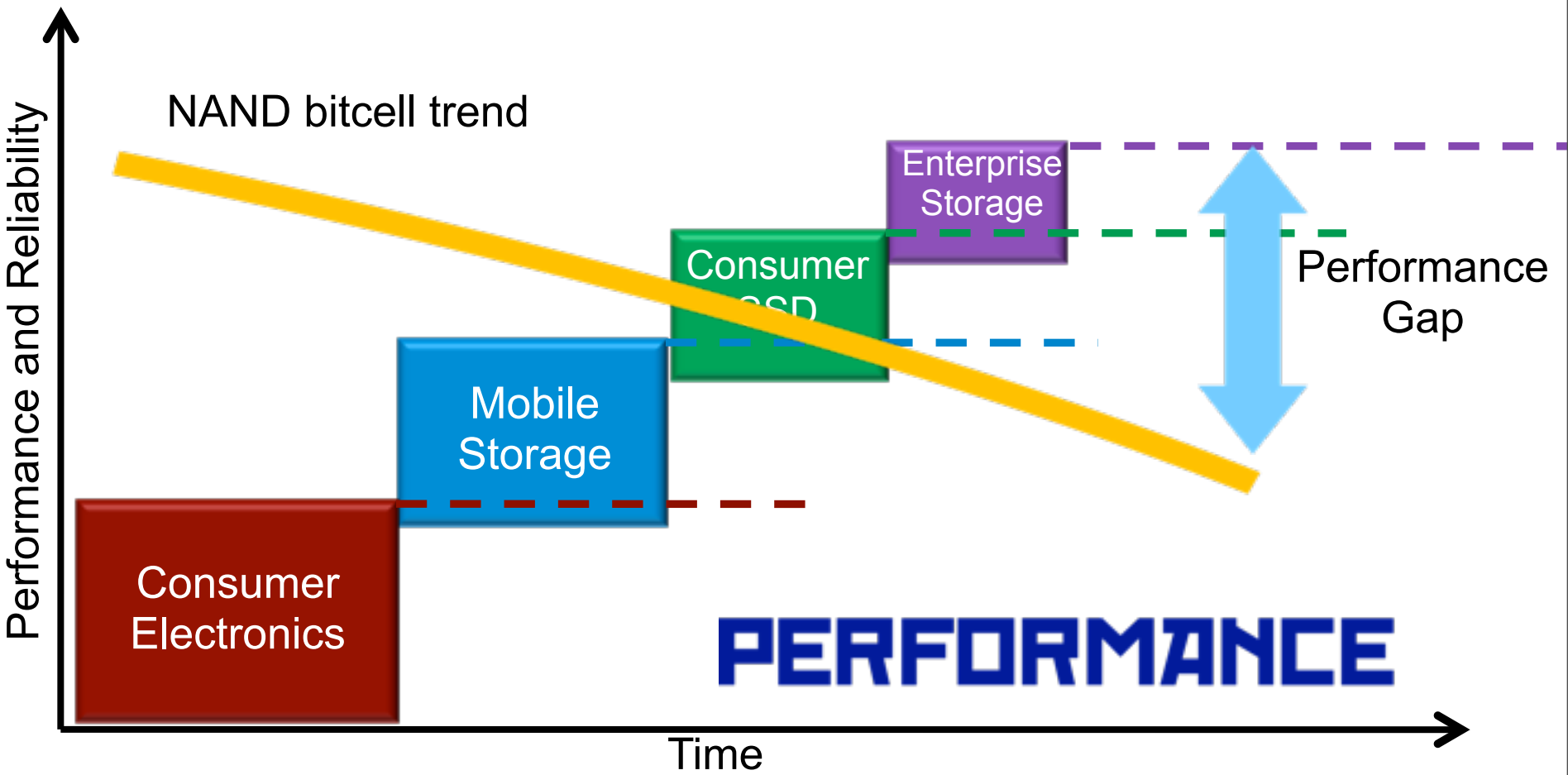
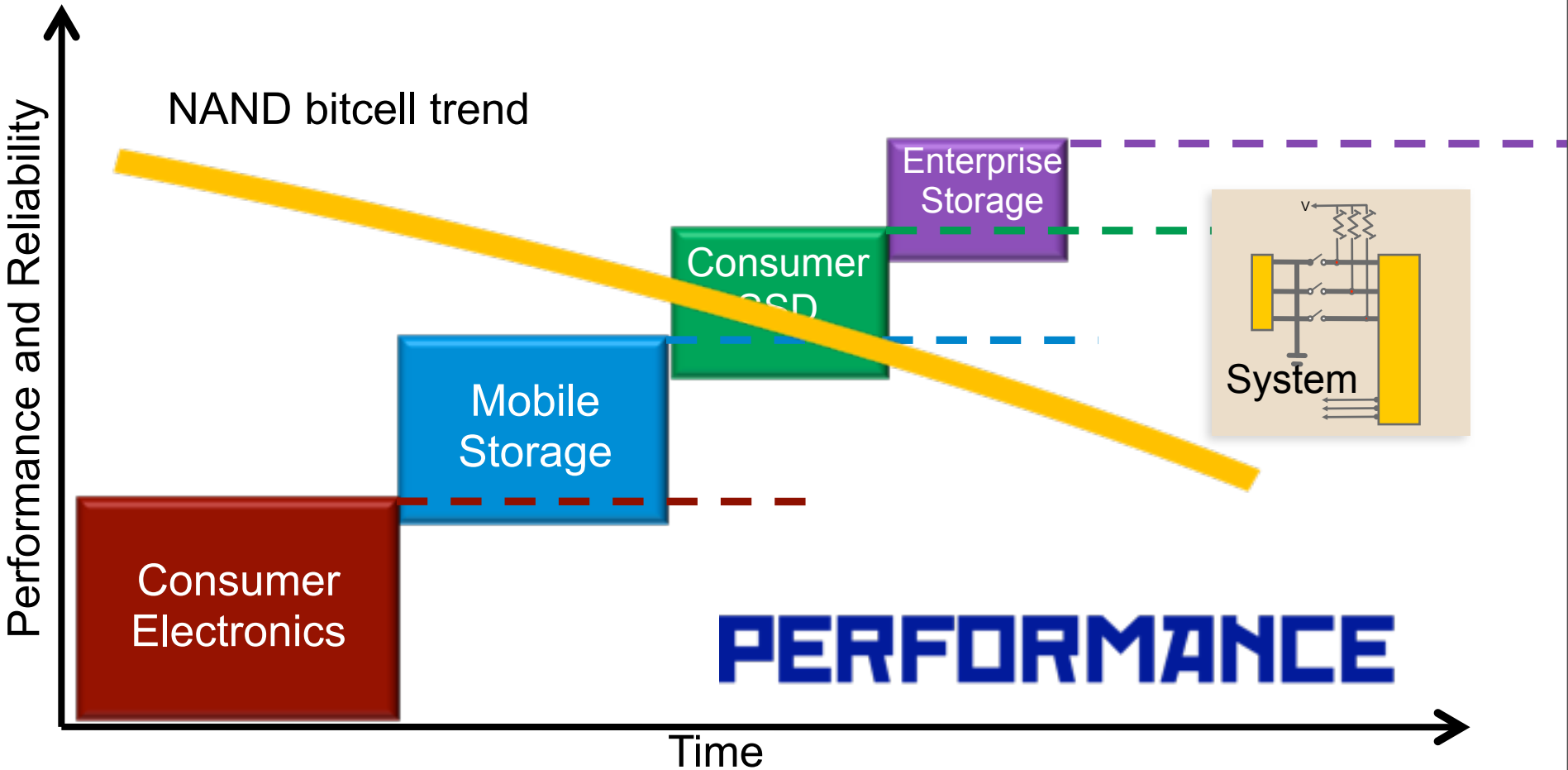


NAND Bitcell vs. Requirements



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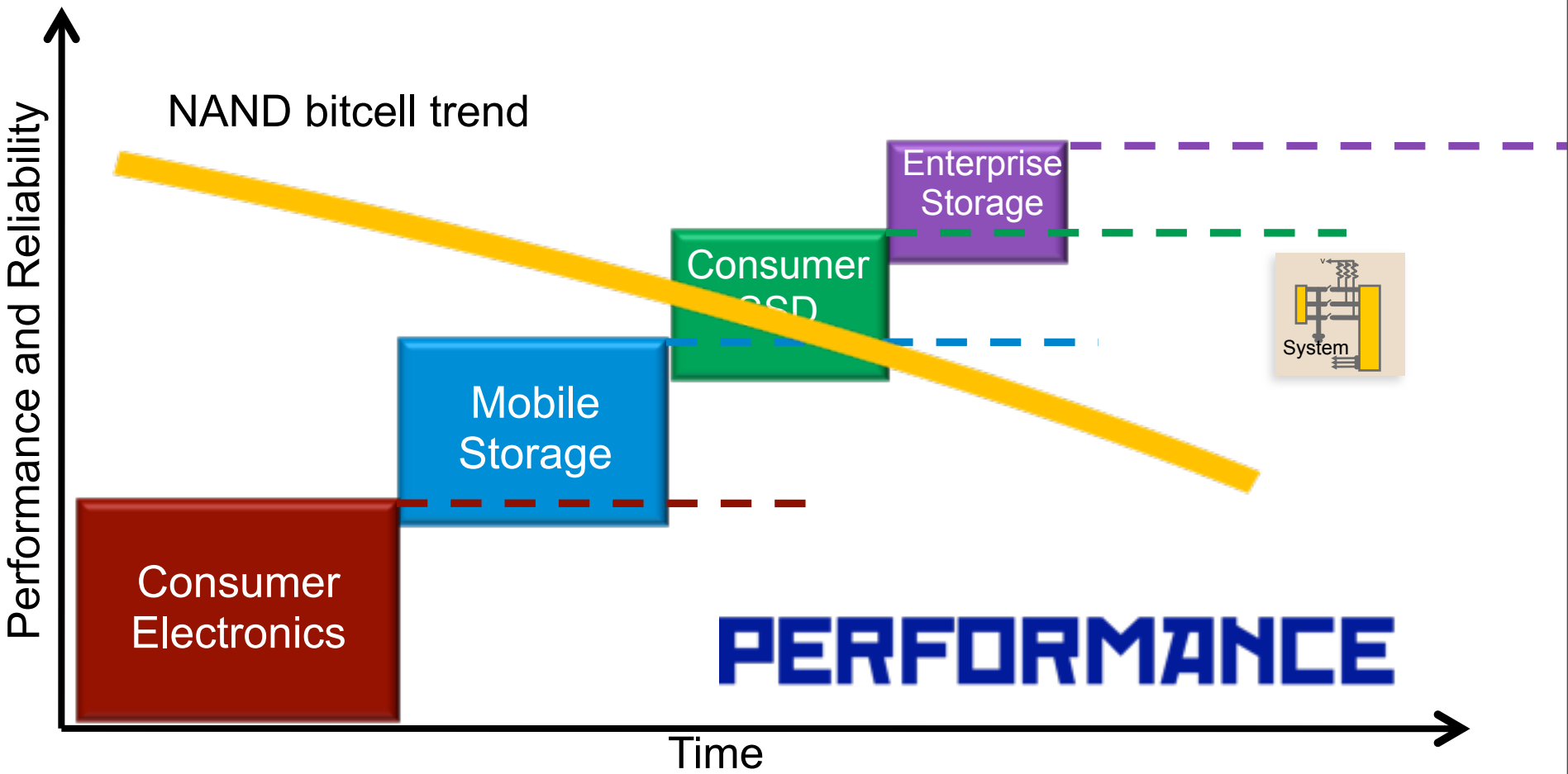

Key Criteria for Emerging Memory

Key Criteria for Emerging Memory

SCALING

Key Criteria for Emerging Memory

SCALING

PERFORMANCE

Contenders

Main Memory

DRAM

STT-RAM

$6F^2$

Fast

CB-RAM

PCRAM

Data Storage

Memristor

NAND

RRAM

$1F^2$

Slow

Contenders

Main Memory

DRAM

STT-RAM

$6F^2$

Fast

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Contenders

Main Memory

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$6F^2$

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$1F^2$

Slow

Contenders

	STT-RAM	PCRAM	RRAM	NAND
Memory Cell (F^2)	$30F^2 \rightarrow 6F^2$	$10F^2 \rightarrow 5F^2$	$20F^2 \rightarrow 0.25F^2$	$4.5F^2 \rightarrow 1F^2$
Cell type	1T-1R	1T-1R 1D-1R	1T-1R 1D-1R **1R**	1T-FG
Write Speed (Bit level)	1's ns	10's ns	10's ns ~ 100's ns	10,000 ns
Application	Embedded Main memory	Code storage NV cache	**Data storage** NV cache Embedded	**Data storage**

Contenders

	STT-RAM	PCRAM	RRAM	NAND
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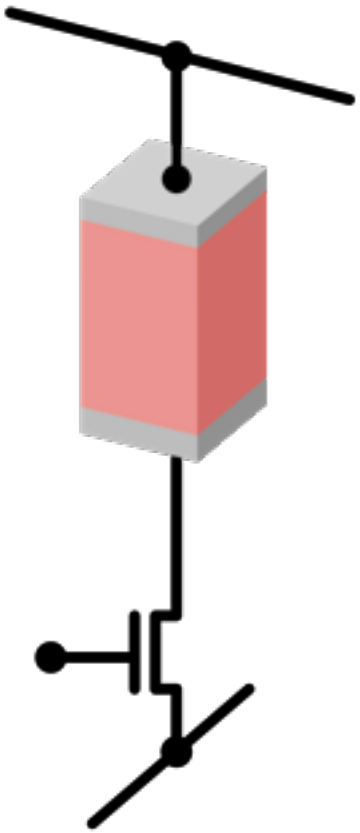
Bitcell Selection

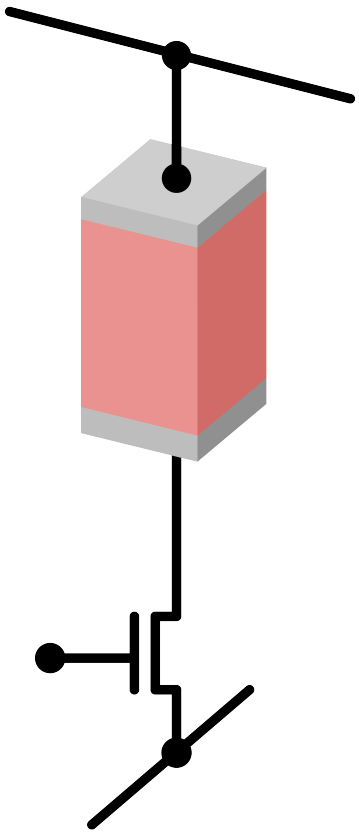


1T-1R

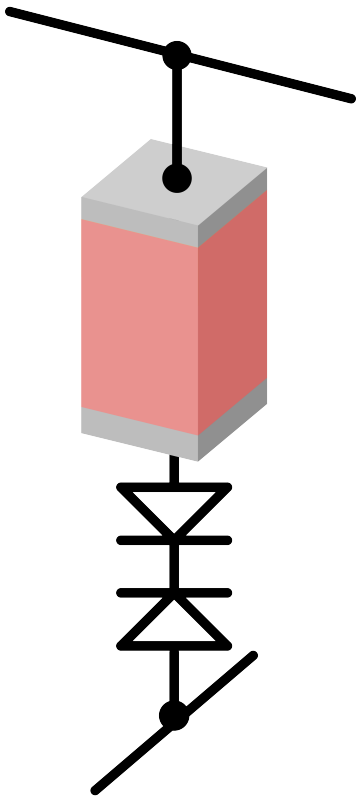
1D-1R

1R

Bitcell Selection



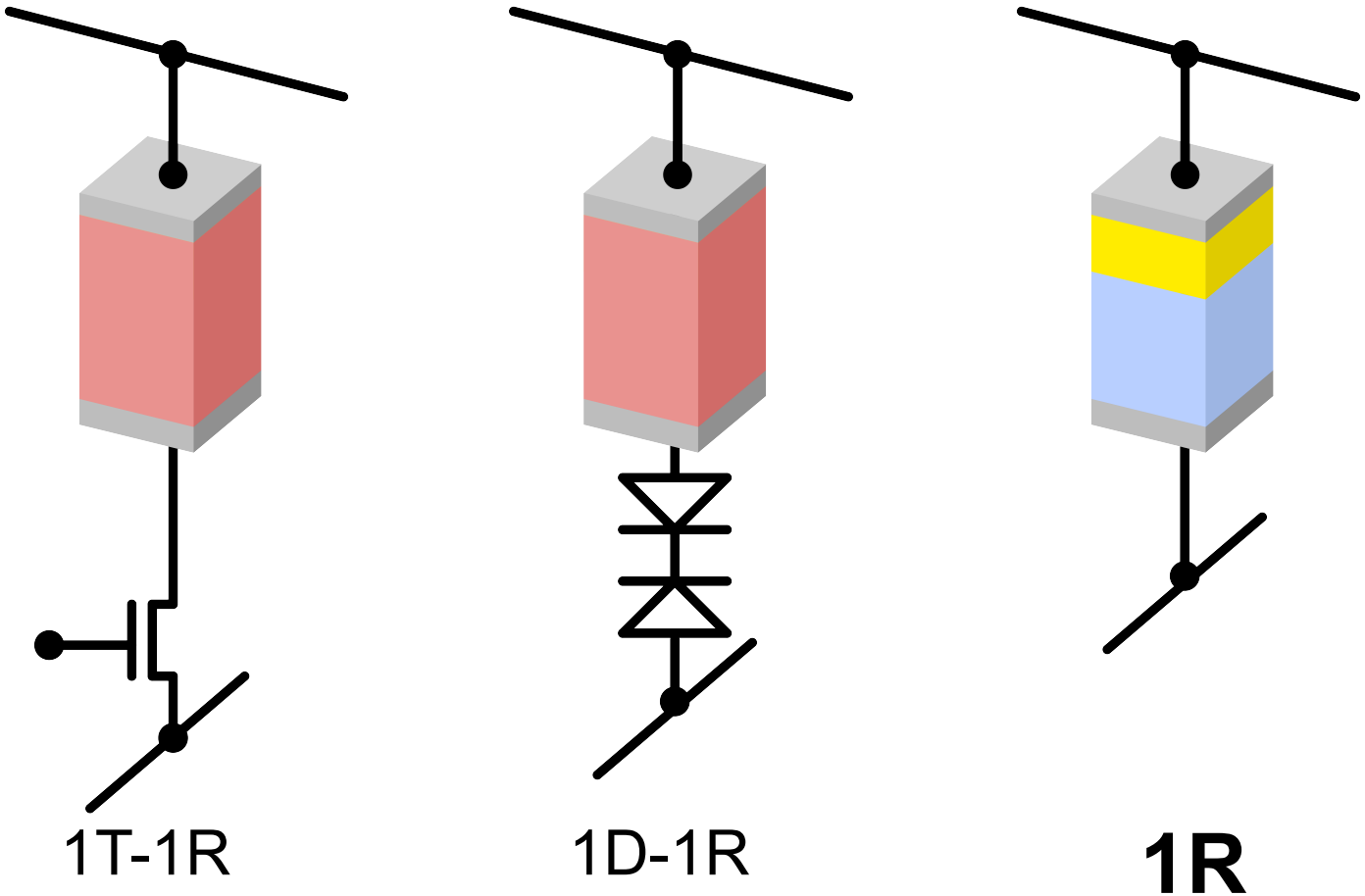
1T-1R



1D-1R

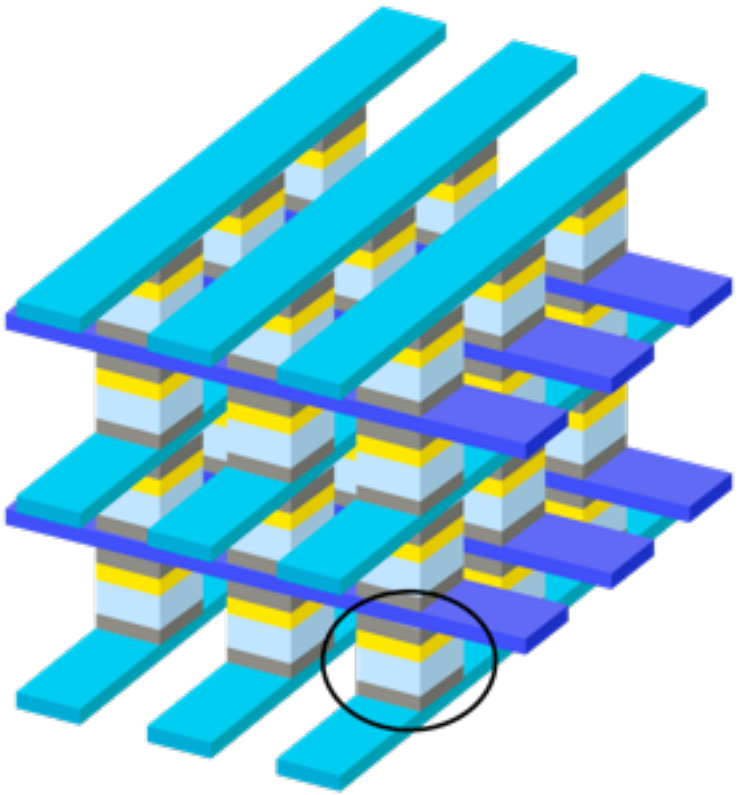
1R

Bitcell Selection



Cross-Point Arrays

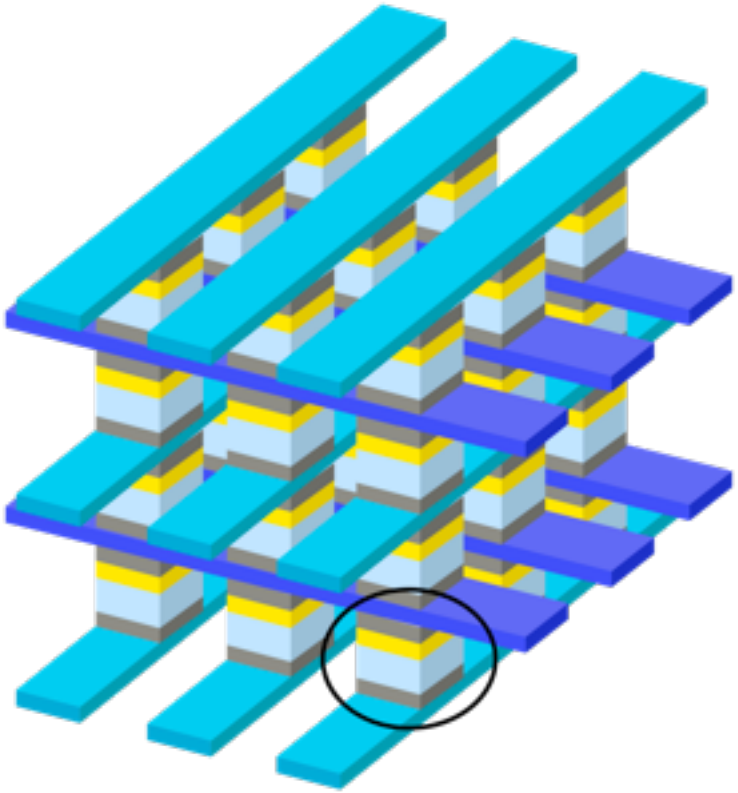
Stacked Planar



$4F^2/N$
2 Masks per Layer

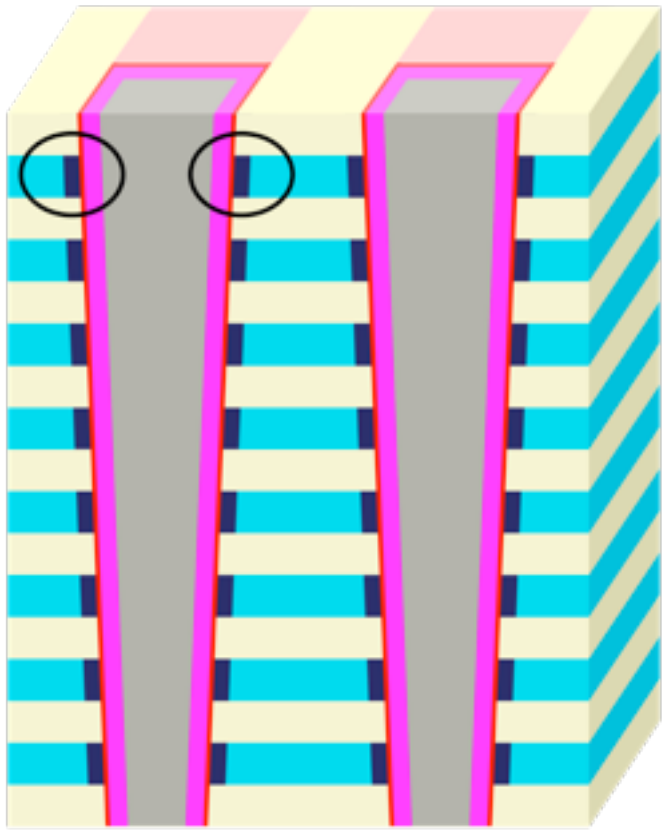
Cross-Point Arrays

Stacked Planar

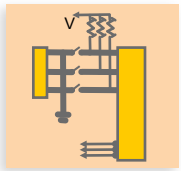


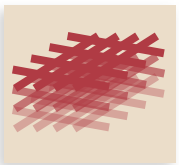
$4F^2/N$
2 Masks per Layer

Stacked Vertical



$2F^2/N$
2 Masks per 8 Layers





Storage Interface

NVM Handling

NVM Interface

Design & Architecture

NVM Bitcell

NVM Handling: $1B+

NVM Handling: $1B+

SandForce™

$350M

anobit

$400M

$250M

NVM Handling: $1B+

SandForce™

$350M

anobit

$400M

$250M

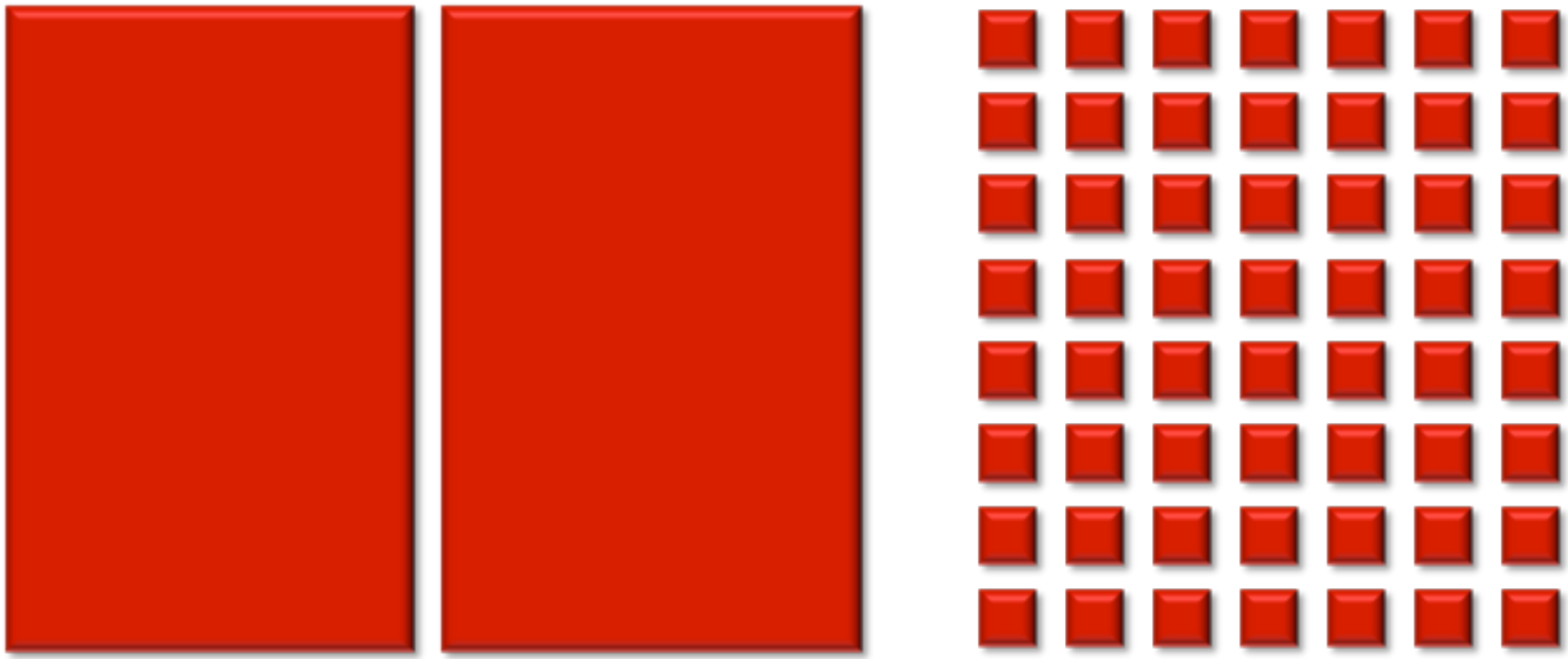
- NVM handling makes failing NAND bitcells usable
- Requires deep knowledge of bitcell & architecture

Memory Array Architecture

Memory Array Architecture

NAND: Few massive arrays
built from erase blocks

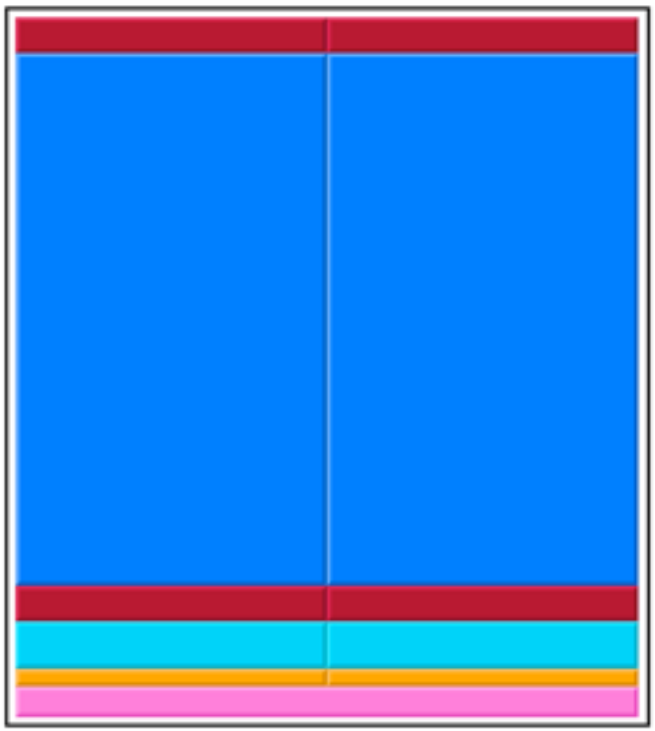
Memory Array Architecture



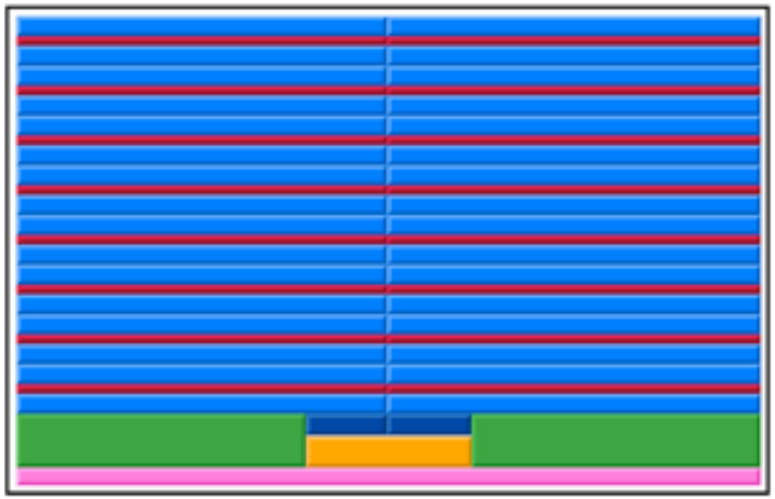
NAND: Few massive arrays built from erase blocks

RRAM: Numerous memory tiles

Memory Array Efficiency

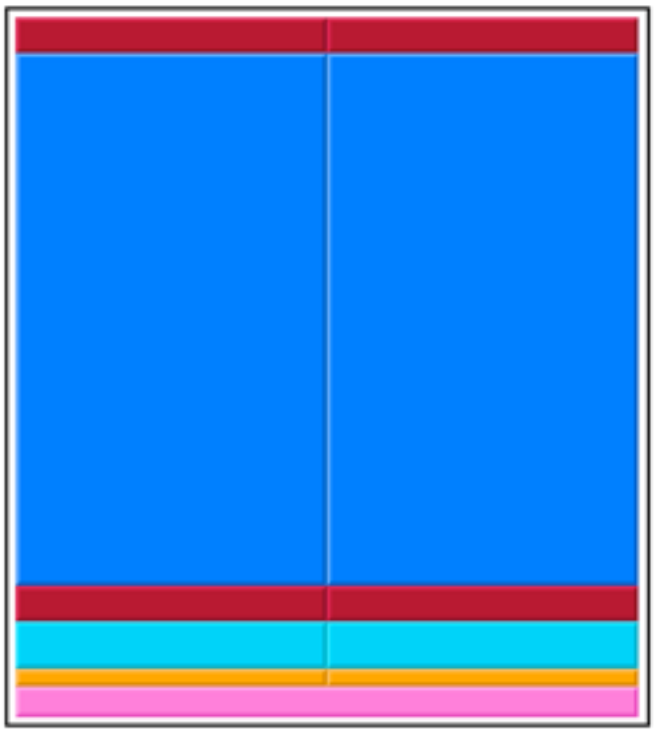


256Gb PBiCS
3D-NAND (projected)



1Tb 1R
3D-RRAM (projected)

Memory Array Efficiency



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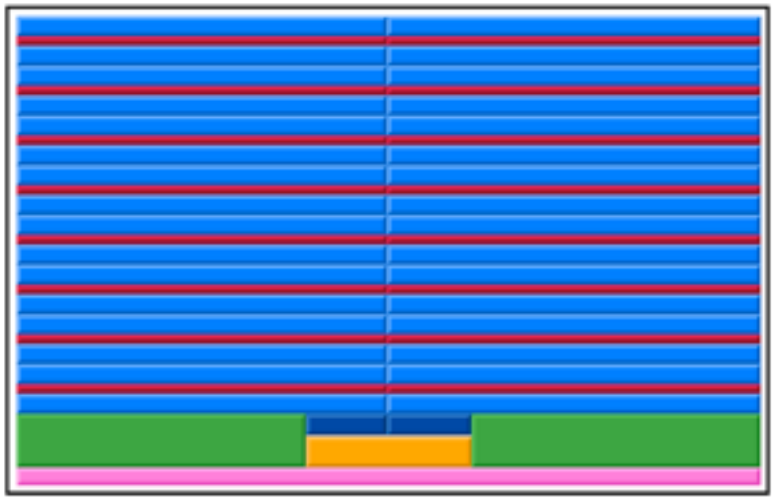

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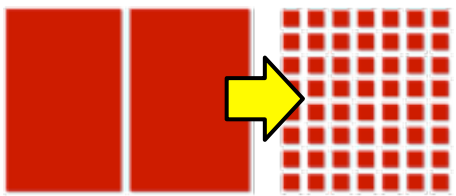
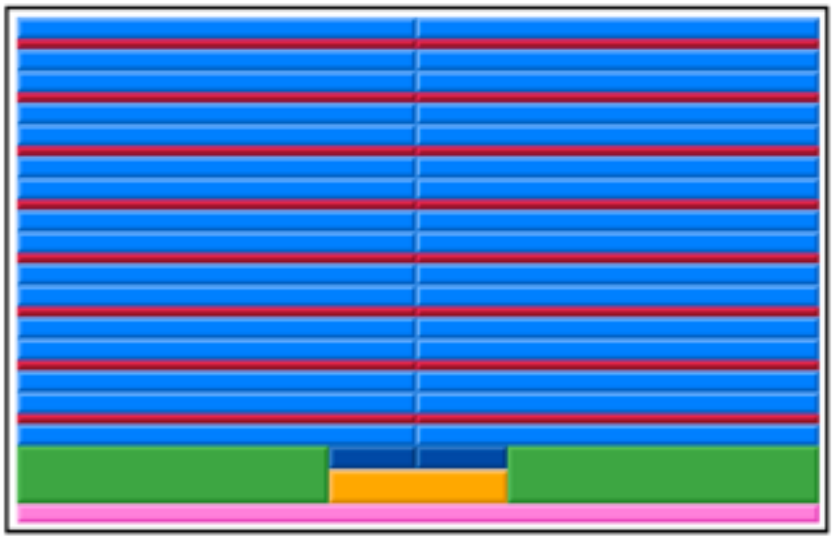
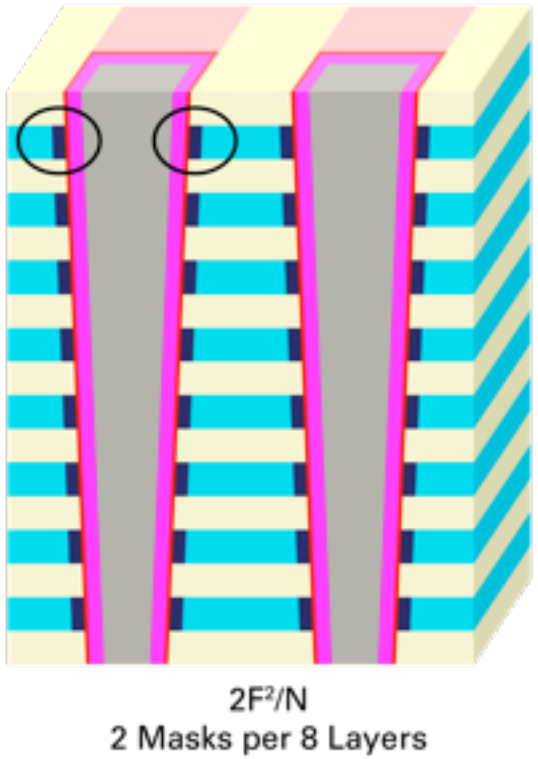


NVM Handling: Examples



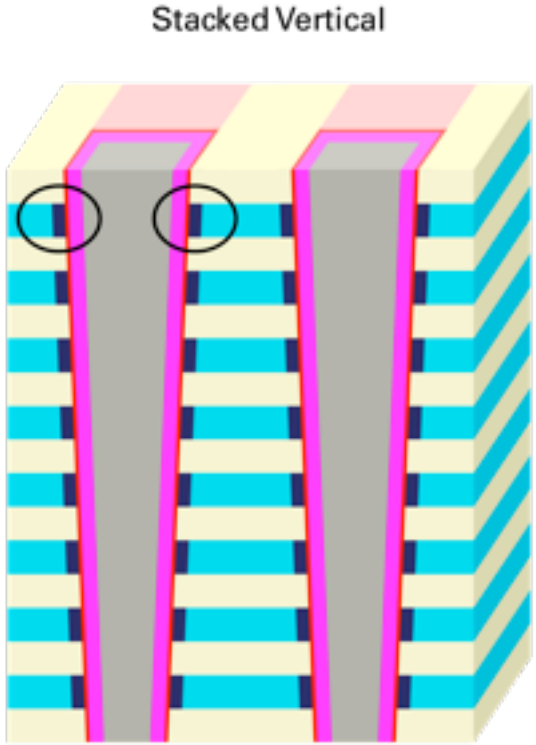
Block → Tile Management



2D → 3D Bit Interference

NVM Handling: Examples

Block → Tile Management



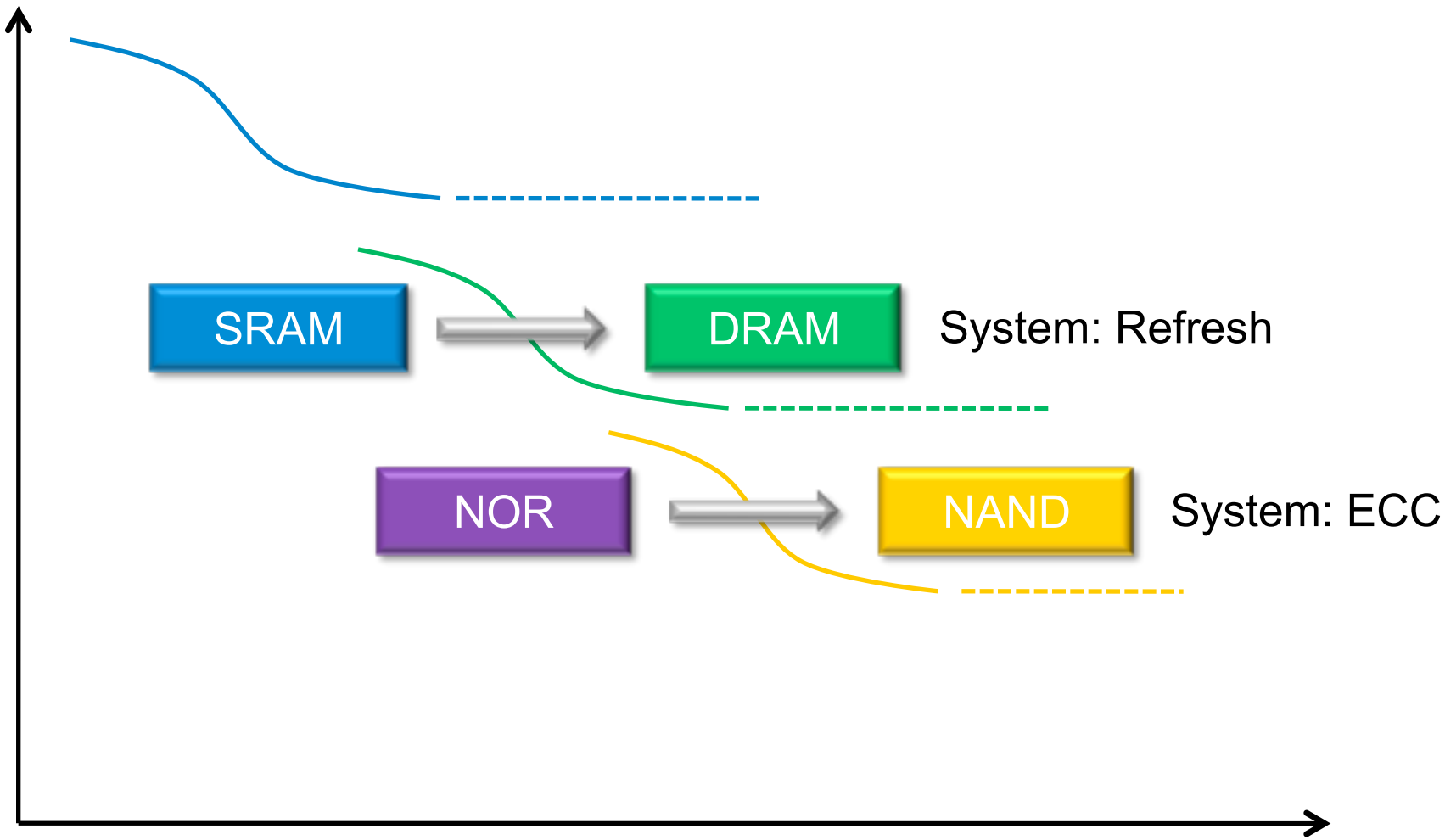
2D → 3D Bit Interference

NVM Handling: Examples

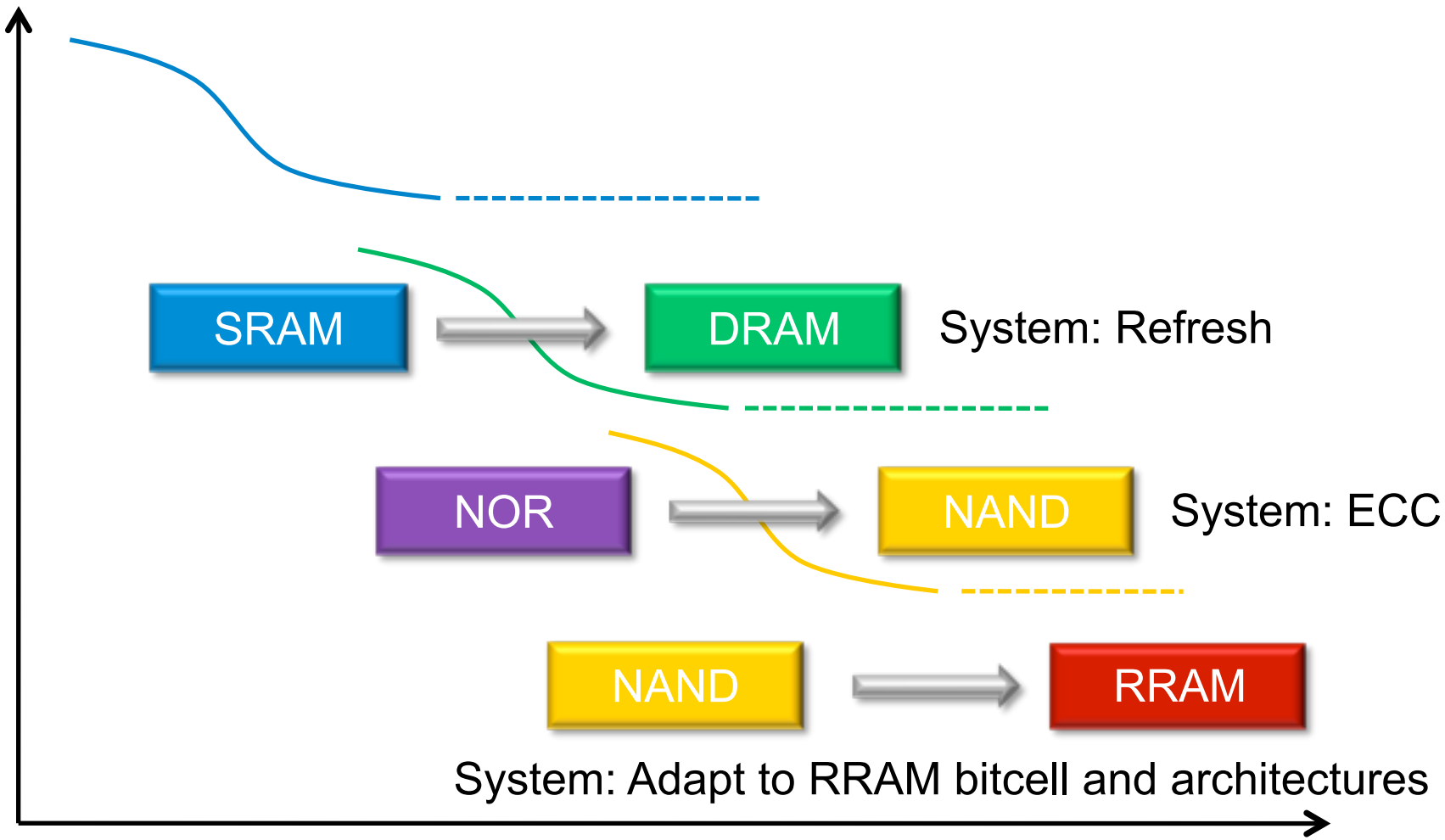
Block → Tile Management

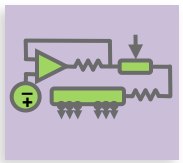
2D → 3D Bit Interference

NVM Handling: System



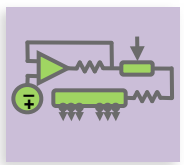
NVM Handling: System





Storage Interface

NVM Handling

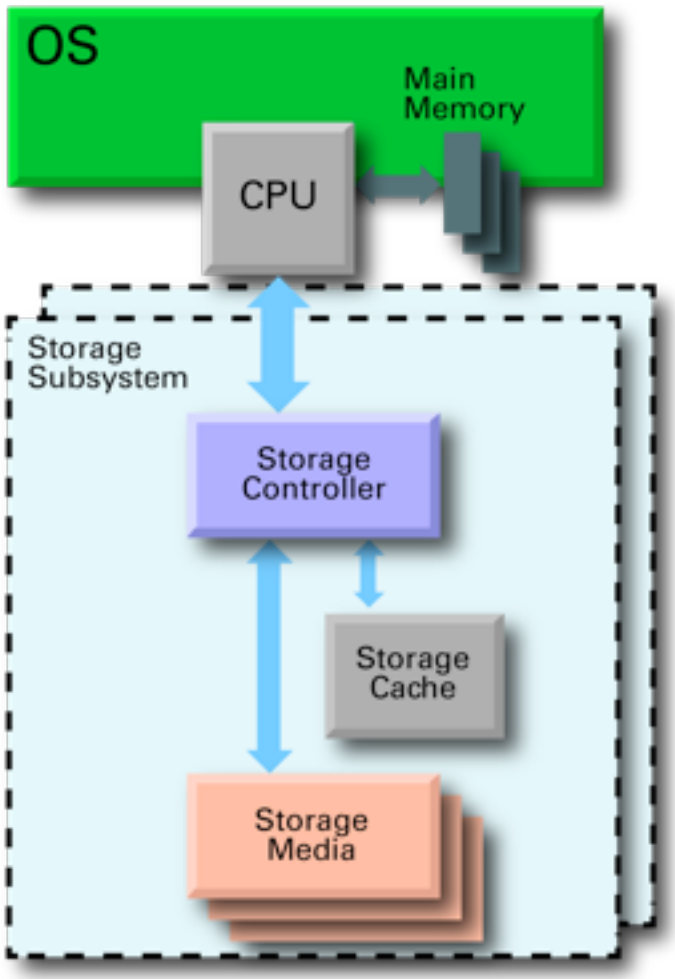


NVM Interface

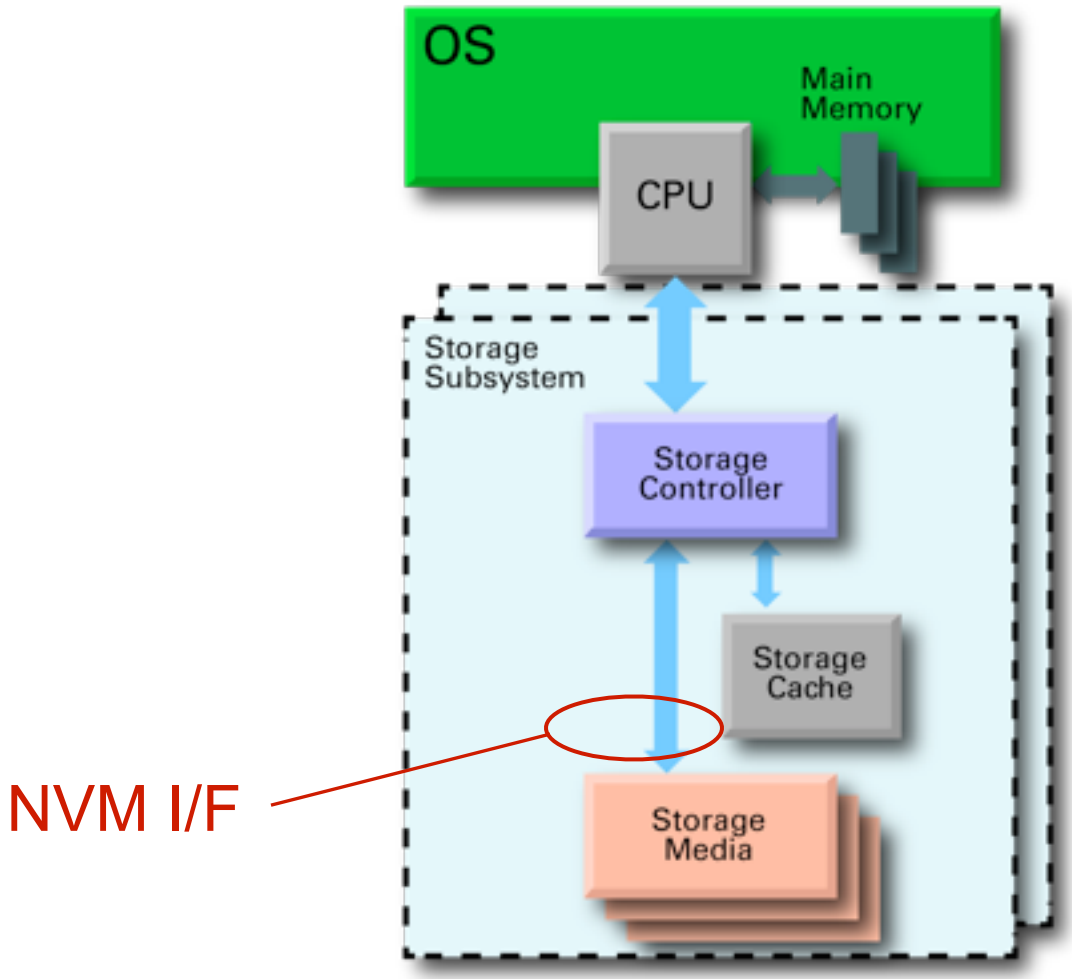
Design & Architecture

NVM Bitcell

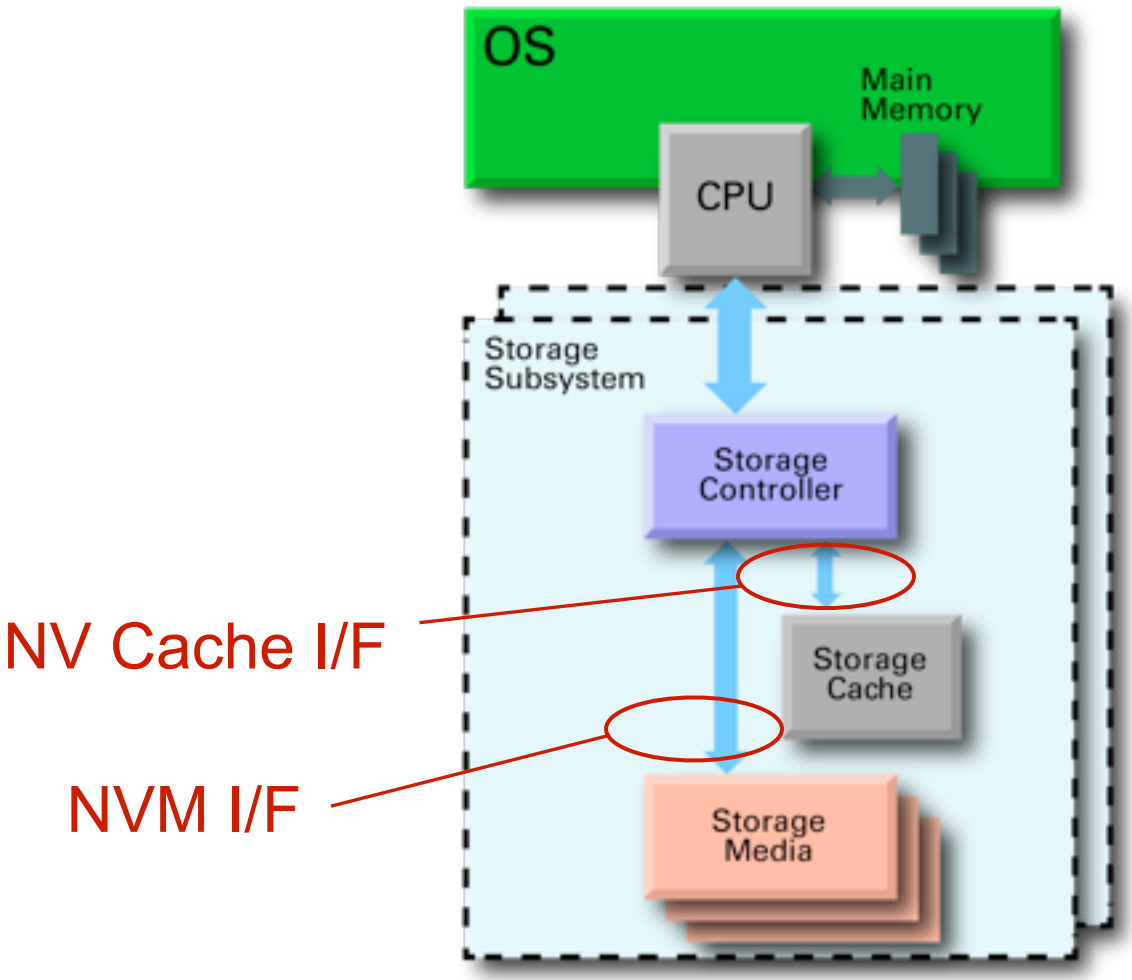
Interfaces in a Storage System



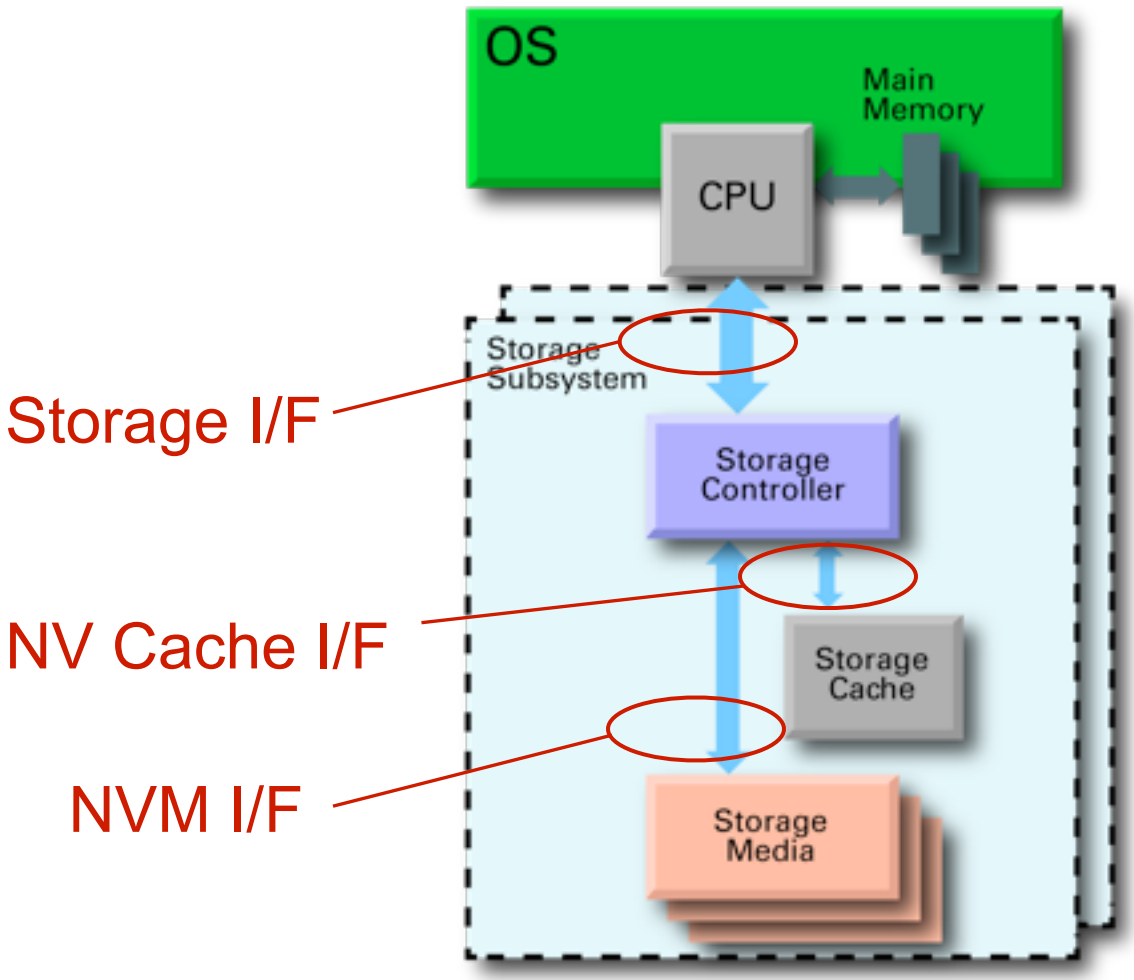
Interfaces in a Storage System



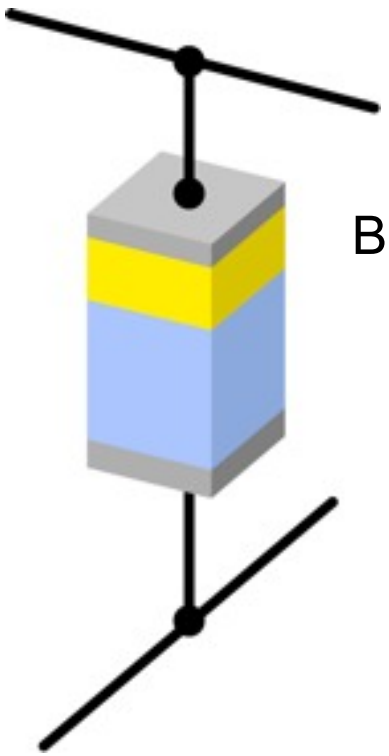
Interfaces in a Storage System



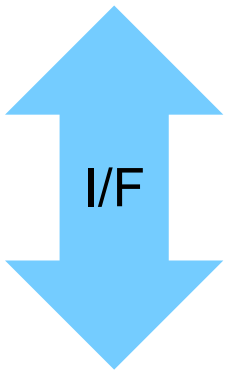
Interfaces in a Storage System



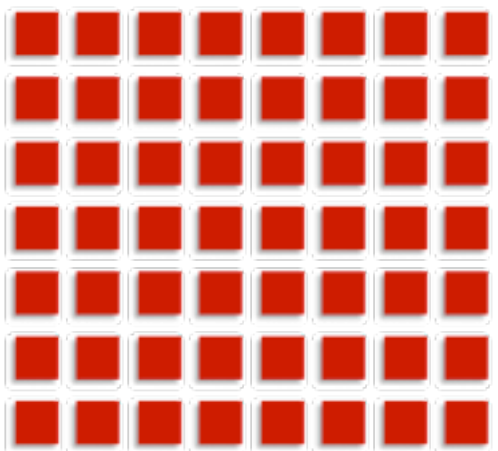
Driving the NVM Interface speed



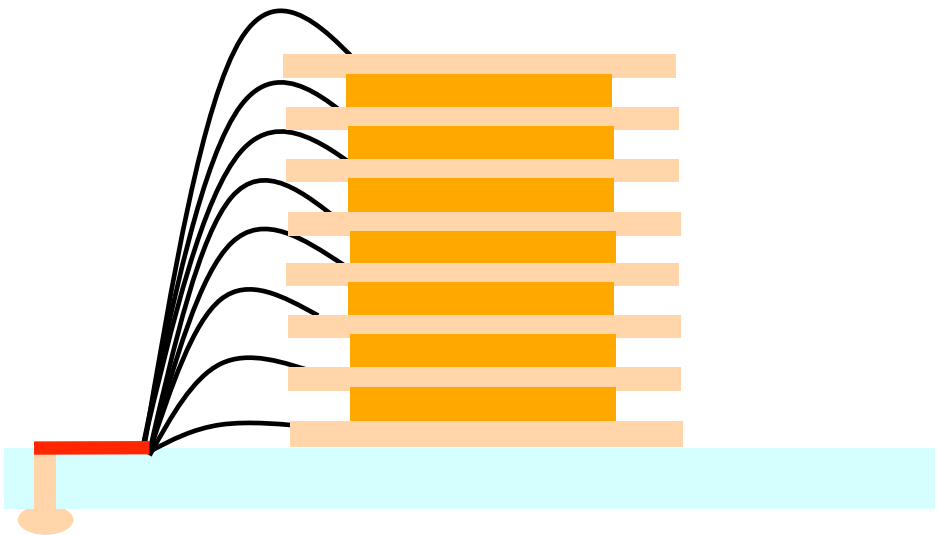
Bitcell switching speed

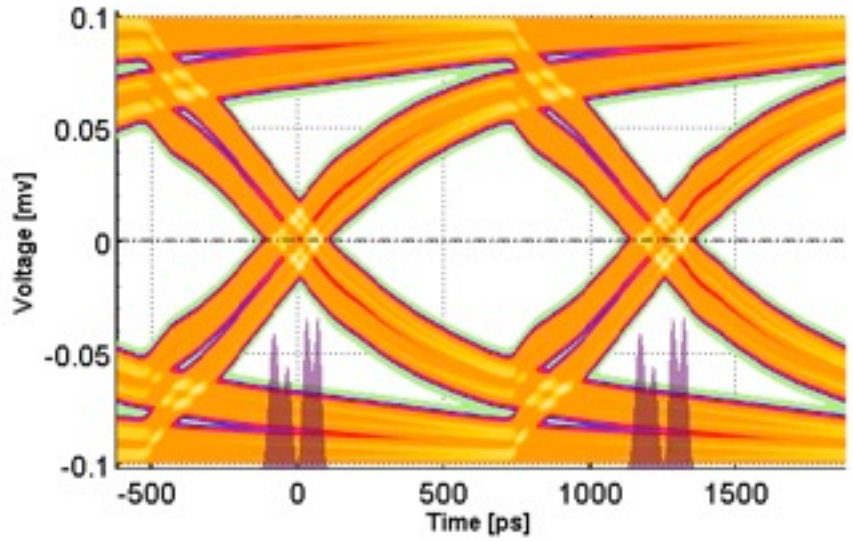


Array parallelism



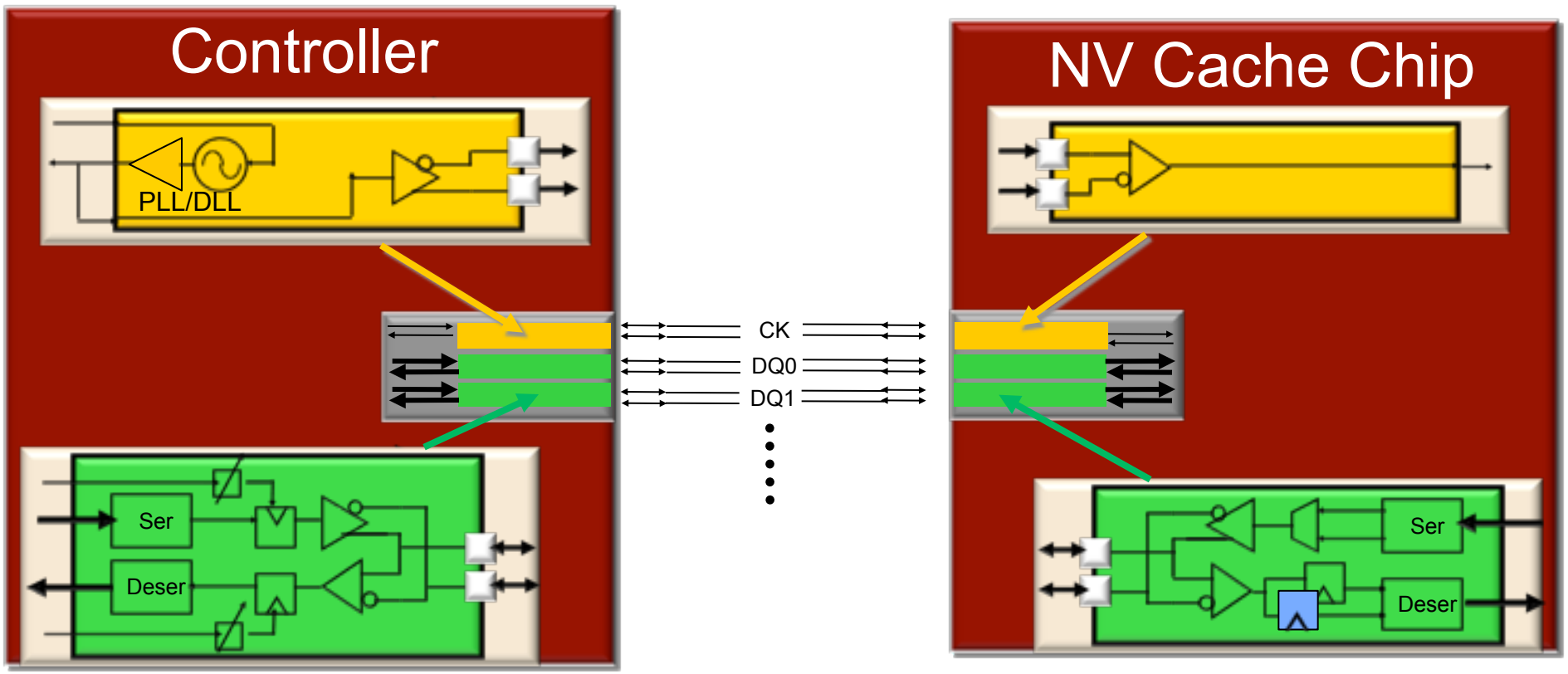
NVM Interface





Capacity	8 loads	16 loads
Max Data Rate per pin	1.2+Gbps	1Gbps

NV Cache Interface

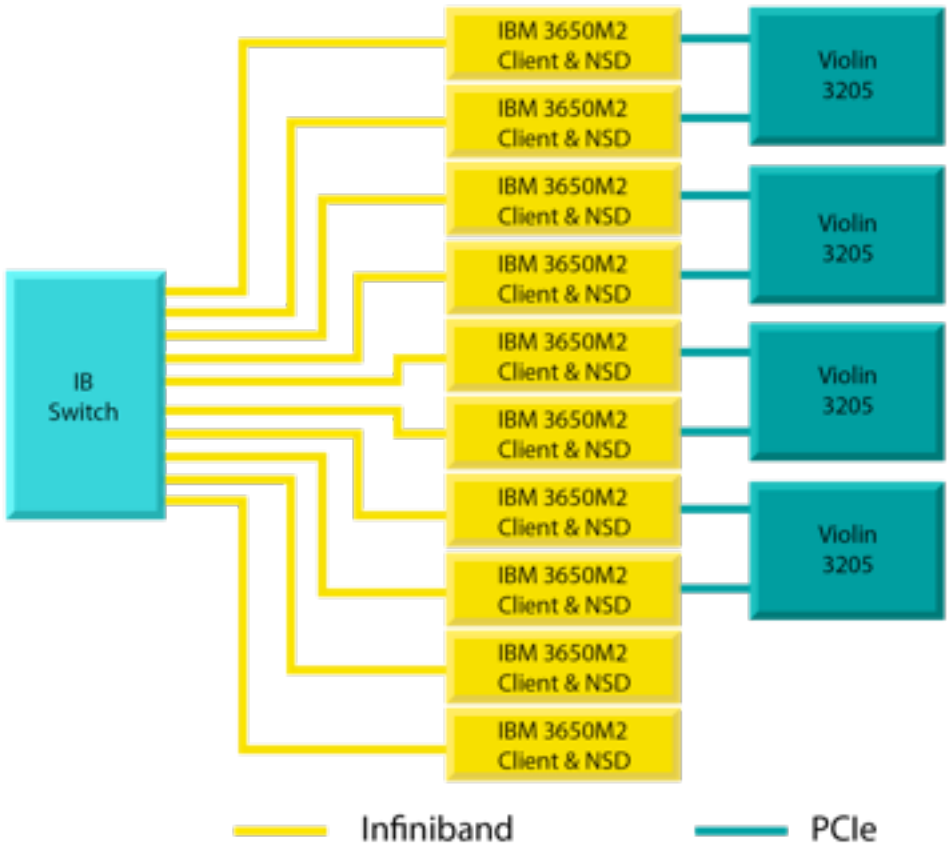


Total Signal Pins (DQ)	Max Data Rate per pin	Read Latency
10 (4 DQ)	4Gbps	Low, Deterministic

Storage: Real World Example

Project Presto! (2011)

- IBM research demonstrated the ability to do policy guided storage management for 10 Billion file environment in 43 minutes. Previous record was 1,591 minutes
  - Used cluster of 10 IBM xSeries servers
  - IBM's cluster file system (GPFS)
  - Placing file system's metadata on new solid-state storage appliance from Violin Memory

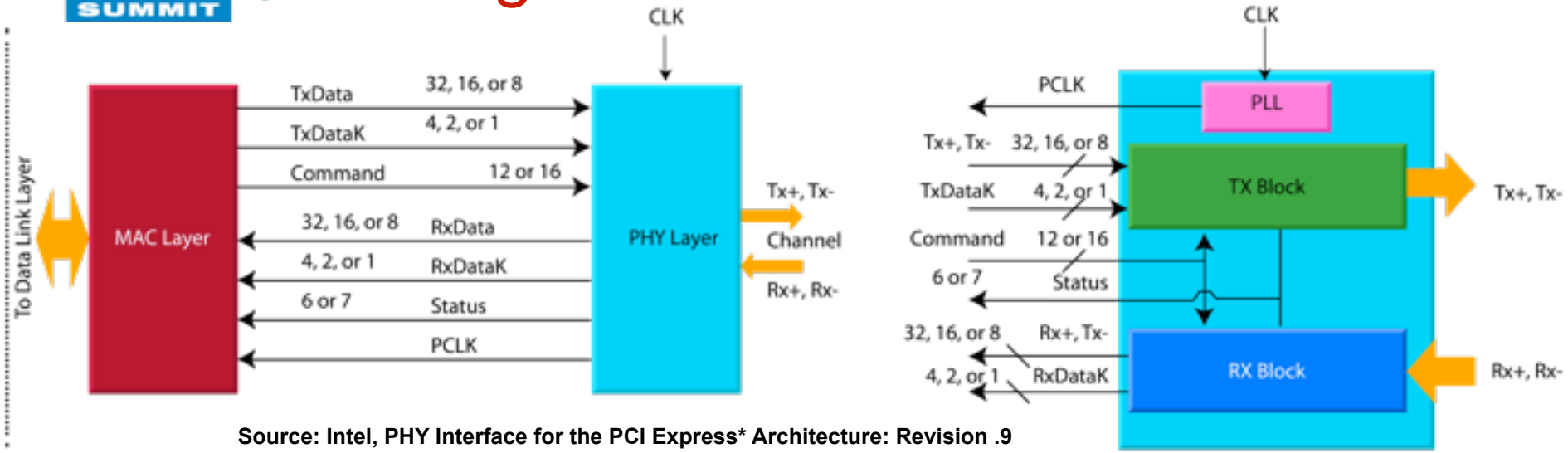


Cooling is the number one concern.

- Server and storage failure due to sustaining high resource utilization.

Source: Storage Class Memory: Technologies, Systems and Applications – FAST, February 2012

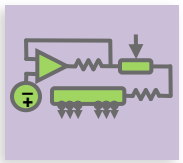
Storage I/F: PCIe Power Reduction



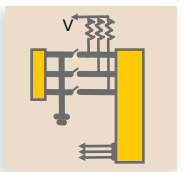
Source: Intel, PHY Interface for the PCI Express* Architecture: Revision .9

- **Active Power Optimization**
  - L1 sub-states => finer granularity power management
  - Dynamic Bus Sizing - Scaling bus width based on changing bandwidth needs
  - Resonant techniques to recirculate clock energy
- **Idle Power Optimization**
  - Fast power On/Off circuits => Deeper power down
  - Leakage control

Virtualization



Storage Interface



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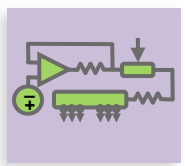

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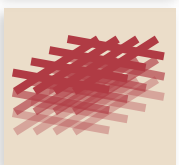
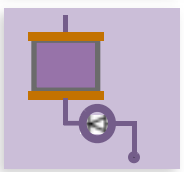


Design & Architecture



NVM Bitcell

Future Trends

Future Trends

INTELLIGENCE → MEMORY

Future Trends

INTELLIGENCE → MEMORY

BEOL MEMORY & LOGIC INTEGRATION

Future Trends

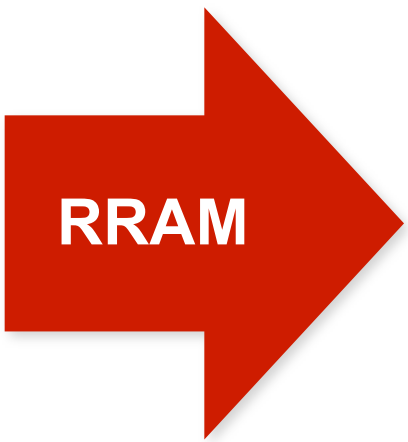
INTELLIGENCE → MEMORY

BEOL MEMORY & LOGIC INTEGRATION

MESH COMPUTING WITH RRAM STORAGE NODES

When?

2012	2014	2016	2018	2020+



When?

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RRAM

Phase 1:
"High Value" Niche Mkt Adoption
- 1T-1R RRAM
- Embedded memory
- NV cache
- New characteristics bring high value
- Not as cost sensitive
- Establish technology

When?

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RRAM

Phase 1:
"High Value" Niche Mkt Adoption
- 1T-1R RRAM
- Embedded memory
- NV cache
- New characteristics bring high value
- Not as cost sensitive
- Establish technology

Phase 2:
NAND Replacement

- 1R RRAM
- Data Storage
- Tb densities
- Lowest cost
- Broad adoption

Quotes

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"…You don't need a weatherman to know which way the wind blows."

- Bob Dylan

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REVOLUTION!
THE IMPACT OF EMERGING MEMORY
DAVID EGGLESTON
SVP NVM STORAGE DIVISION, RAMBUS

Abstract

Each major transition in memory technology has been coupled with a revolution in system architectures that exploit the key advantages of the new memory. NAND flash enters its third decade of mass production as strong as ever, but it appears increasingly likely that a new non-volatile memory technology will emerge over the course of this decade to answer the demands of the data center and the mobile consumer.

- What are the key advantages of these emerging memories?
- What attributes are required to become the successor to NAND flash?
- What sort of revolution will these emerging memories bring to system architectures?
- How (and when) will these new memories bring change to the data center and mobile devices?