

# *Optimize your system designs using Flash memory*

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# Agenda



- Non-Volatile Market & Trends
- Flash Cell Architectures
- Flash Memory Choices
- System Considerations
- Summary



### **2012 Semiconductor Market Forecast**



Source: Gartner 3Q11



### The Embedded Markets



Source: Gartner/iSuppli/Micron 2011



# Embedded Flash Technology Trend



Source: iSuppli, Mkt research, does not include large data applications (ie PMP, MP3, SSD, Media Cards, etc)

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### Cell architectures





# PCM product attributes

- Available in NOR-type options
- Industry driving toward LPDDRx
- Fast programming for NVM
- Fast read capability



### **Evolved Options**

- NOR replacement NOW
- NAND replacement <5 yrs</li>
- RAM replacement <5 yrs</li>

### **Disruptive Options**

- Integrated memories NAND/RAM
- System Cache Options
  - HDD/SDD Integration
  - PCIe

### PCM benefits



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# Solutions for different requirements





#### **Customer Requirements Dictate the Solution**



# NOR product attributes

- Simple command sets
- Cost effective at low densities
- Stable architectures
- Value added features (XiP, security, quality, small data, etc)



### <u>Serial</u>

- Low pin counts
- Easy PCB routing
- Smallest footprint
- Synchronous operations
- Cheapest low density

### Parallel

- Basic add/data interface
- Asynchronous random access
- Synchronous burst operations
- Higher throughput
- Best XiP architecture

# NAND product attributes

- Low pin counts
- Cheapest cost/bit at high densities
- Frequent conversions/migrations required
- Fast programming



### **Discrete**

- Some controllers support boot
- Some standards (ONFI)
- Common packages
- Needs SW for error management
- Demand paging saves bits

### Managed

- Error management onboard
- Some controllers support boot
- Higher density reach
- Easier conversions/migrations
- Standards (MMC, USB, uSD...)

### Flash Architectures – Component Level



All architectures have their advantages

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Trend in the industry moving toward the lower pin count architectures

### NAND technology challenges

#### How to manage the ECC requirements?

- NAND controllers with high ECC capability
- ECC NAND managed solutions
  - on-die ECC, ClearNAND
- Fully managed solutions
  - eMMC, eUSB, others

#### How to manage lower Endurance?

- Understand the application and usage model
  - How does the file system work?
  - How often are you programming?
  - How big is the data file/s?
  - What is the PLC of your system?



Determines PE Cycles and Density Required

#### Intersecting your project and the memory technology is key to success!



### NAND system solutions for Industry

Host Controller I **Raw NAND** for application "expert" with NAND data NAND Interface **Raw NAND** NAND BUS management and ready to support ECC needs. ECC FTL LLD Host Controller II **ECC NAND** for application that do not want to change the ECC NAND **NAND** Interface NAND BUS ECC with the NAND litho shrink. ECC FTL LLD Host Controller III SPI Serial NAND for application requiring high density with ECC **SPI Interface** SPI BUS Serial protocol. FTL LLD eMMC NAND Host Controller IV **eMMC interface** for application that want to offload by any ECC eMMC Interface MMC BUS NAND data management with a standard interface. LLD FTL Host Controller V **eUSB NAND eUSB interface** for application that want to offload by any ECC **eUSB** Interface USB BUS NAND data management with a standard interface. LLD FTL



### Level of Management by NAND solutions

### Level of Management by NAND Solution

	Raw NAND	ECC NAND (On-Die ECC, ClearNAND)	Fully Managed (eMMC, eUSB)
Complexity of Customer Development (NAND Management by Host)	High	Med	Low
New Product Qualification (Complexity & Effort)	High	Med	Low
Relative Cost	Low	Med	High

Trade offs between Complexity, Qualification Effort & Cost



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### Performance considerations for system solutions



Raw NAND, ECC NAND and eMMC require different management software

The correct performance evaluation is at system

 LLD = Low Level Driver
 ECC = Error Correction Code
 FTL = NAND Scheduling Logical Mapping, Bad Block Management, Wear Leveling

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# Memory subsystem designs/architecture



#### Execute in Place (XIP) Architecture

#### "Store and Download" (SnD) Architecture



- Simple architecture
- Possible to reduce DRAM density
- Lower stand-by power

- Complex but higher performance
- More DRAM required
- Higher stand-by power

#### 

# System cost reductions and simplification

#### Software Architecture



#### **Understand Your Usage Model**

- xRAM Usage models
- How many CE#/Banks do you use
- Why might you split memory into separate chips
- Other system SW requirements (file system, data logging, etc)



Performance vs. Cost ratio

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### Larger Data Fetches

Random Read Access Performance vs. Data Size



### Performance Comparison – Small Data

Random Read Access Performance vs. Data Size



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# Memory technology comparison



All memory technologies have their advantages

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Look for ways to differentiate and stay cost effective

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### What's next?

### **Customers**

- 1. Understand memory usage
- 2. Understand true cost
- 3. Work with a trustworthy supplier



### **Suppliers**

- 1. Provides technology leadership & product longevity
- 2. Architecture transparency
- 3. Systems expertise & silicon/solution standards



### **Broadest Portfolio**

- Industry's broadest portfolio
- Computing, server/networking, embedded, mobile, consumer





# Micron's Product Portfolio

#### NOR

- Parallel and Serial NOR product portfolios, densities 512Kb-2Gb+
- Technology leadership on 65nm and 45nm.
- Automotive and industrial qualified solutions

#### NAND

- Discrete and managed solutions, densities 128Mb-64GB
- Technology leadership on 20nm
- Automotive and industrial qualified e·MMC<sup>™</sup> solutions
- Legacy support for low density NAND

#### DRAM

- Legacy SDRAM through cost/performance leading DDR3 offerings
- Discrete and module DRAM solutions
- High speed RLDDRx Options
- Automotive and industrial qualified solutions

#### **Phase Change Memory**

- First commercially available PCM products
- P5Q: Serial NOR compatible, densities 32-128Mb
- Award winning technology
- New families on 45nm













