ST-MRAM for High Volume Commercial Memory

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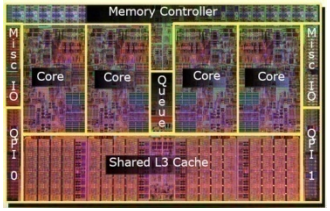
Types of High-Volume Commercial Memory

Non-Volatile

- NAND Flash
  - Charge storage on floating gate
  - Very high density
  - Fault-tolerance using ECC
  - Limited write endurance
- NOR Flash
  - Charge storage on floating gate
  - High density
  - Faster access than NAND
  - Nearly 100% good bits (ECC)
  - Limited write endurance

Volatile

- DRAM
  - Charge storage on capacitor
  - High density
  - “Infinite” read/write (Endurance)
  - Nearly 100% good bits (ECC)
- SRAM
  - 6 transistor latch
  - Very fast read/write
  - “Infinite” read/write
  - 100% good bits (no ECC)

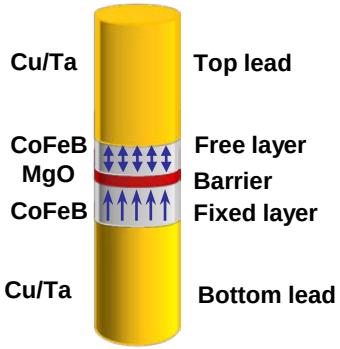


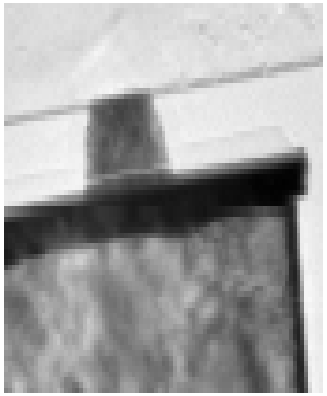
Alternate (non charge based) Storage Mechanisms

- Moving Atoms
  - PCM, CBRAM, RRAM (Filament, Metal Oxide), FeRAM, CNT, Molecular....
- Moving Spins
  - MRAM, STTRAM, Racetrack...

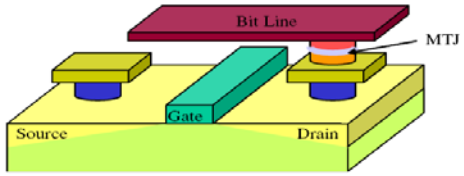
Spin Transfer Torque (STT) RAM

Technology: Magnetic Tunneling Junction (MTJ) device





MTJ



STTRAM cell

Advantages:

- No capacitor
- Very fast (<1ns) switching possible
- High endurance (>1E15 cycles)

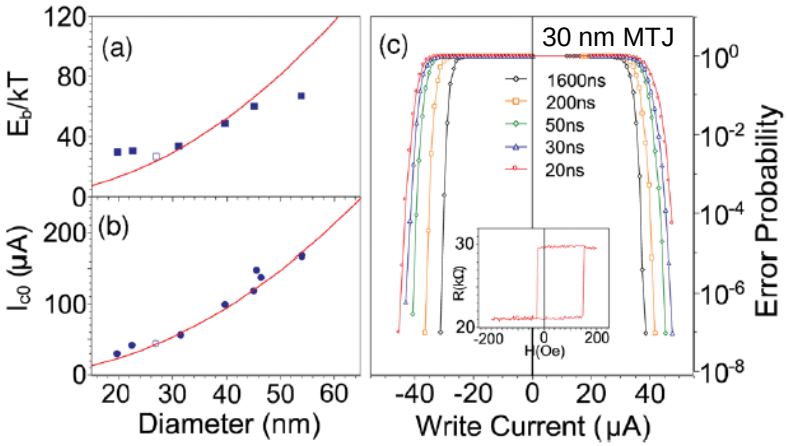
Disadvantages:

- Likely problems with:
  - Refresh, Soft Errors,
  - ECC likely required
- Programming current scaling requires more materials research
- System level solutions needed

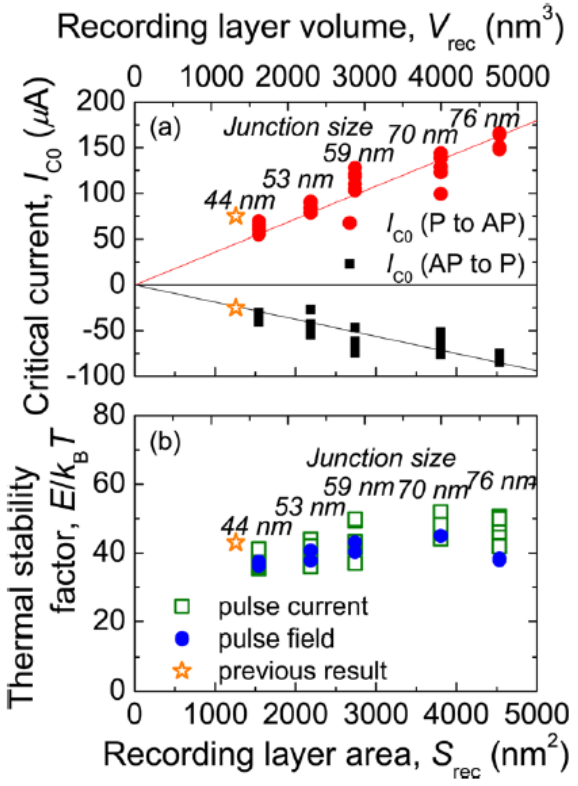
ST-MRAM Technology Challenges

- Physical mechanism of PMA still being understood/debated
- Memory cell concept not proven in high-density array or at leading edge lithography
- Manufacturing concerns of complex stack of many (~8) thin (~sub-1nm to 10nm) layers
- High current selector device needed, limiting cell size
- Fastest switching (~1ns) requires high current (~1mA)
- Scalability not demonstrated and concerns about thermal fluctuations (retention) and writing voltage/current (reliability)

Scalability - Retention vs. Write Current



IBM; M. Gajek et al., Appl. Phys. Lett. 100, 132408 (2012)



Tohoku Univ.; H. Sato et al., Appl. Phys. Lett. 99, 042501 (2011)

High Volume Manufacturing (HVM) - Challenges and Gaps

MTJ Stack Deposition

- Complex stack of multiple films with thickness control at < 0.1 nm

MTJ Stack Etch

- Subtractive removal of multi-layer metal stack for on pitch features at <30nm

Film Metrology

- Composition and thickness measurement with < 0.1 nm accuracy

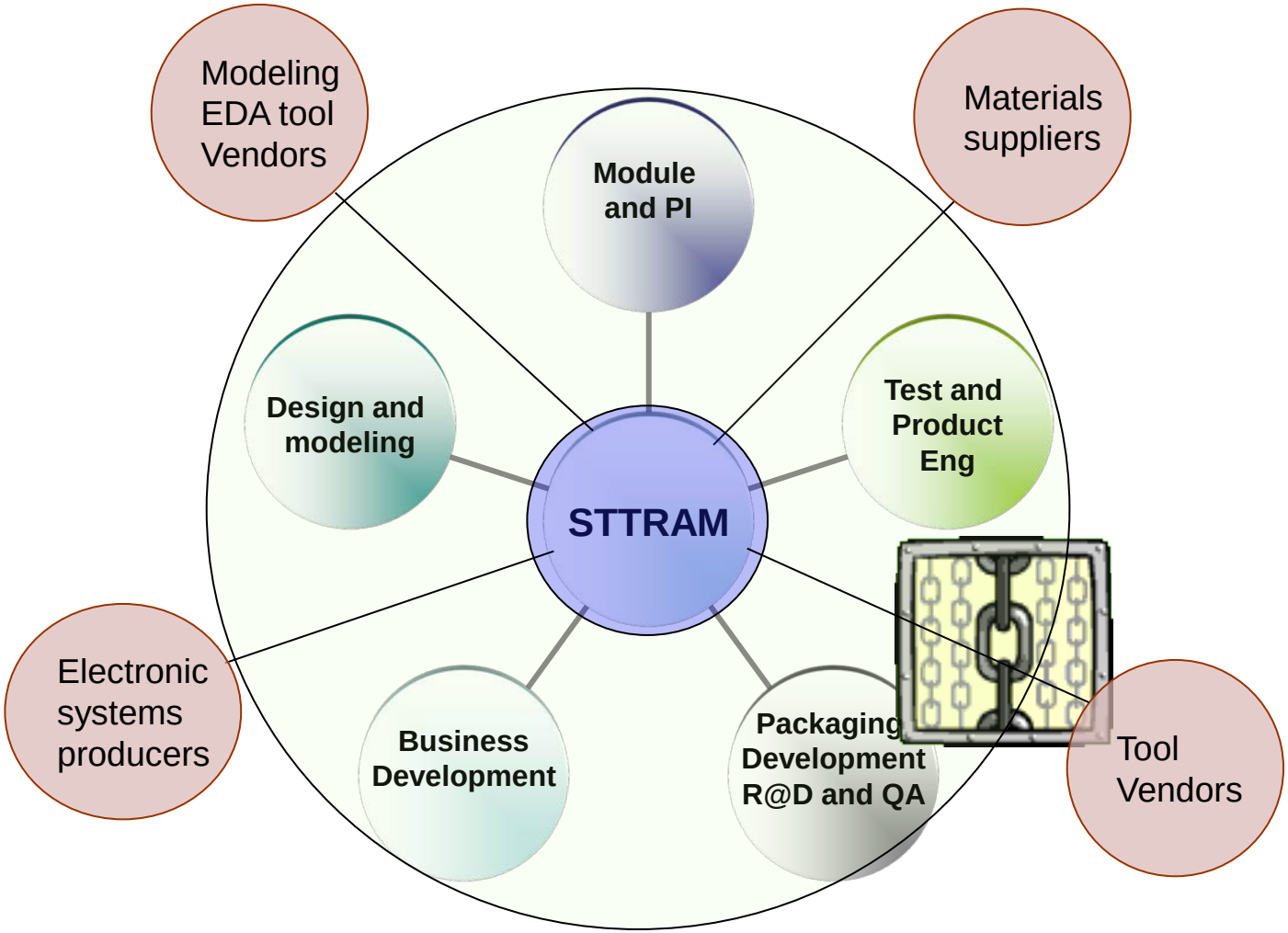
Market Opportunities

- Meet “Always On/Always Connected” requirements of newer/future operating systems without limiting memory capacity
  - Translates to very long standby battery life - key feature of ultra-thin notebooks and other mobile platforms
- Hybrid storage-class memory – use ST-MRAM as a cache/write-buffer in conjunction with a slower/higher density NV memory type
  - Eliminates the risk of losing buffer contents due to power loss

Market Opportunities

- Replace Flash-backed/NVDIMMs
  - NVDIMMs are a step forward from battery-backed DIMMs; ST-MRAM DIMMs can continue the progression
  - Eliminate super-caps, use a single memory type, simplify system implementation

Technology Deployment – IDM perspective



Summary

- ST-MRAM is a promising emerging memory technology
- Socket level replacement of DRAM is highly unlikely
- Technology has potential to serve and enable new value-add applications