3 Bit Per Cell NAND Flash Memory on 19nm Technology

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Forward Looking Statement

During our meeting today we will be making forward-looking statements.

Any statement that refers to expectations, projections or other characterizations of future events or circumstances is a forward-looking statement, including those relating to revenue, pricing, market share, market growth, product sales, industry trends, expenses, gross margin, future memory technology, production capacity and technology transitions and future products.

Actual results may differ materially from those expressed in these forward-looking statements due to the factors detailed under the caption "Risk Factors" and elsewhere in the documents we file from time-to-time with the SEC, including our annual and quarterly reports.

We undertake no obligation to update these forward-looking statements, which speak only as of the date hereof.

Outline

- Introduction to 3 bits per cell
- Margin loss due to temperature
- X3 program algorithm
- Performance and endurance tradeoff
- High speed IO TM 400Mbps
- Conclusion

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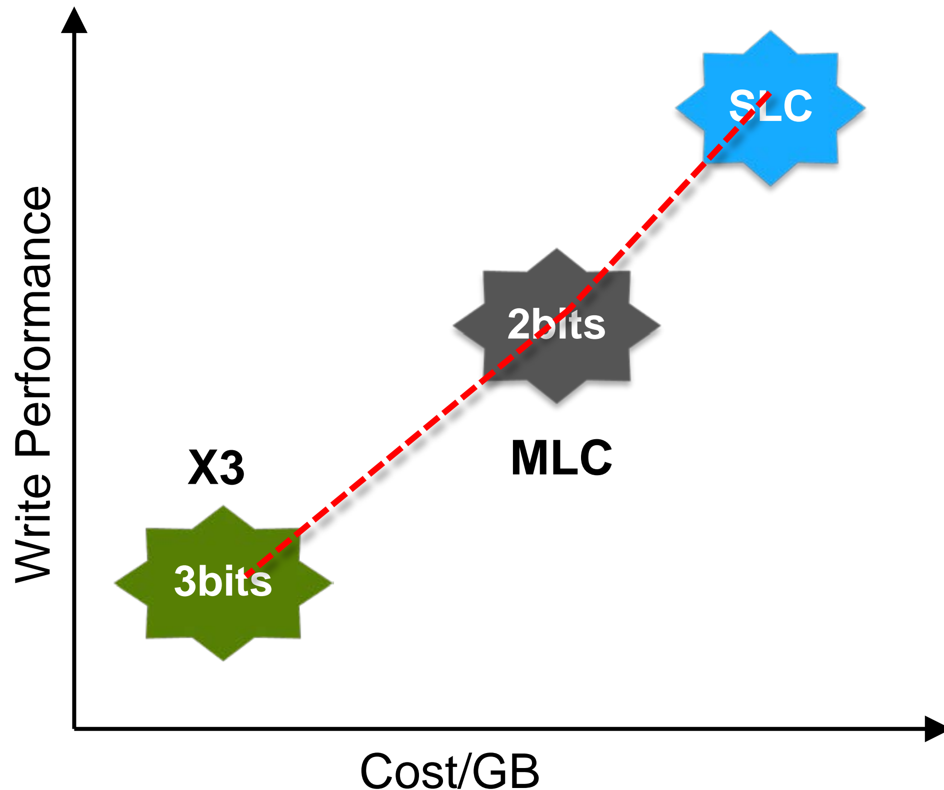
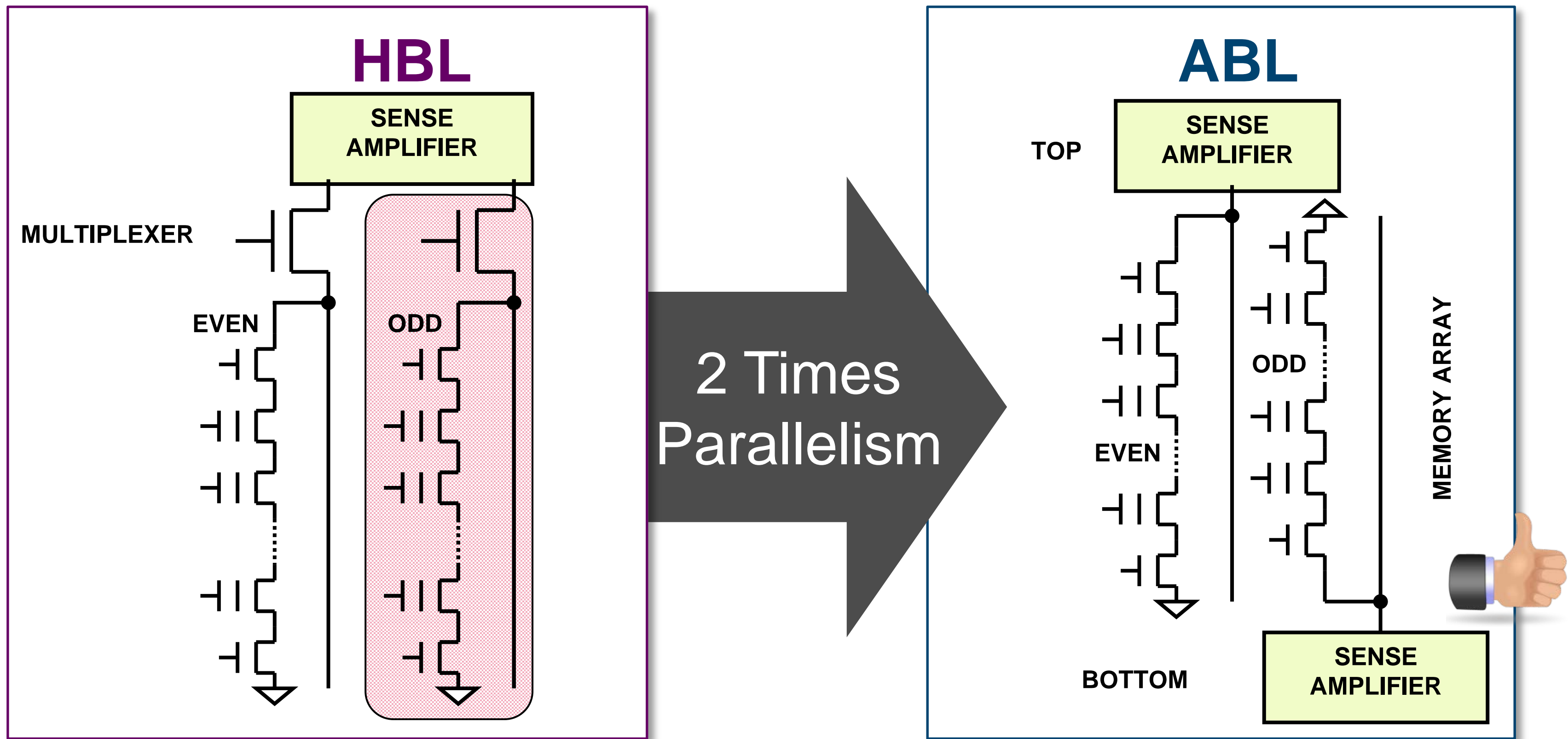
SLC MLC X3



- Ever increasing digital data – increase demand for NAND flash memory
- The Read Perf in X3 does not differ much between SLC/MLC

All Bit Line Architecture (ABL) for High Performance



Comparison	Conventional	ABL
Write	Half of Bitlines	All of Bitlines (x2)
Read	Half of Bitlines	All of Bitlines (x2)
Erase	Whole Block	Whole Block

Endurance is better (Less PD)

ABL and X3 Technologies

X3 Technology

Maintain low cost

Reduce die size

ABL Technology

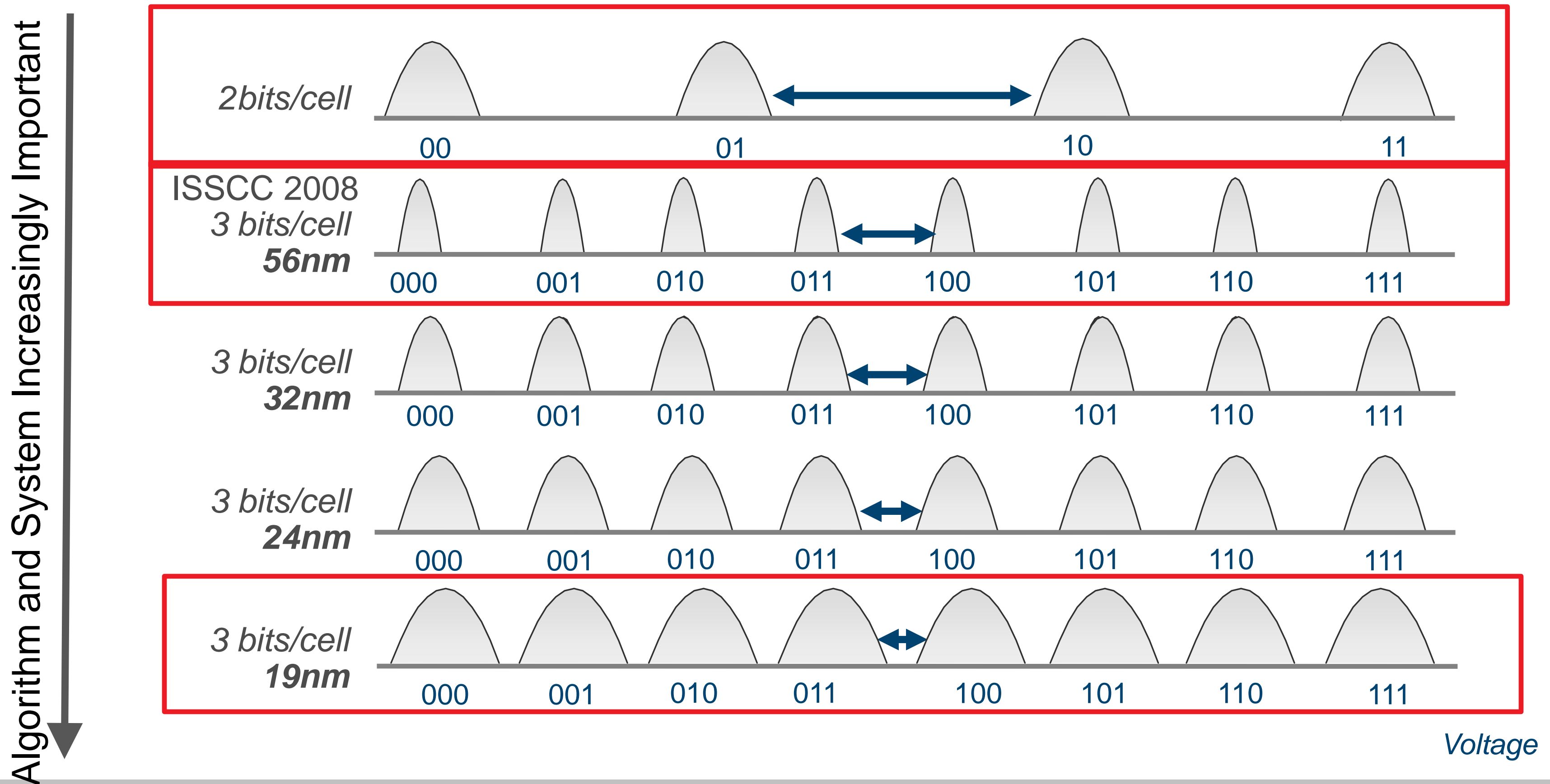
Increase performance

Reduce power consumption

Combining X3 and ABL technologies @19nm means

Enabling many applications with higher capacity in Small Form Factor

Cell Degradation from Physical Scaling



- Need innovative algorithms to maintain the reliability
- Shrinking Vt margin requires more system management

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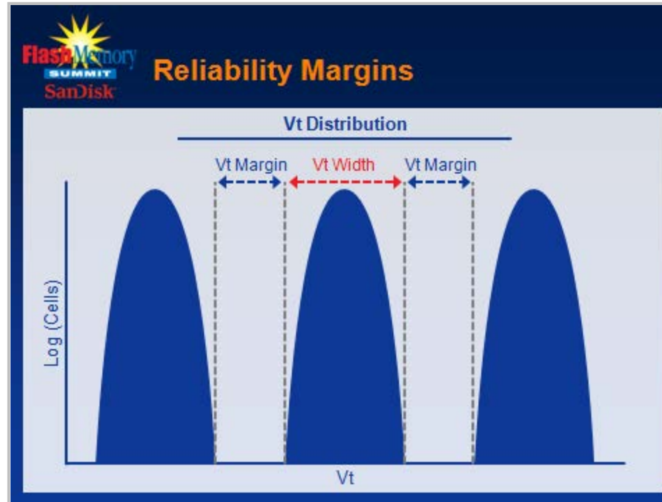
Factors Affecting Vt Window

Based on SanDisk Internal Evaluation

Low End Vt Limitations

(a) Ability to sense deeper

(b) Can not Erase deeper



High End Vt Limitations

(1) Can not Program higher

(2) Program Disturbs

Vt Margin Budgets for

(a) Program/Read Disturb

(b) Program/Erase cycling and Data Retention

(c) Margin loss (such as temp cross)

Factors Affecting Individual Vt Width

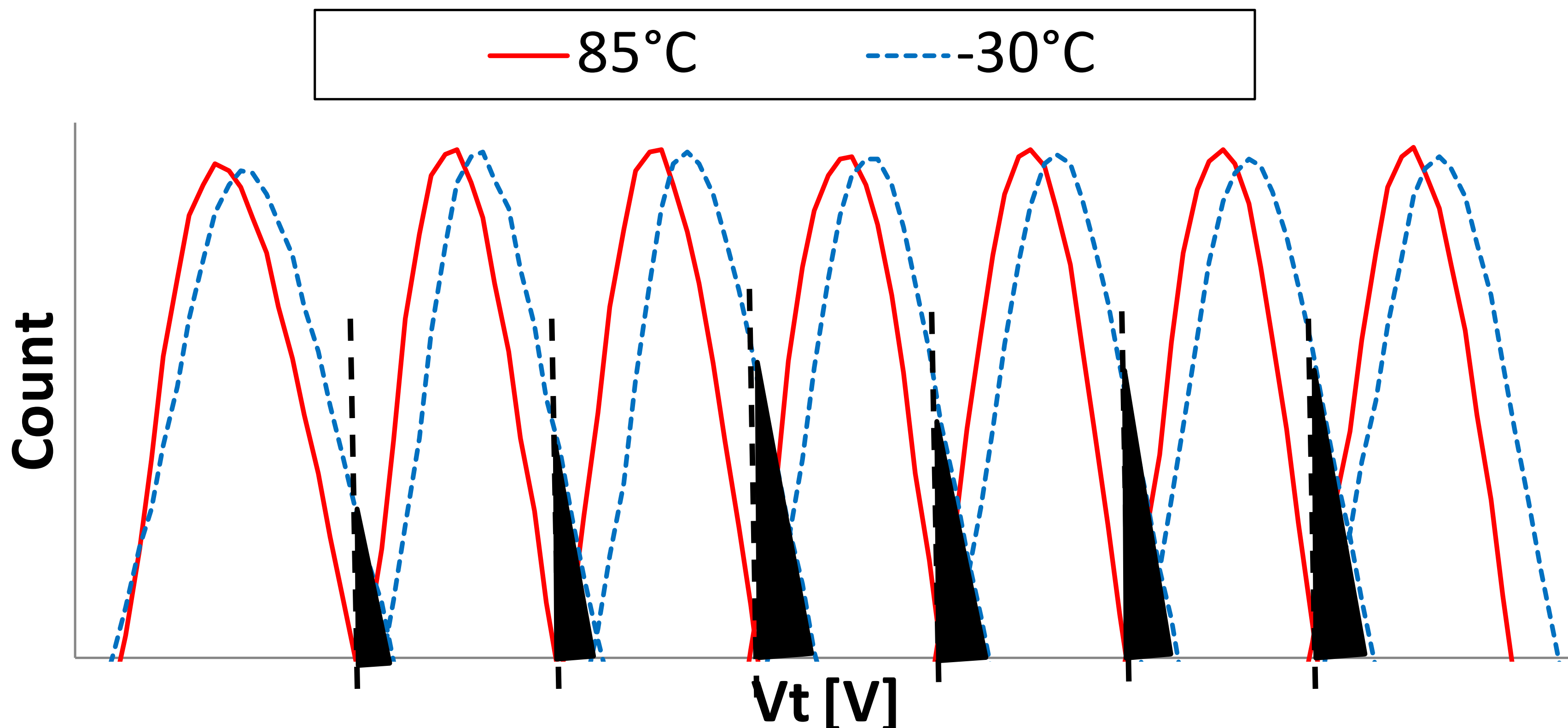
(1) Programming step size

(2) ECC capability

(3) Cell scaling factors

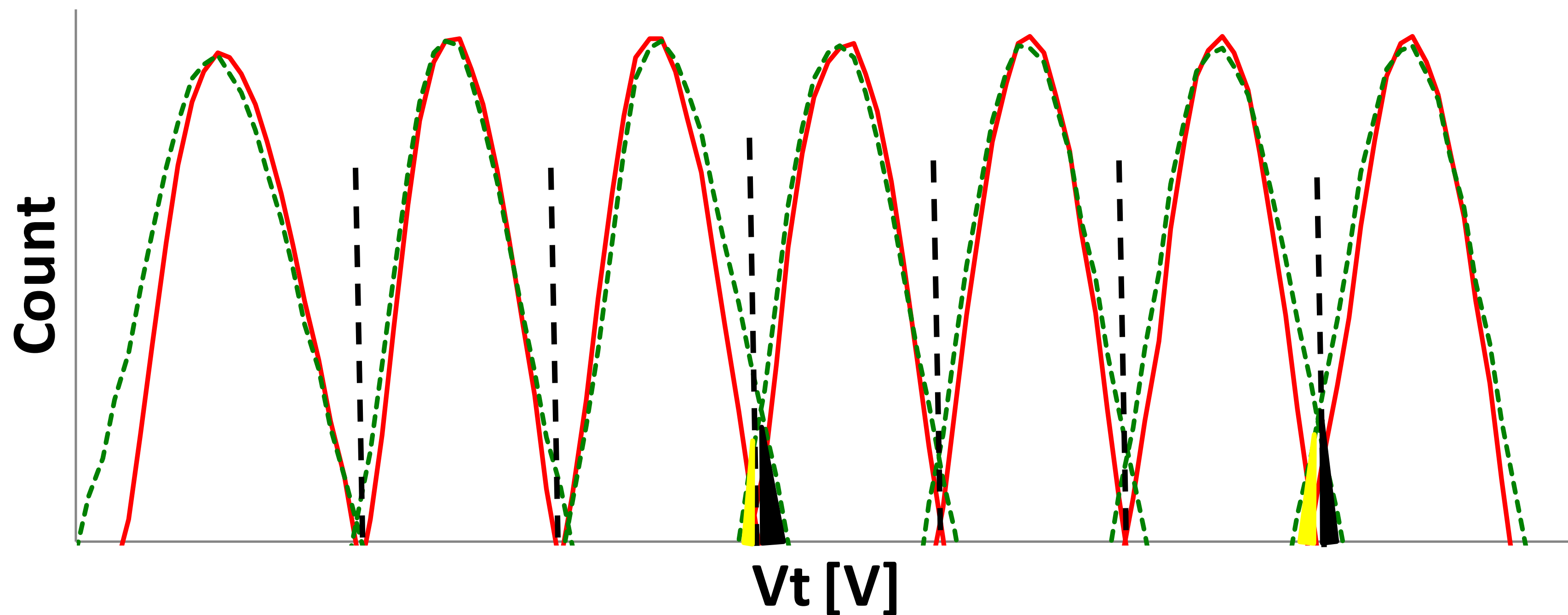
---**Cell to cell Coupling effects**

Temperature Cross Shift (TCS)



- When the X3 read levels are set at High Temp, there will be a lot of error bits when reading at Low Temp due to TCS

TCO Compensated



- After temperature compensation, the read error reduced by 75%

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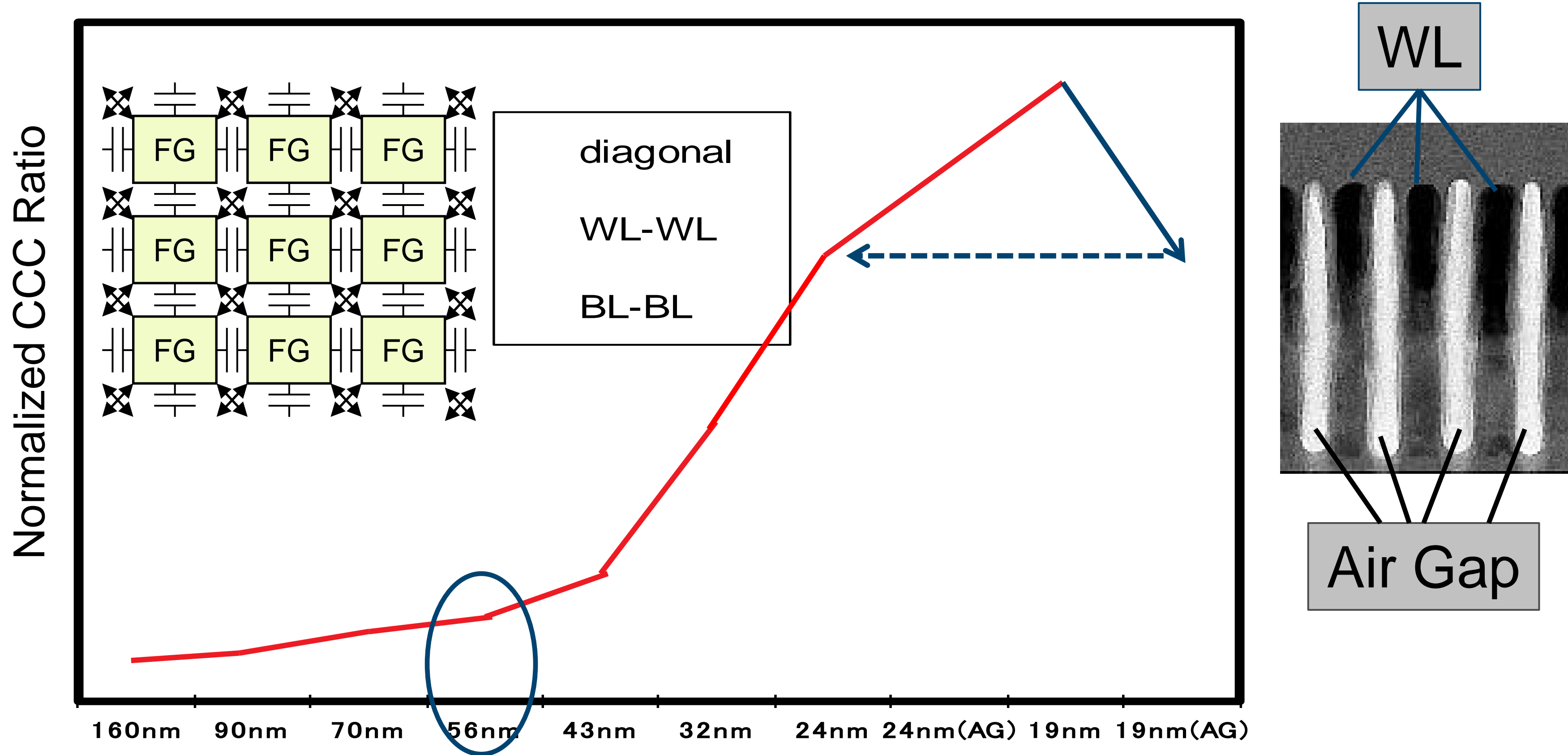
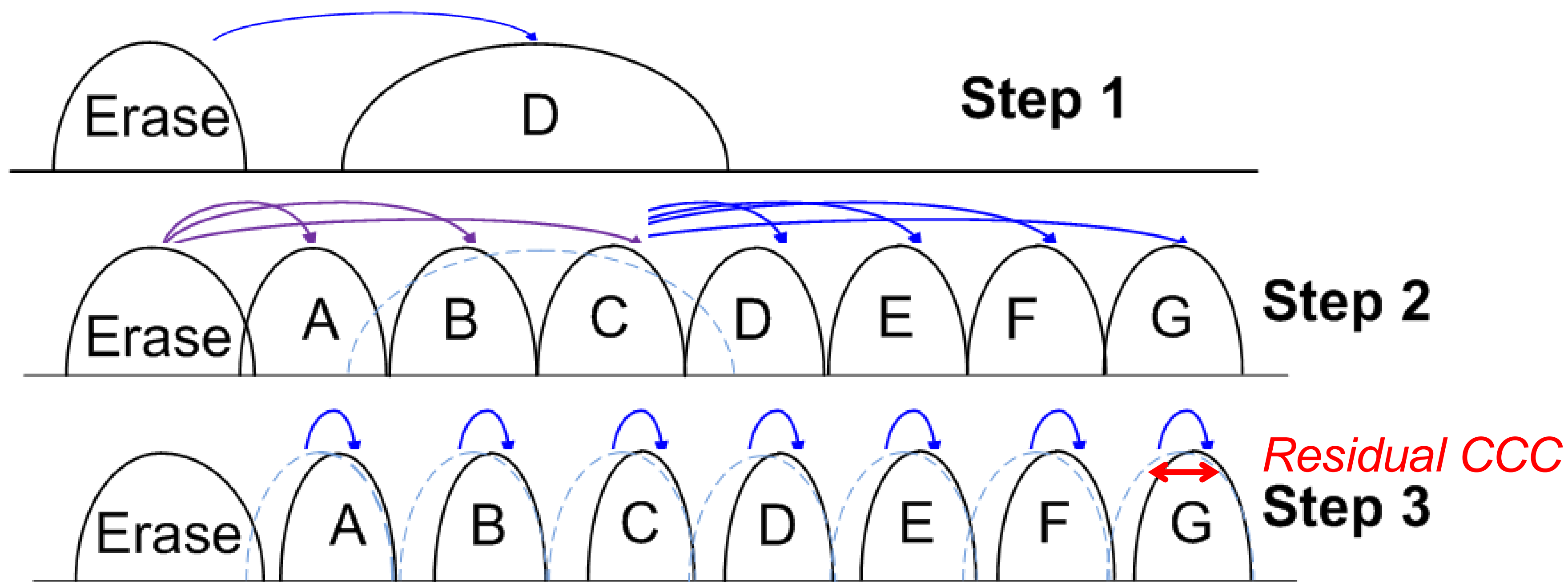
Cell-to-Cell Coupling (CCC) Trend



- With technology scaling, CCC increases dramatically
- Air Gap technology make the 19nm (AG) CCC equivalent to 24nm (no AG)~ 27% reduction

Three-Step Programming (TSP)



- Each WL programming consists of 3 steps:
  - **Step 1:** Binary program
  - **Step 2:** Coarse program
  - **Step 3:** Fine program
- Residual CCC (RCCC~final Vth movements) is 5%

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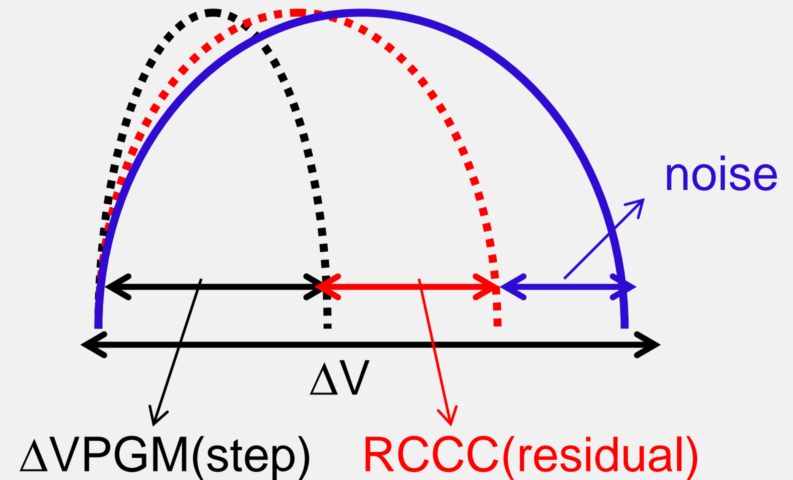
Factors Affecting Performance

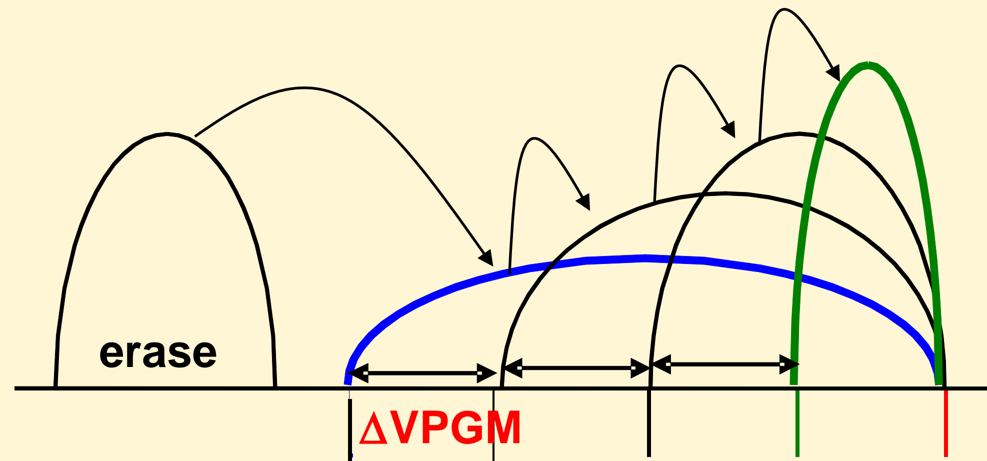
- The final cell Vth distribution width ΔV is determined by
  - ΔV = ΔVPGM(step)
    + RCCC(residual)
    + noise



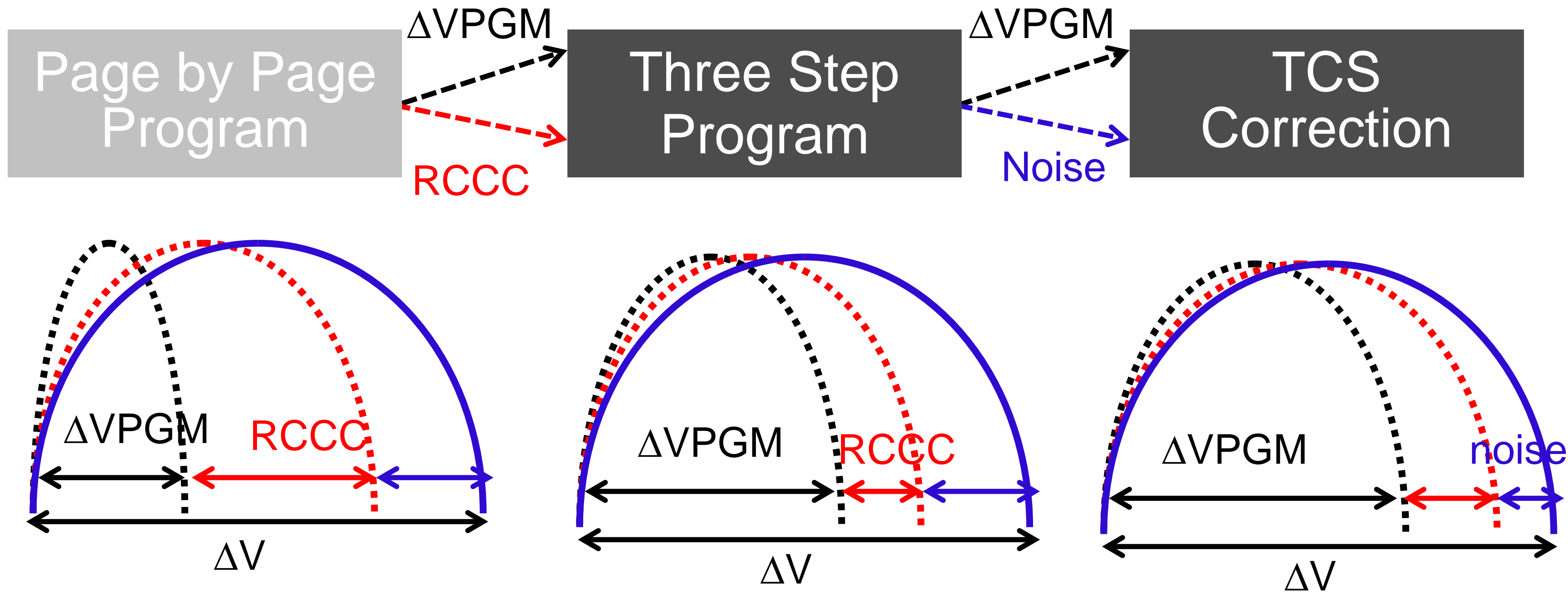
- Number of program pulse needed to finish program

  $NP = (V_G\text{-}Ver)/\Delta VPGM(step)$

  NP=number of program pulses



Performance Gain

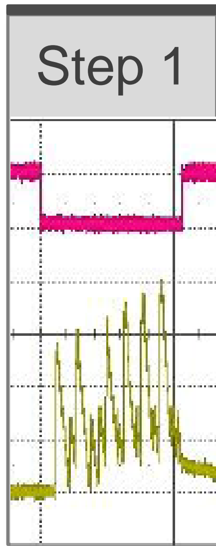


- The performance gain in 19nm X3 from the small residual CCC (RCCC) using TSP is 7% compared with 56nm X3 even though the CCC increased by 4.5 times
- Performance gain from precise TCO compensation is 5%

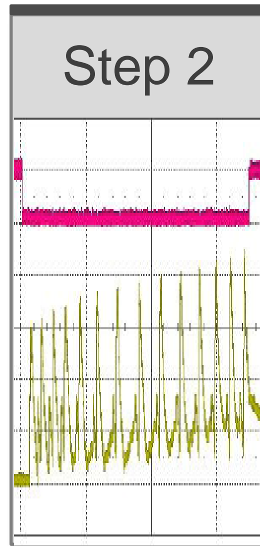
Performance for 19nm X3 128Gb

Selected WL Waveforms

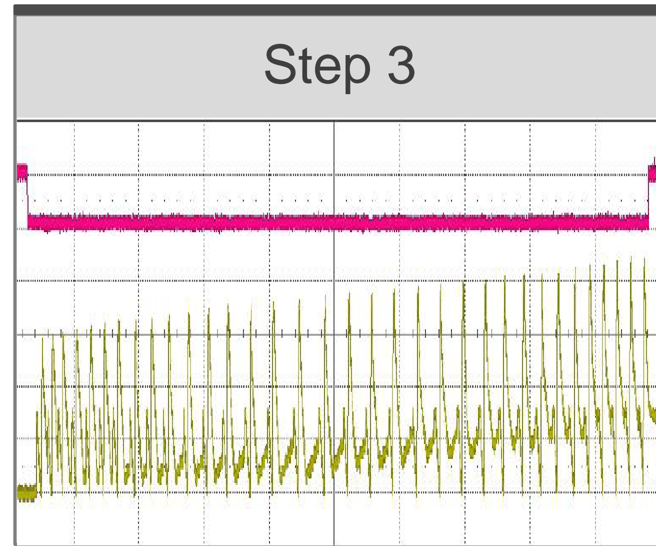
Step 1



Step 2

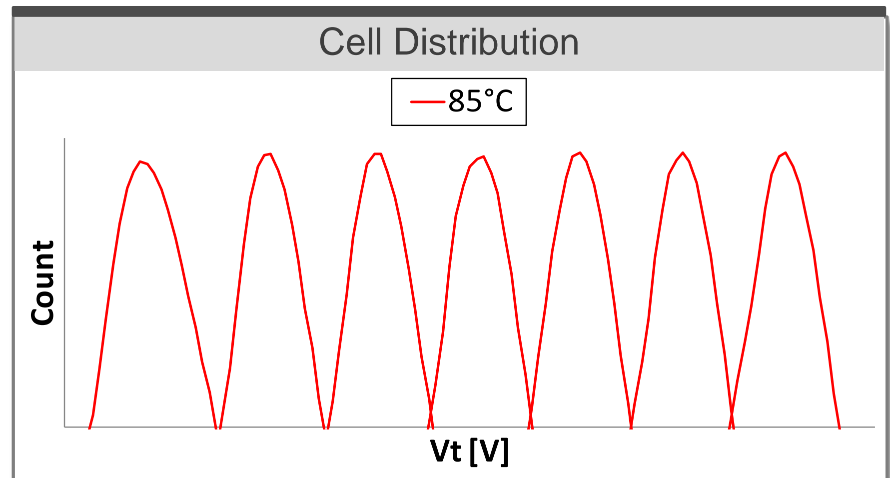


Step 3



- **18MB/s** with 2-plane (16KB x 2x3) programming
  - ABL is the main contributor to high performance
- Die Size **170.6mm²**

Cell Distribution



Raw Flash Capabilities vs. Market Requirements

Cost per Bit

Endurance

Sequential R/W

Vertical Integration between memory design and system management
→Enabling Applications of X3

24nm 2 bits/cell
19nm 2 bits/cell
19nm 3 bits/cell

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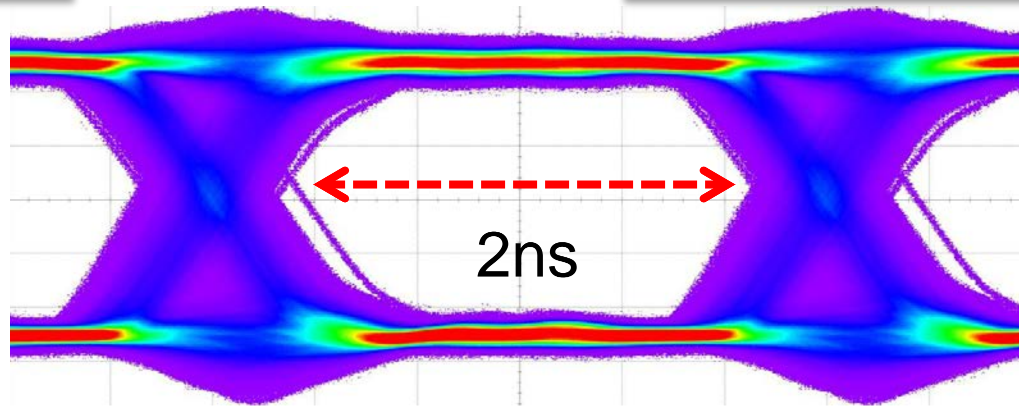
TM 400MB/s on 19nm X3 NAND

NAND (Toggle Mode)		Controller
DQS	↔	DQS
CE#	←	CE#
ALE	←	ALE
CLE	←	CLE
RE#	←	RE#
WE#	←	WE#
R/B#	→	R/B#
WP#	←	WP#
I/O[7:0]	↔	**I/O[7:0]**



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Conclusion

- 19nm 3 bits/cell is successfully manufactured
  - 3 bits/cell NAND flash still possible in deep sub 20nm NAND flash
- 3 Bits/cell provide cost benefit and small form factor
- High Speed IO interface can achieve 400MB/s which improve the system performance
- Tradeoff can be employed between ECC, Endurance and Performance
- Vertical Integration between memory and system enable X3 into many applications at SanDisk

Acknowledgments

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