Operation Algorithms of NAND Chips for SSDs

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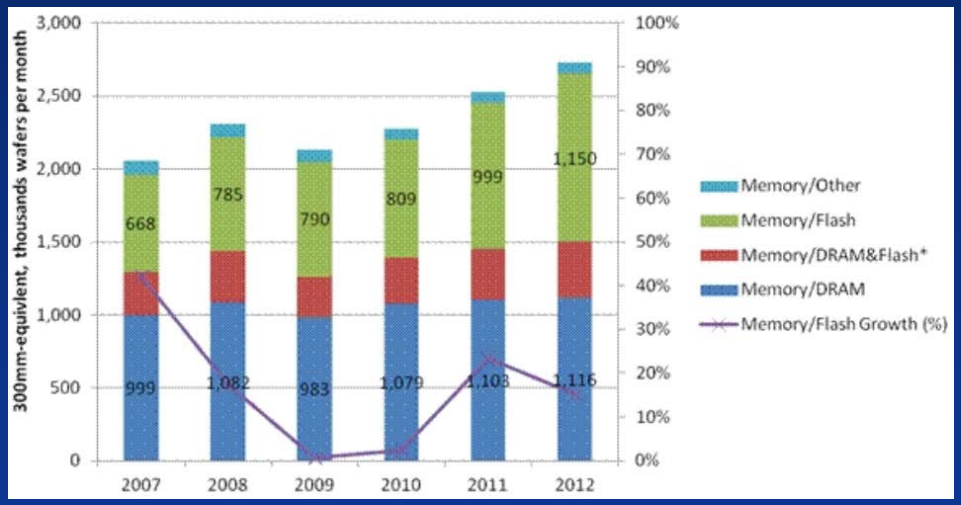
NAND Flash Trend

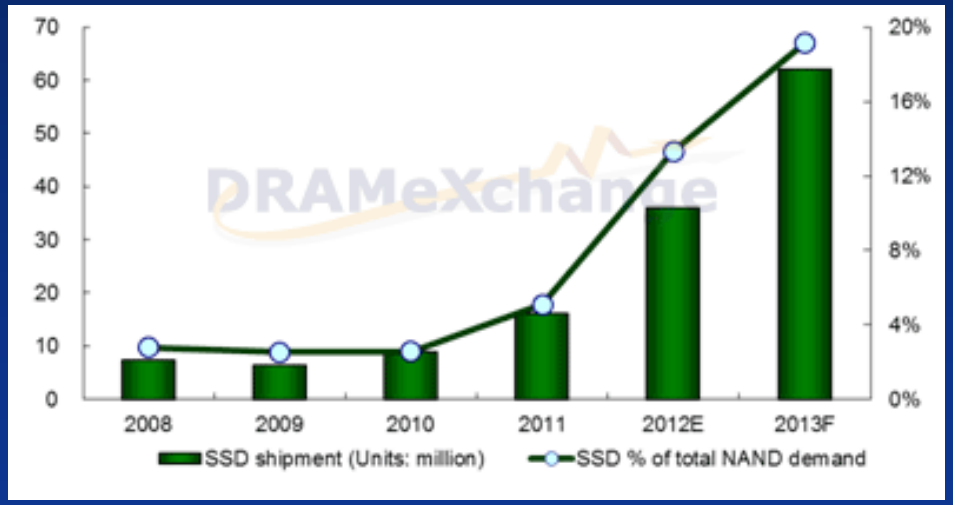
- *NAND portion in memory market grows up!*
- *Memory density increases along with SSD boom from 2011*

WW market share of NAND Flash in memory



Source: *http://www.semicon.org*

SSD market forecast

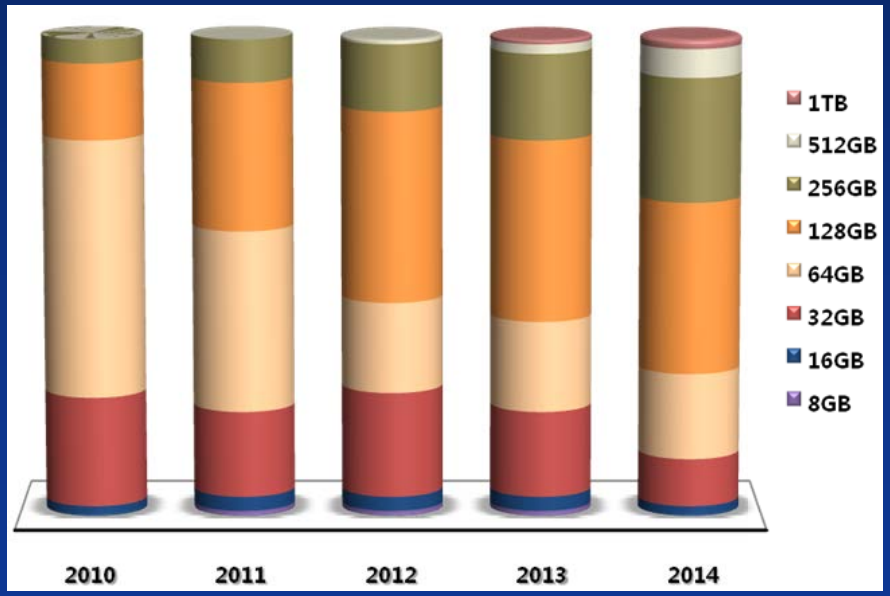


Source: *DRAMeXchange, Jan., 2012*

Density trend of SSD and NAND Flash

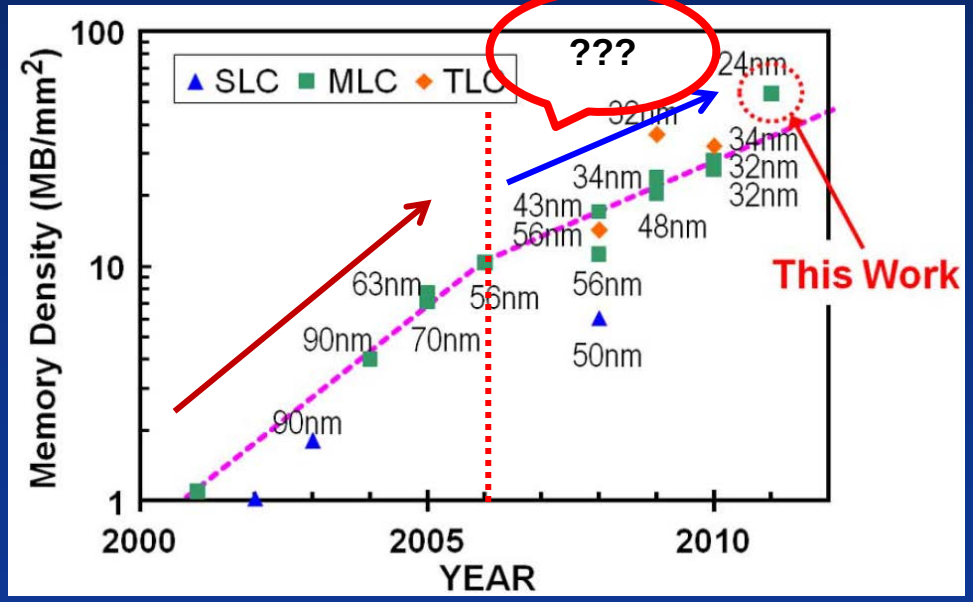
- *Drop in NAND price increases SSD adoption rate, thus increasing demand for higher density SSDs.*
- *The growth of memory density goes down since 2006 ← Difficulties for scaling down*

Mobile PC SSD Density Trend



Source: ***SK hynix marketing***

Memory density trend of NAND Flash

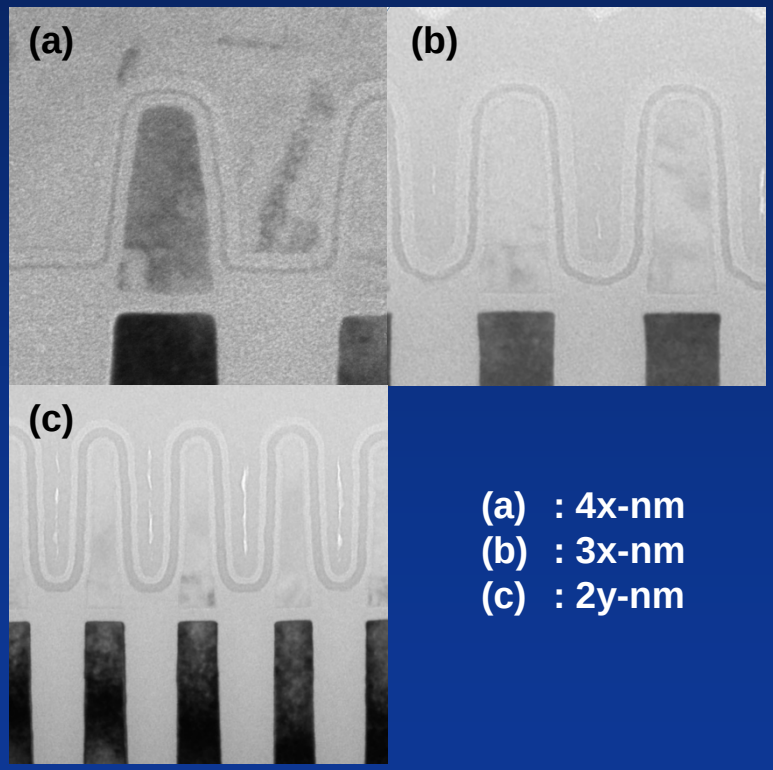


Source: ***K. Fukuda, et al., ISSCC vol. 47, pp. 75-84, 2012***

Challenges in Scaled Down

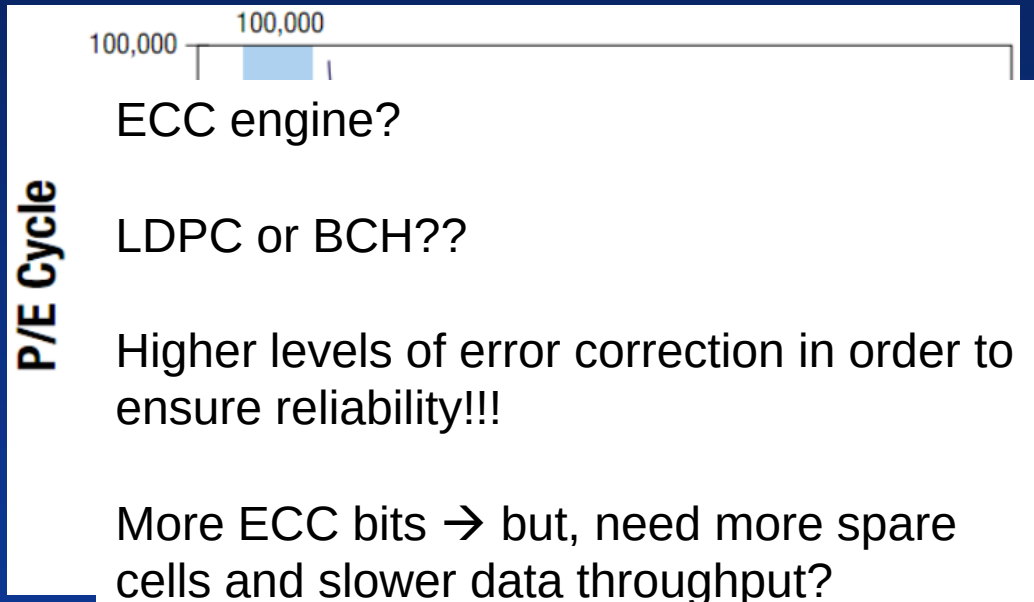
- *As technology node shrinks, endurance characteristics are degraded and ECC requirements are increased. → Cell properties should be improved.*

TEM images with various technology nodes



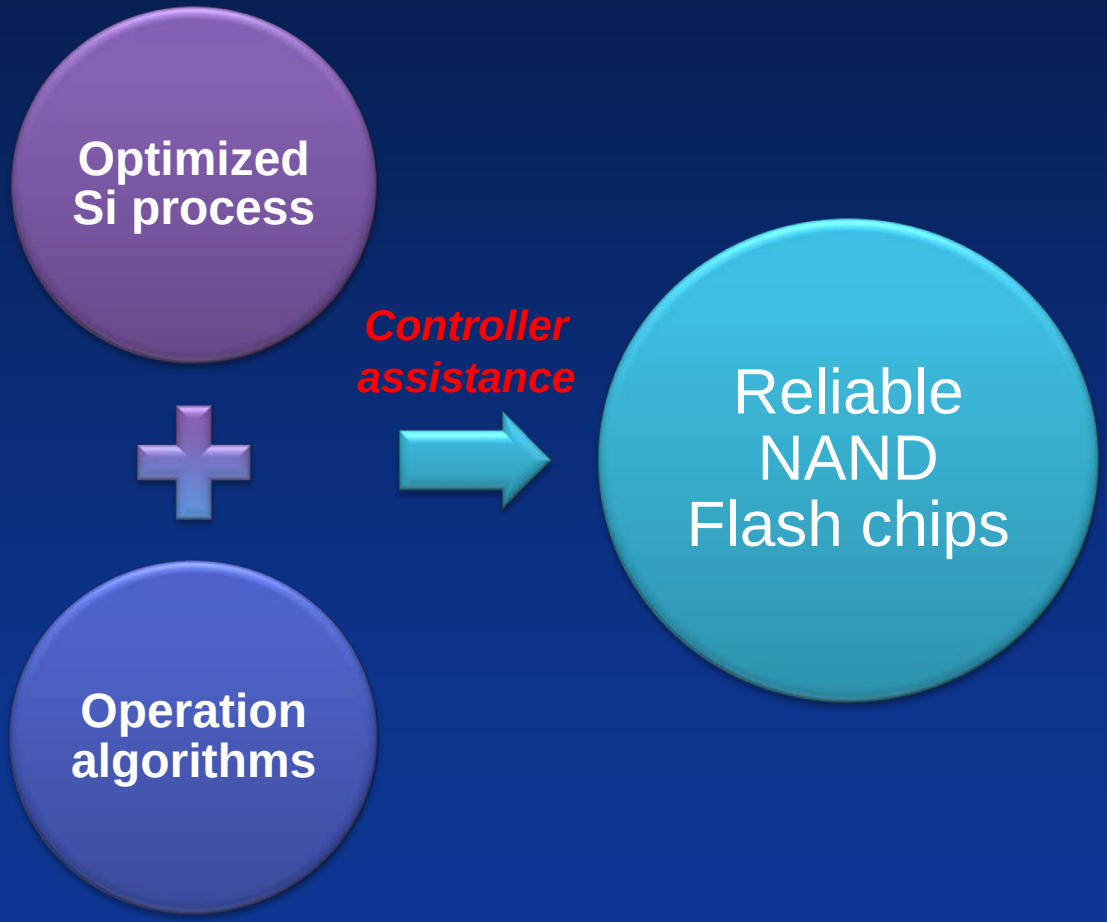
(a) : 4x-nm
(b) : 3x-nm
(c) : 2y-nm

A life cycle and ECC comparison of NAND Flash



Source: JMicron, Western Digital, Morgan Stanley Research

How can we improve NAND performance?



- *Optimized Si process*

→ To obtain narrow Vth distribution with newly adopted Si process

- *Operation algorithms*

→ Vth adjustment considering with original cell properties.

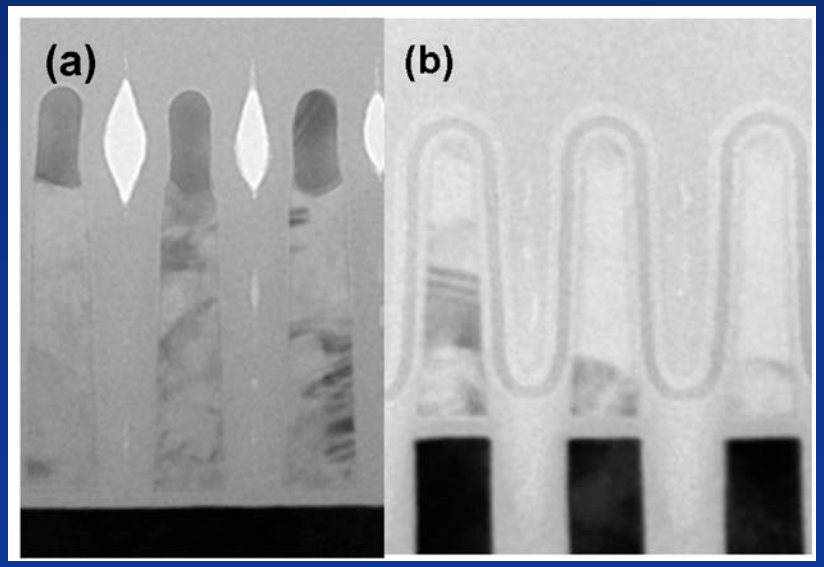
- *Controller assistance*

→ Wear-leveling, retention/read refreshment, garbage collection and etc.

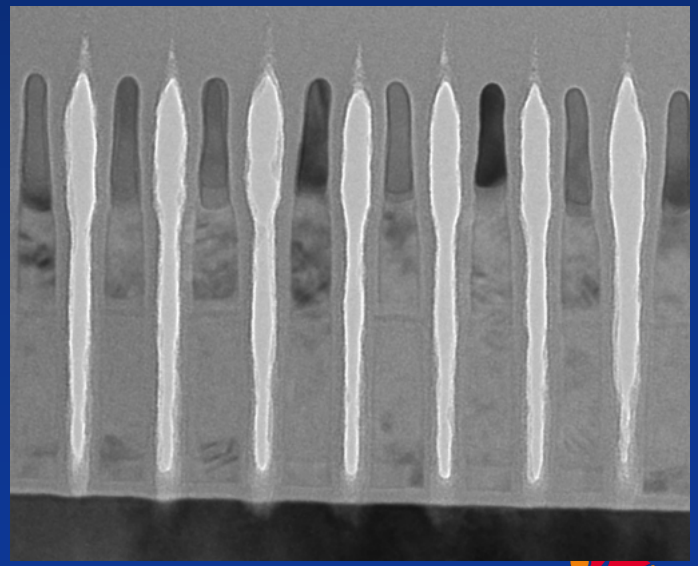
Physical structure of NAND chips

- *MLC and TLC NAND Flash memory devices are fabricated with 3x-,2x- and 2y-nm technology.*
- *Optimized Si process conditions to minimize cell distributions and improve endurance characteristics .*

Cross-sectional TEM images of 2x-nm NAND Flash chips

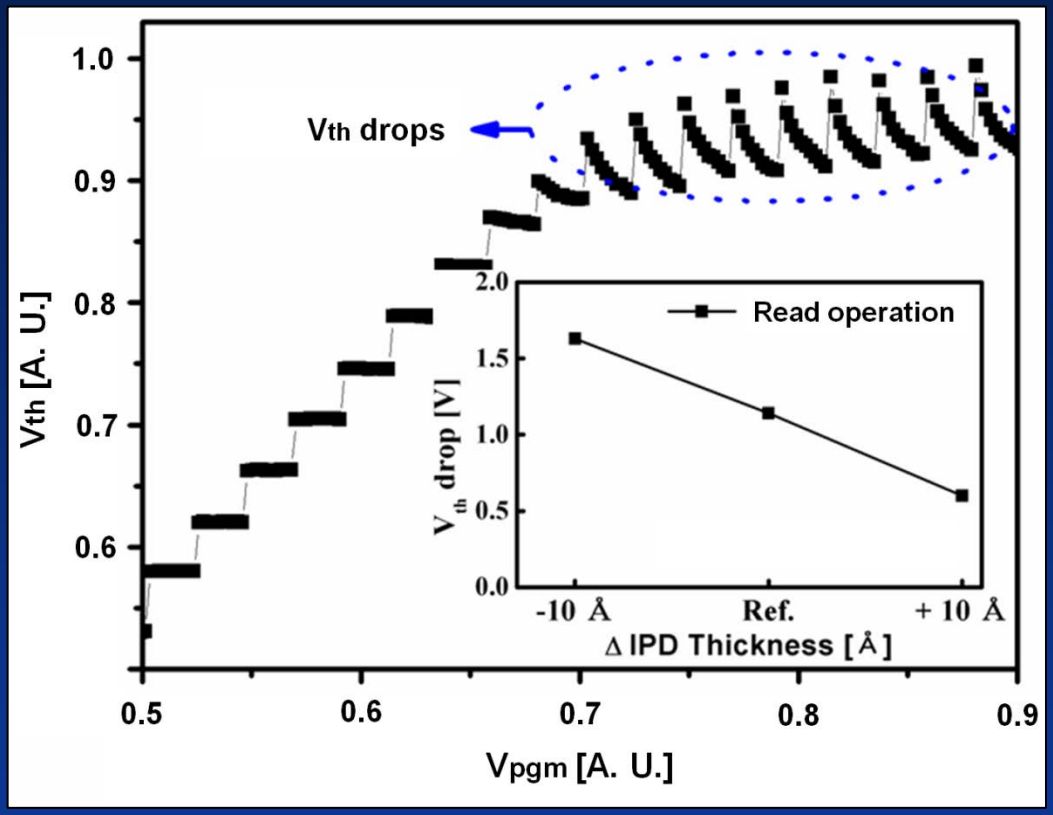


An TEM image of air-gap between WLs with NAND chips



Electrical characteristics of NAND chips (1)

Vth characteristics as a function of Vpgm



The inset figure shows Vth drops during read operation with various IPD thickness

- *Saturated Vth*

→ *Leakage current between the F/G and C/G through the IPDs.*

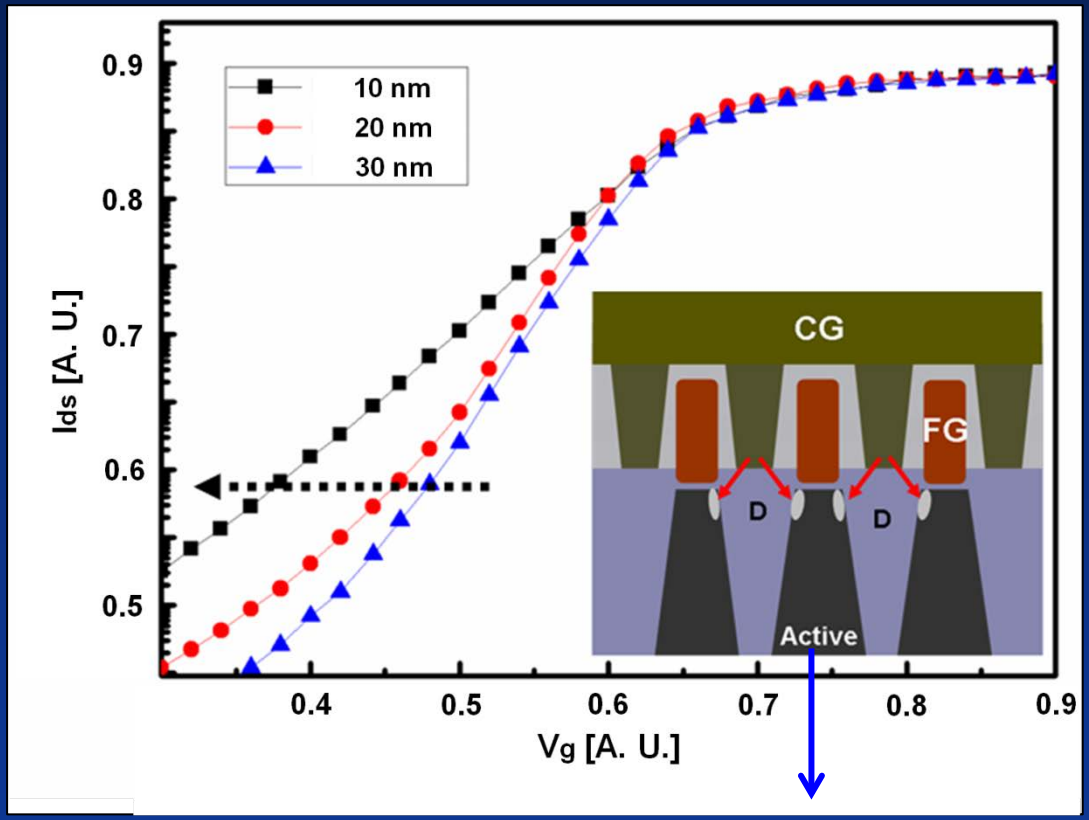
- *Thin vs. thick IPDs*

→ *more leakage current through IPDs and decrease of cell Vth.*

→ *Thickness of IPD layers should be optimized to prevent Vth drops.*

Electrical characteristics of NAND chips (2)

I-V curves with various EFD
(Electrical Field Distance, distance between C/G and active layer)



A schematic diagram of inversion at the edge of the active area.

- *Lower EFD*

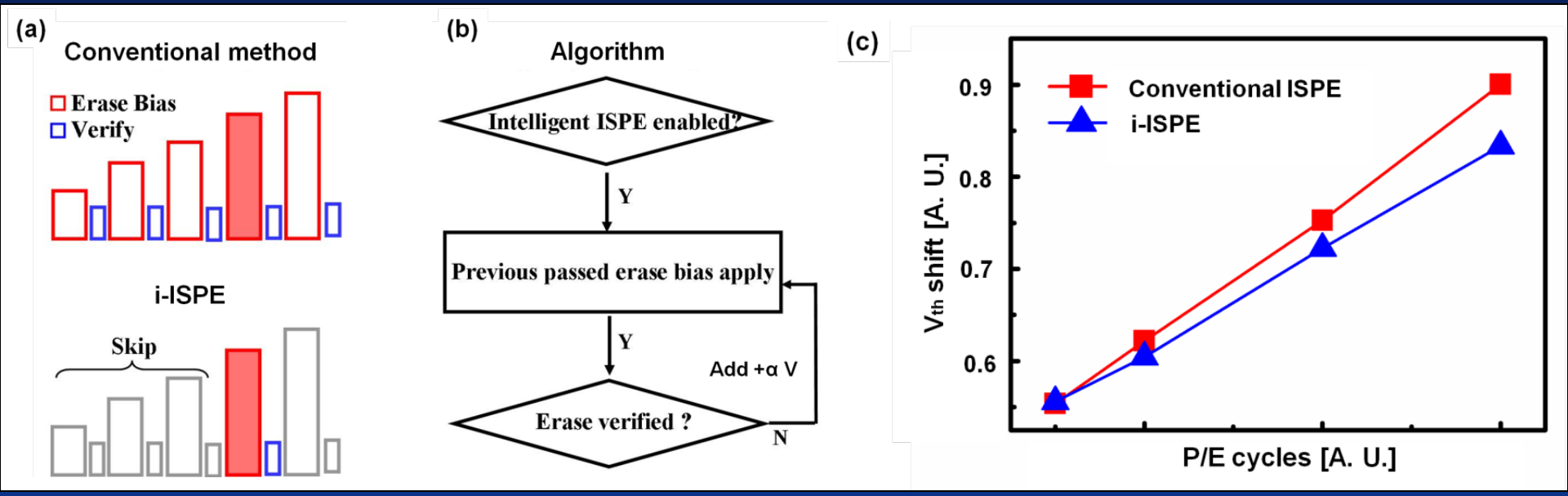
→ *CG directly affects the edge area of the active layer during cell operation*

→ *Also decrease the programmed V_{th}.*

→ *It is very important to optimize the doping concentration of the active area and EFD.*

Operation algorithms (1)

Schematics diagram, state-machine and electrical properties of conventional ISPE and i-ISPE .

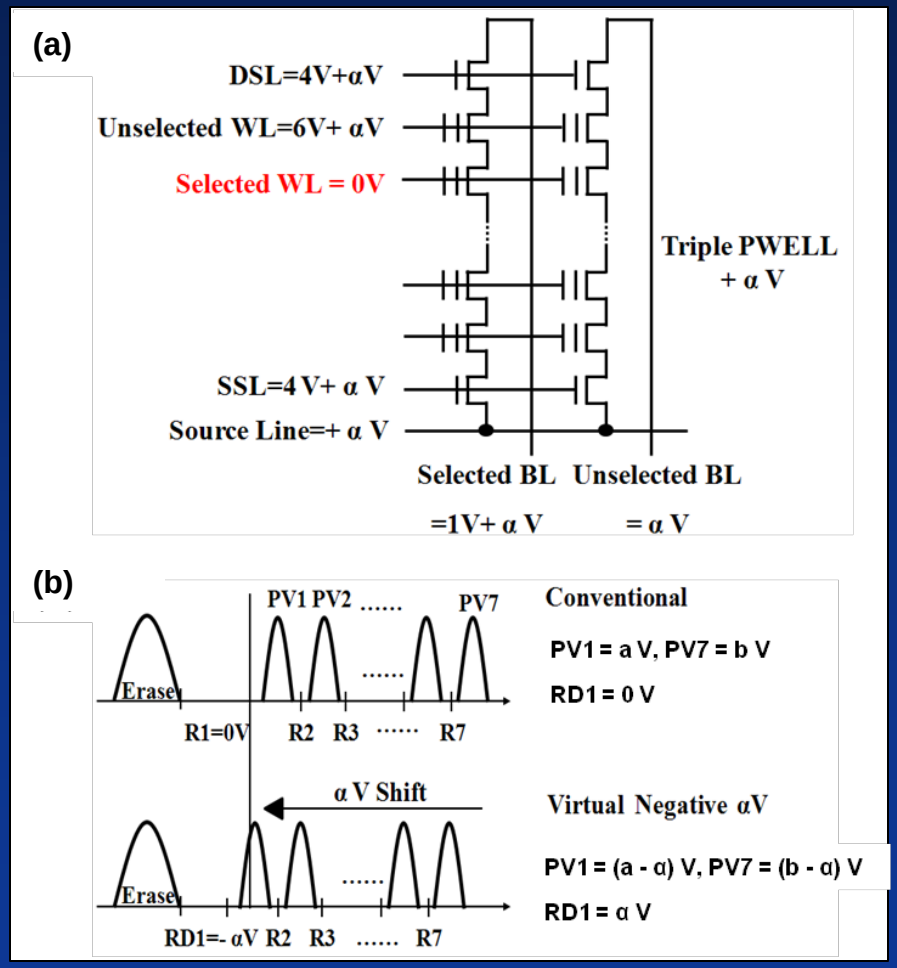


- *Elimination of the redundant erase stress with i-ISPE.*

→ *Erase operation can be finished within only one or two pulses after P/E cycles.*

Operation algorithms (2)

A VNR scheme (a) and Vth shift with VNR operation (b)



- *A VNR scheme*

→ Bias voltages applied source and bulk.

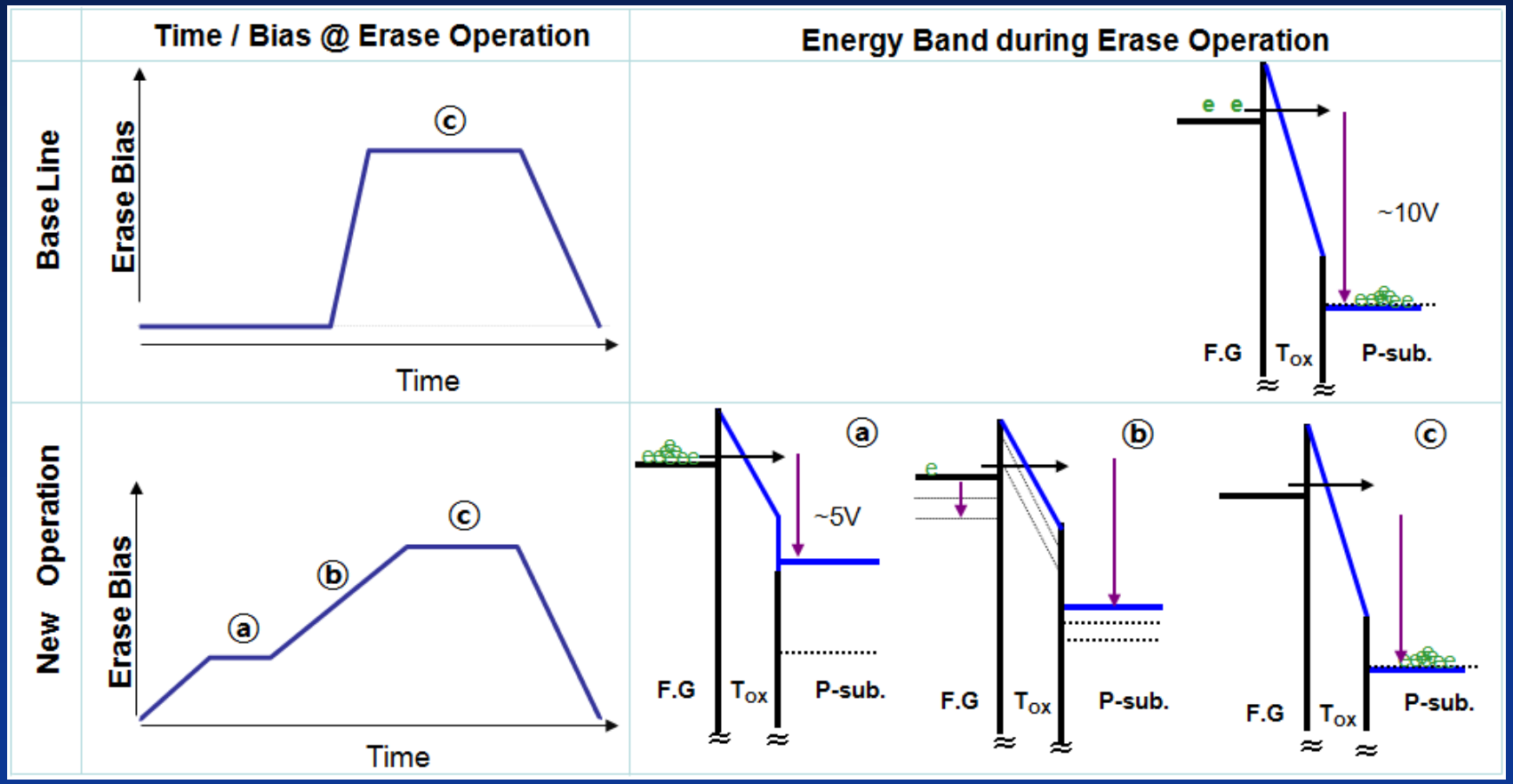
→ Cell V_{th} is virtually sensed higher than real programmed level.

- *Advantages*

→The burden of highest programmed state such as charge loss, program disturbance and interference, can be relieved.

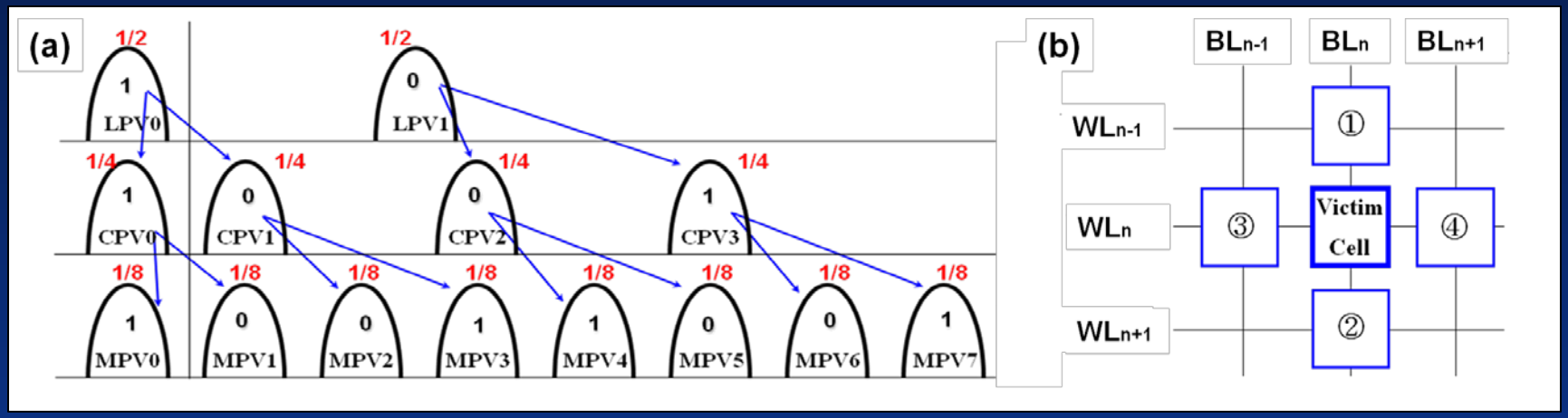
Operation algorithms (3)

Erase operation bias control and optimization



Operation algorithms (4)

Schematic diagram of data randomization process V_{th} distribution



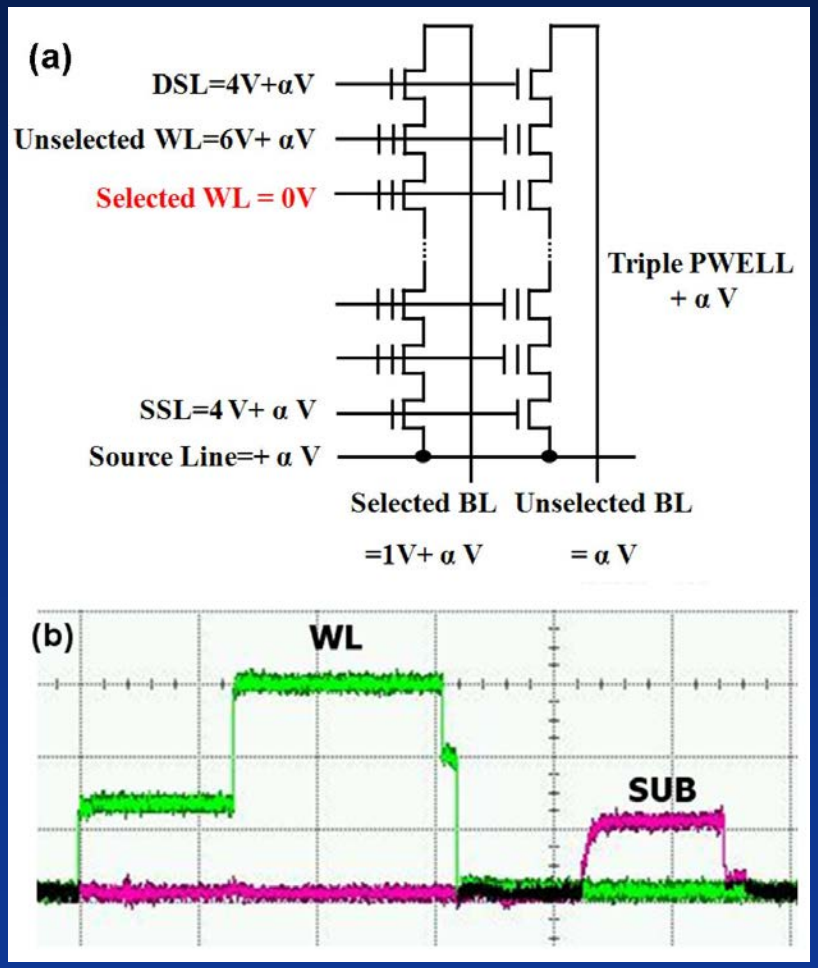
- *To reduce the interference to victim cell.*

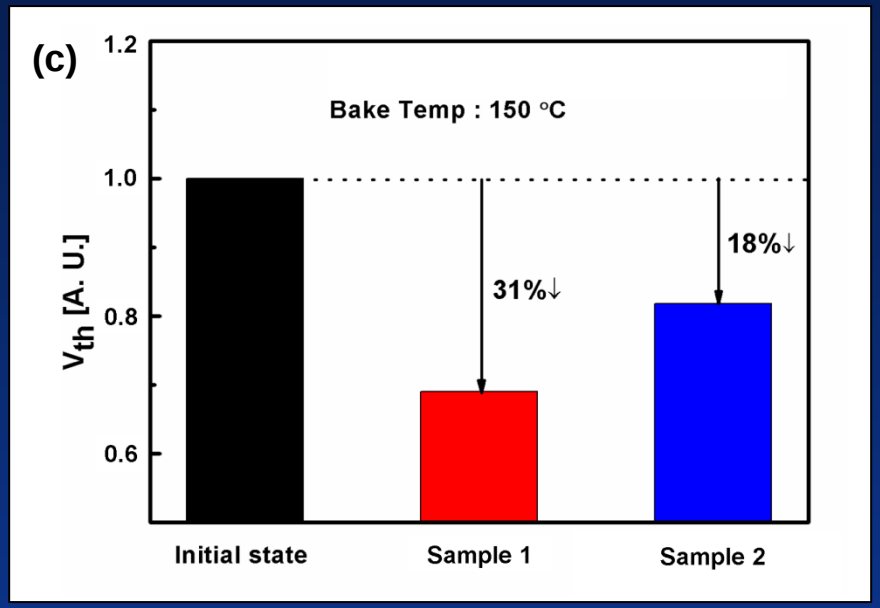
→ *Programmed level of neighboring cells should be considered.*

- *The drastic V_{th} difference between victim and neighboring cells should be avoided to minimize the interference effect.*

Operation algorithms (5)

Detrapping operation during program/erase



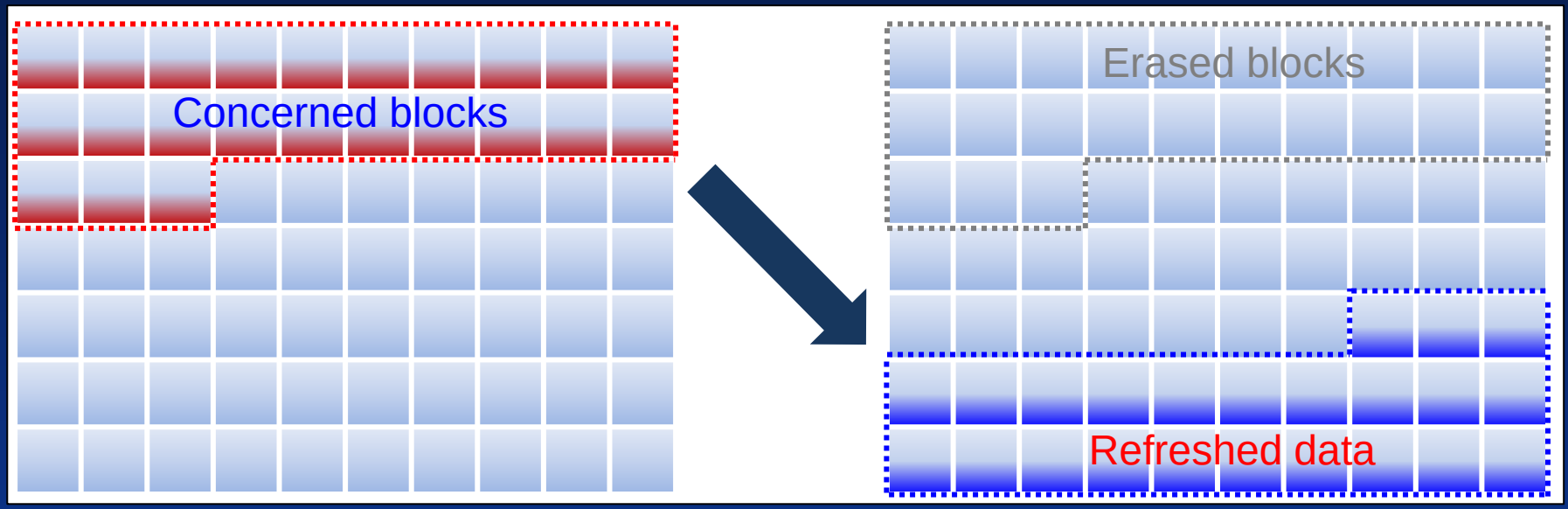


- *An improvement of retention characteristic.*

→ *Life span of NAND Flash is prolonged without more ECC bits due to the specially proposed operation algorithm.*

Controller assistance (1)

Retention & disturbance refreshment operation

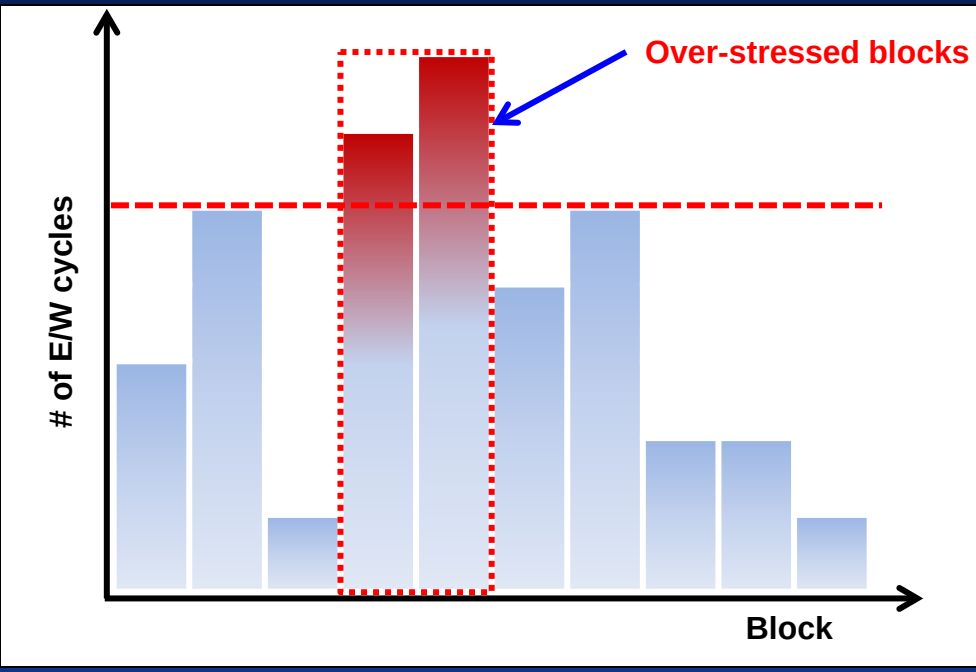


- *Some blocks can be accessed continuously or remained for a long time without P/E and read operation. → Unwanted errors are increased!!!*

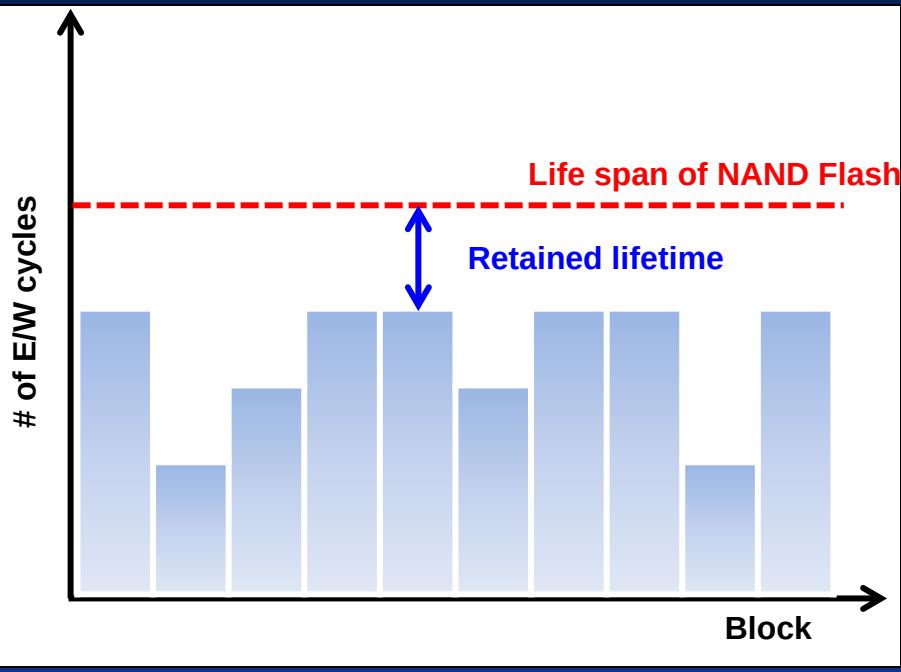
- *To avoid uncorrectable errors over ECC capability, data in these blocks are moved toward other blocks.*

Controller assistance (2)

Without wear-leveling



With wear-leveling



- *Wear leveling technique*

→ *To prolong the lifetime of application devices based on NAND Flash with programming /erasing each block evenly. (Dynamic or static ???)*

Conclusion

- *In this presentation, we show challenges and limitations of NAND flash memory devices based on floating gates for SSDs.*

- *Thickness of IPD layers, EFD and the doping concentration of active area are critical factors to overcome those ones.*

- *Various operation algorithms and controller-assisted NAND management are also introduced for enhancing reliability characteristics.*

- *With these schemes, MLC and TLC NAND flash memory devices can achieve endurance properties for SSDs beyond technology shrinkage.*