19nm 112.8mm^2 64Gb Multi-level Flash Memory with 400Mb/s/pin 1.8V Toggle Mode Interface

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Outline

- Introduction to 19nm 64 Gbit MLC NAND (400 Mb/s/pin interface)
- Chip Architecture for Small Die Size
- MLC Programs Techniques
- New Features(Read-Latency Reduction)
- Summary of Key Features
- Conclusion

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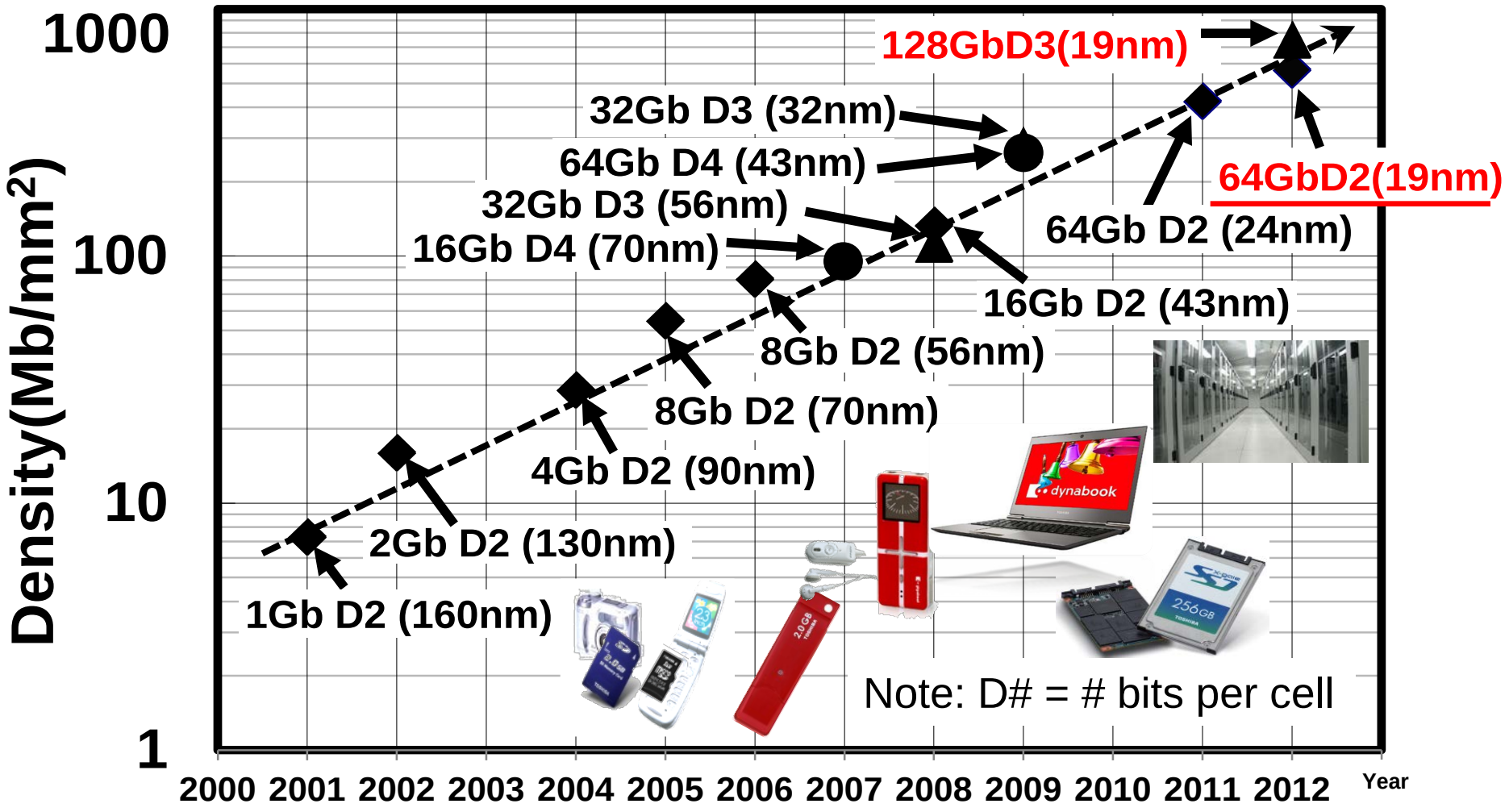
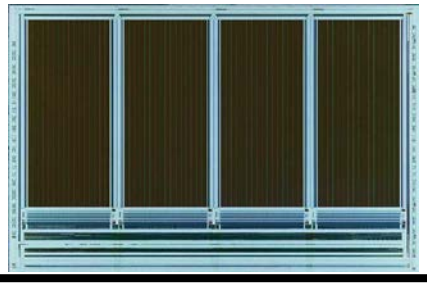
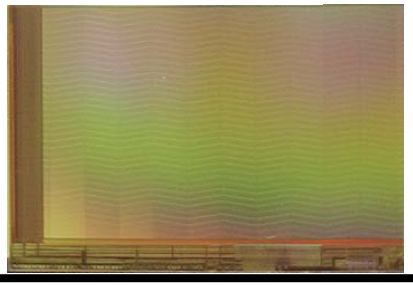
NAND Flash Density Trend



- Since first 160nm 1Gb MLC was commercially introduced in 2001, Memory Density has expanded by over **100 times**

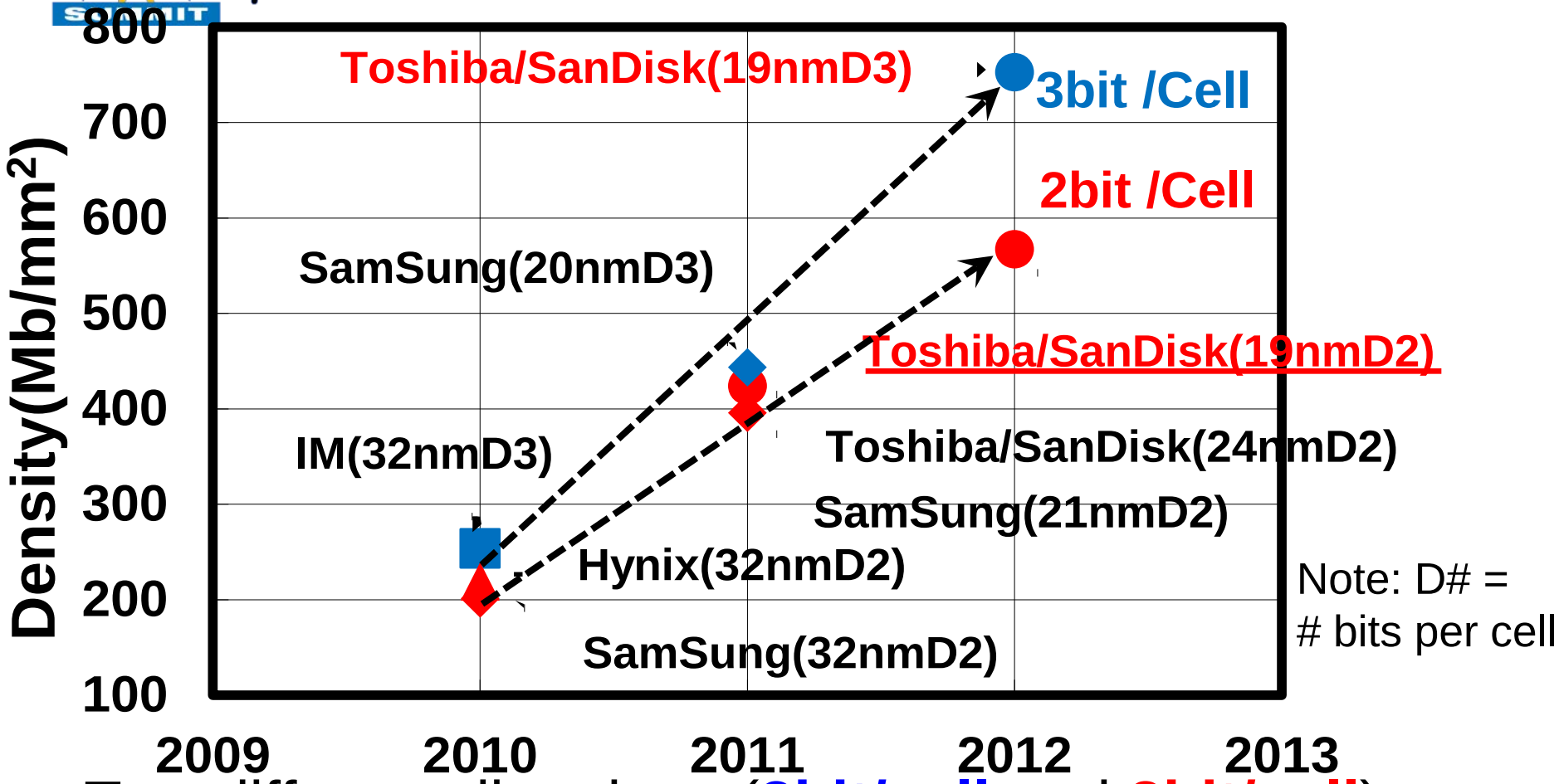
Comparisons of first 1Gb MLC and latest 64Gb MLC





Technology	160nm	one-ninth	19nm
Density	1Gb	64 times	64Gb
Die Size	137mm^2		112.8mm^2
Mb/mm^2	7.5	80 times	581
Architecture	Conventional Even / Odd		All-Bit-Line(ABL)
SA configulation	Both Sided		Single Sided
Program unit	2kB (= 512B x4Plane)	8 times	16kB (=16kB x1Plane)
tProg	1.1ms		1.1ms
Prog. Perform.	1.9MB/s	8 times	15MB/s
Burst Cycle Time	20Mb/s/pin(50ns)	20 times	400Mb/s/pin(2.5ns)
Year	2001	10 years	2011

Comparisons of 3bit /cell and 2bit /cell



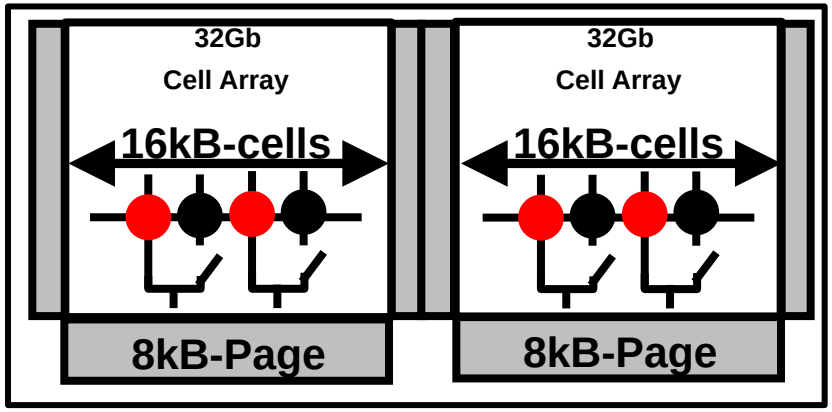
- Two different directions (**3bit/cell** and **2bit/cell**)
  - 3bit/cell enables highest Mb/mm²
  - 2bit/cell offers better **performance and reliability**

Outline

- Introduction
- **Chip Architecture for Small Die Size**
  - **Single-Array Configuration**
  - **One Sided All-Bit-Line(ABL) Architecture**
  - **High Speed Toggle Mode Interface**
- MLC Programs Techniques
- New Features(Read-Latency Reduction)
- Summary of Key Features
- Conclusion

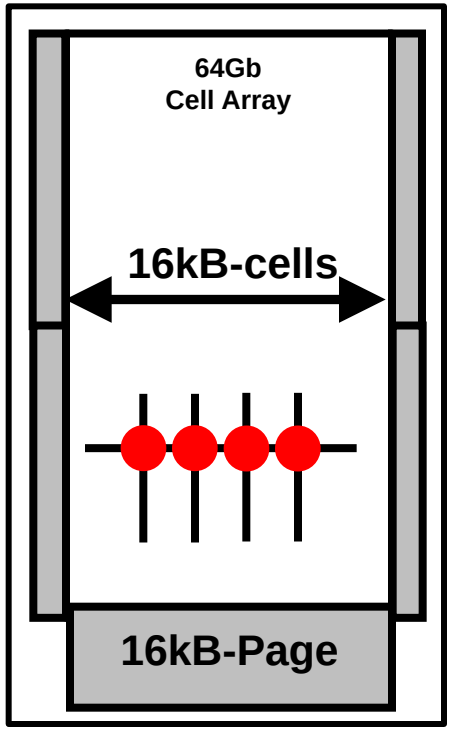
Single Array Configuration

Conventional Evne / Odd Architecture



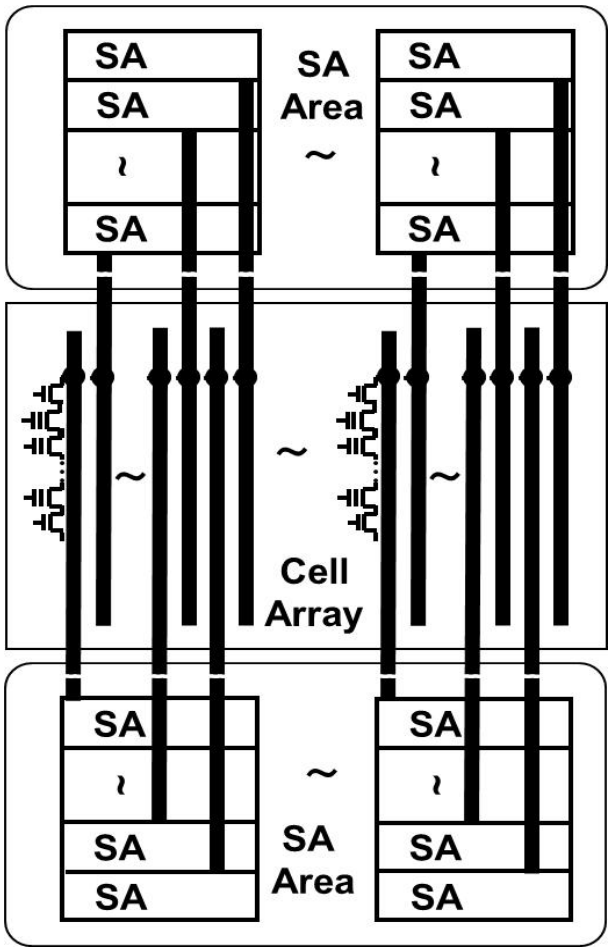
2-Plane array configuration

All-Bit-Line (ABL) Architecture



Single array configuration
⇒ Small Die size

Two-Sided Sense Amp Architecture

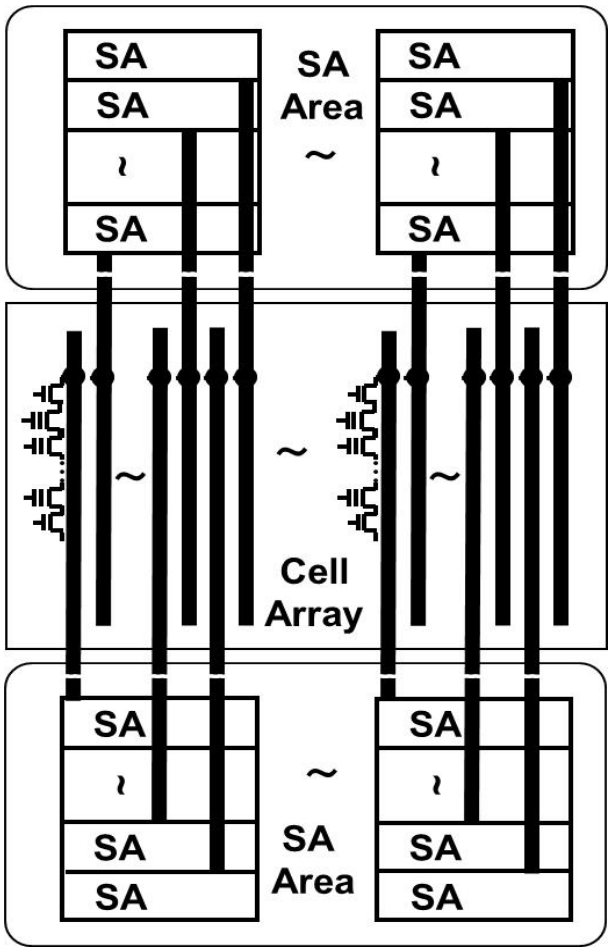


- Half of SAs are placed on each side of the array due to complexity of SA layout.

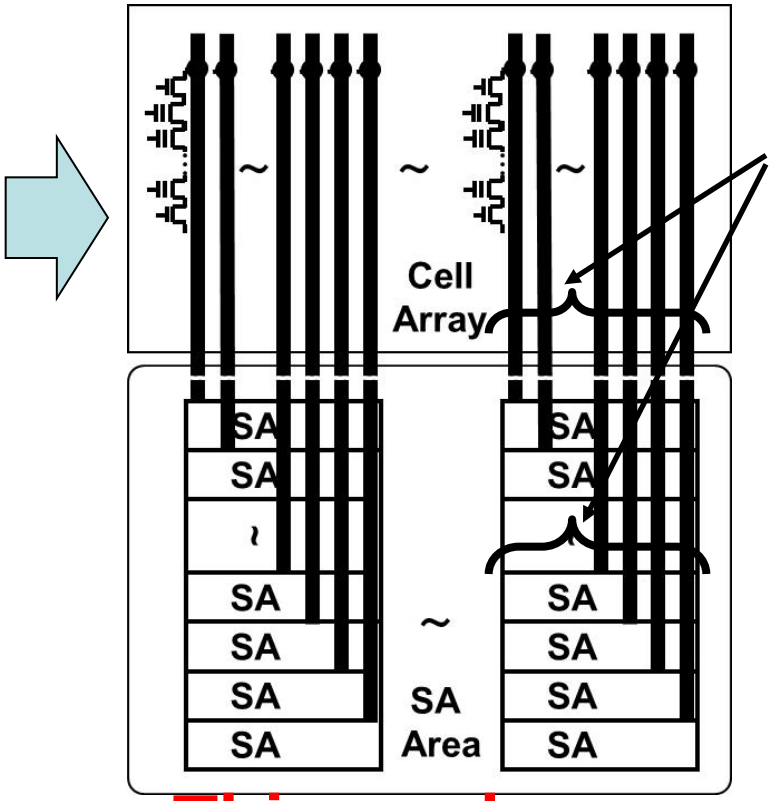
Conventional Two-sided SA

One Sided ABL Architecture

- Same Metal pitch in SA as BL pitch
- Spacer patterning process

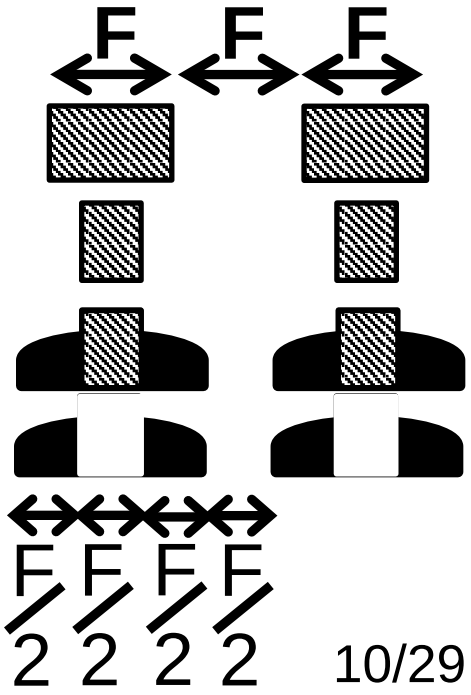


Conventional Two-sided SA



This work One-sided SA

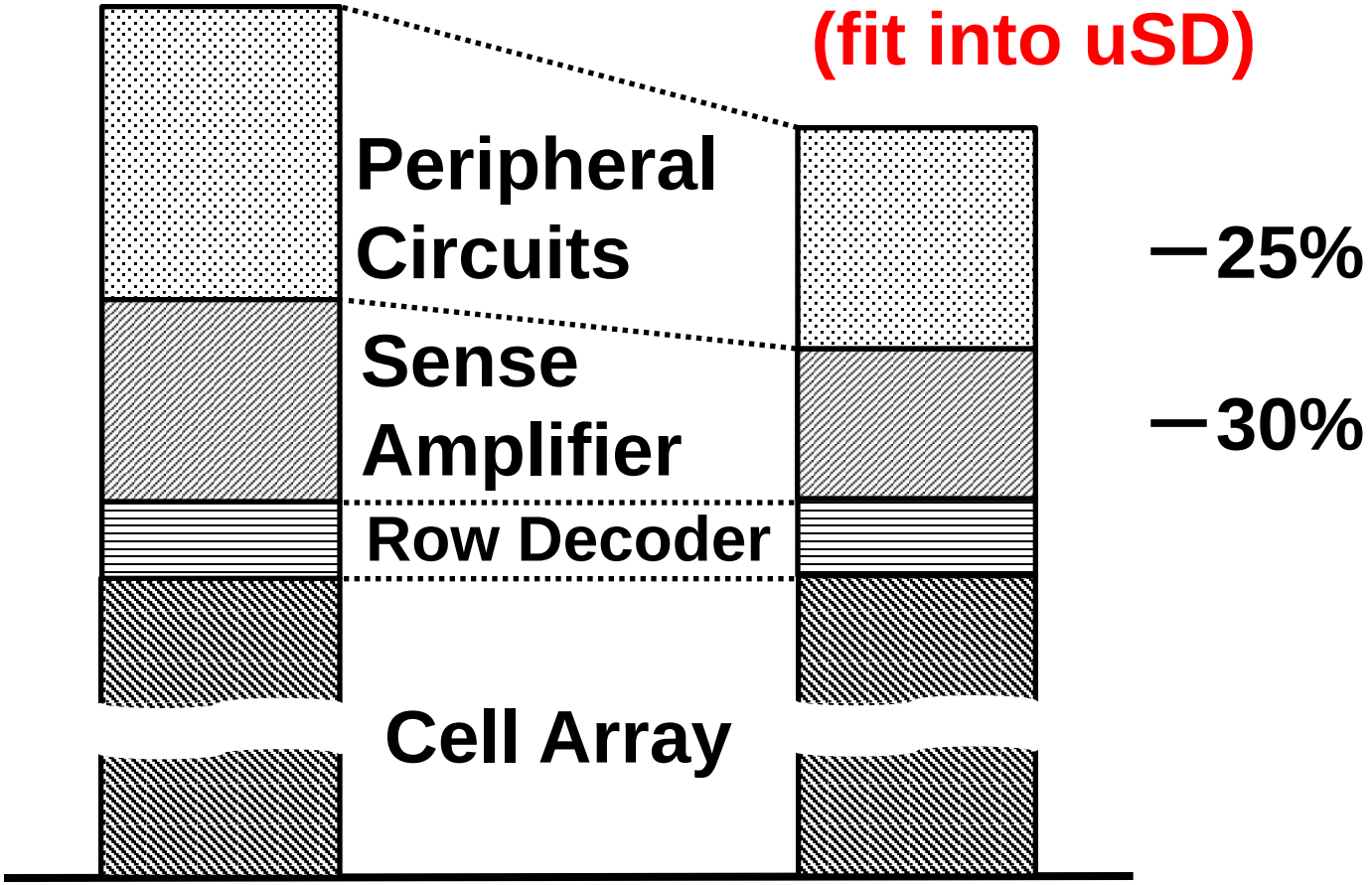
Same Metal pitch



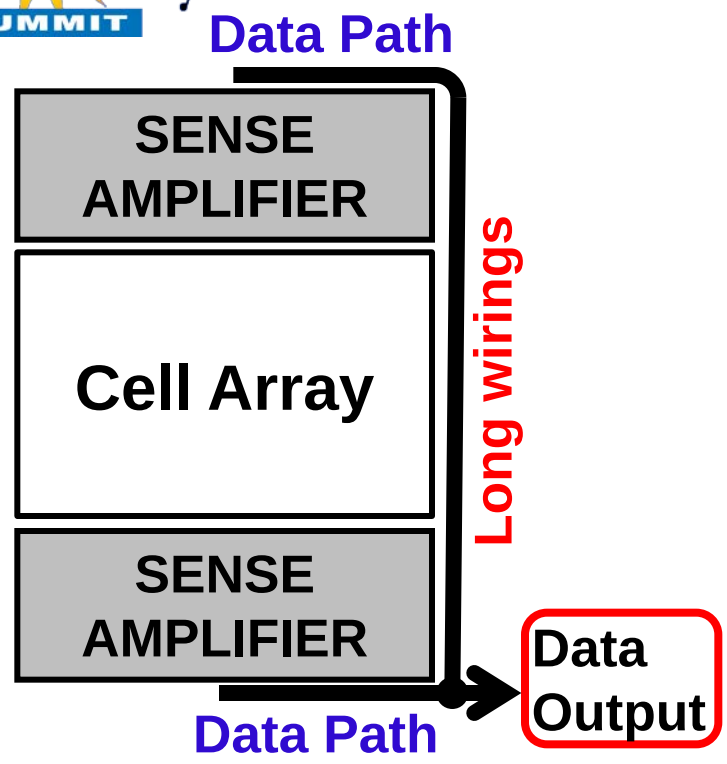
Die Size Reduction

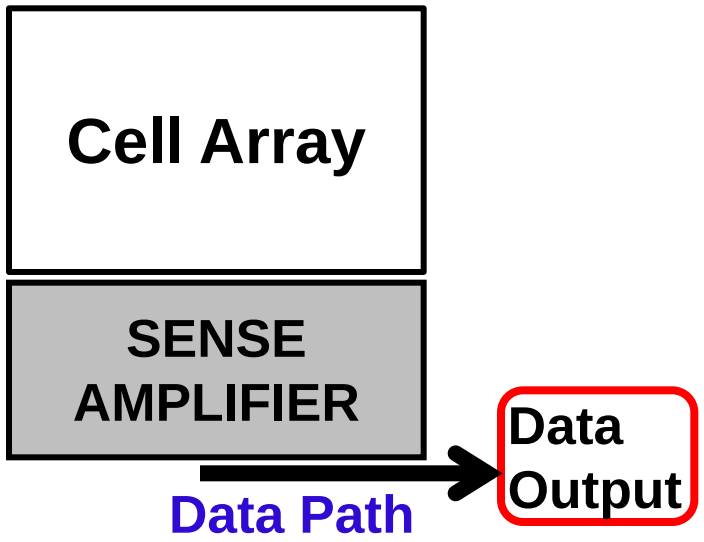
117.3mm²(100%) ⇨ **112.8mm²(94%)**

(fit into uSD)



High Speed Toggle Mode Interface



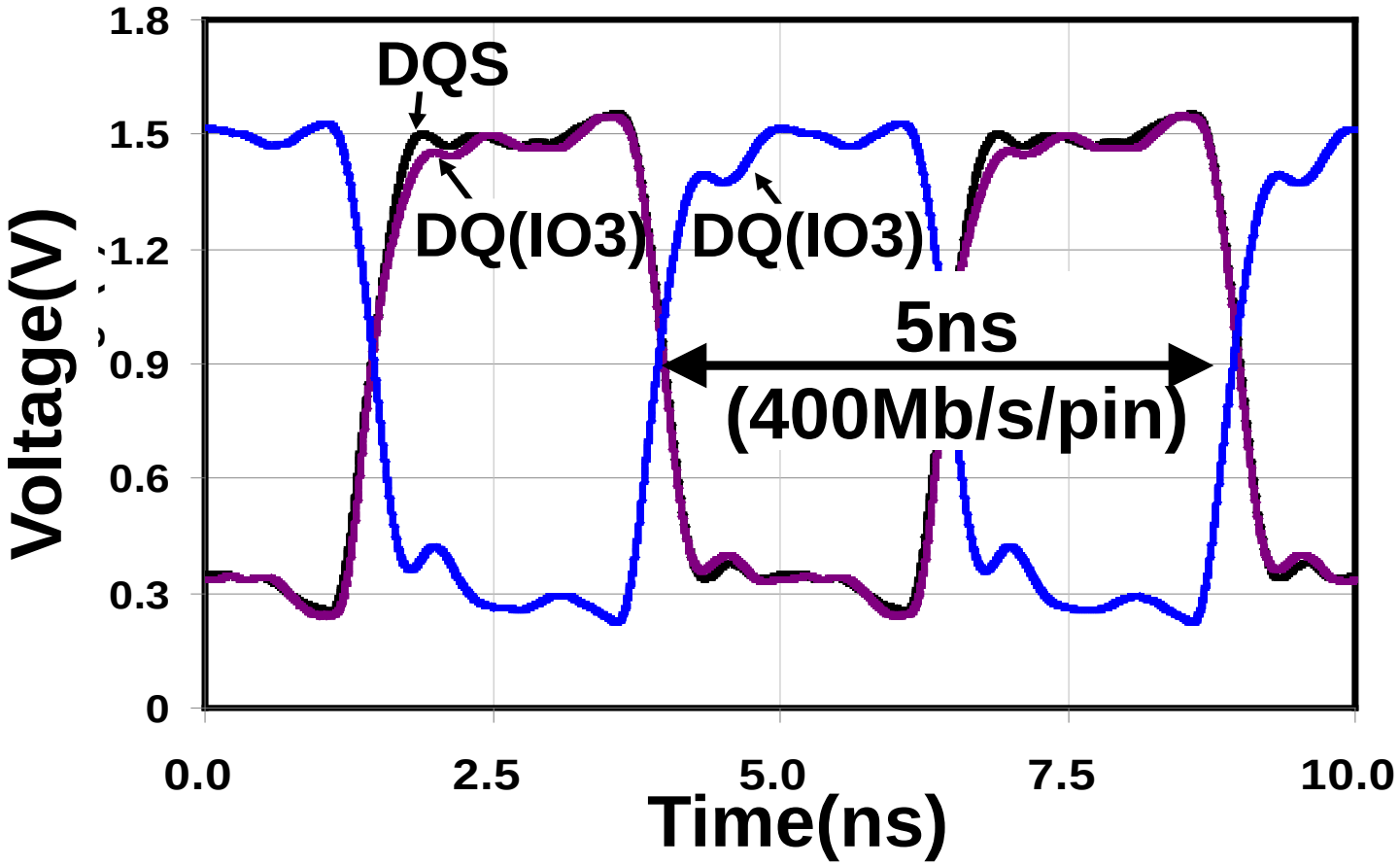


Conventional
Two-sided sense amplifier

This work
One-sided sense amplifier

- **Minimized signal delays**
- **Lower power consumption**

Measured Data Output Eye-Diagram



- **400Mb/s/pin@1.8V high-speed toggle mode interface is achieved!**

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- **MLC Program Techniques**
  - **Bit-Line Bias Acceleration (BLBA)**
  - **BC-States-First Program Algorithm**
- New Features(Read-Latency Reduction)
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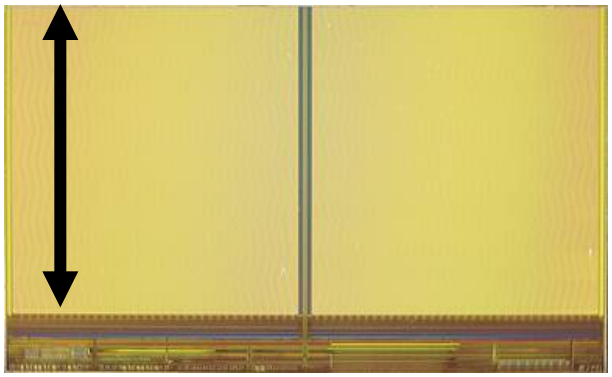
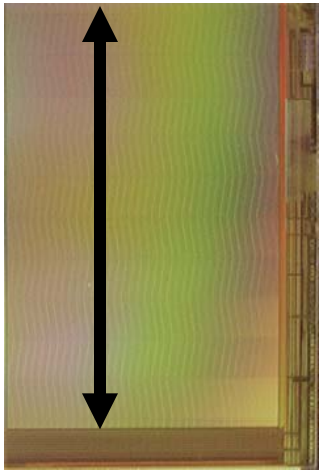
Bit-Line (BL) RC

24nm 64Gb D2



Bit-Line ~ 65,000cells

19nm 64Gb D2

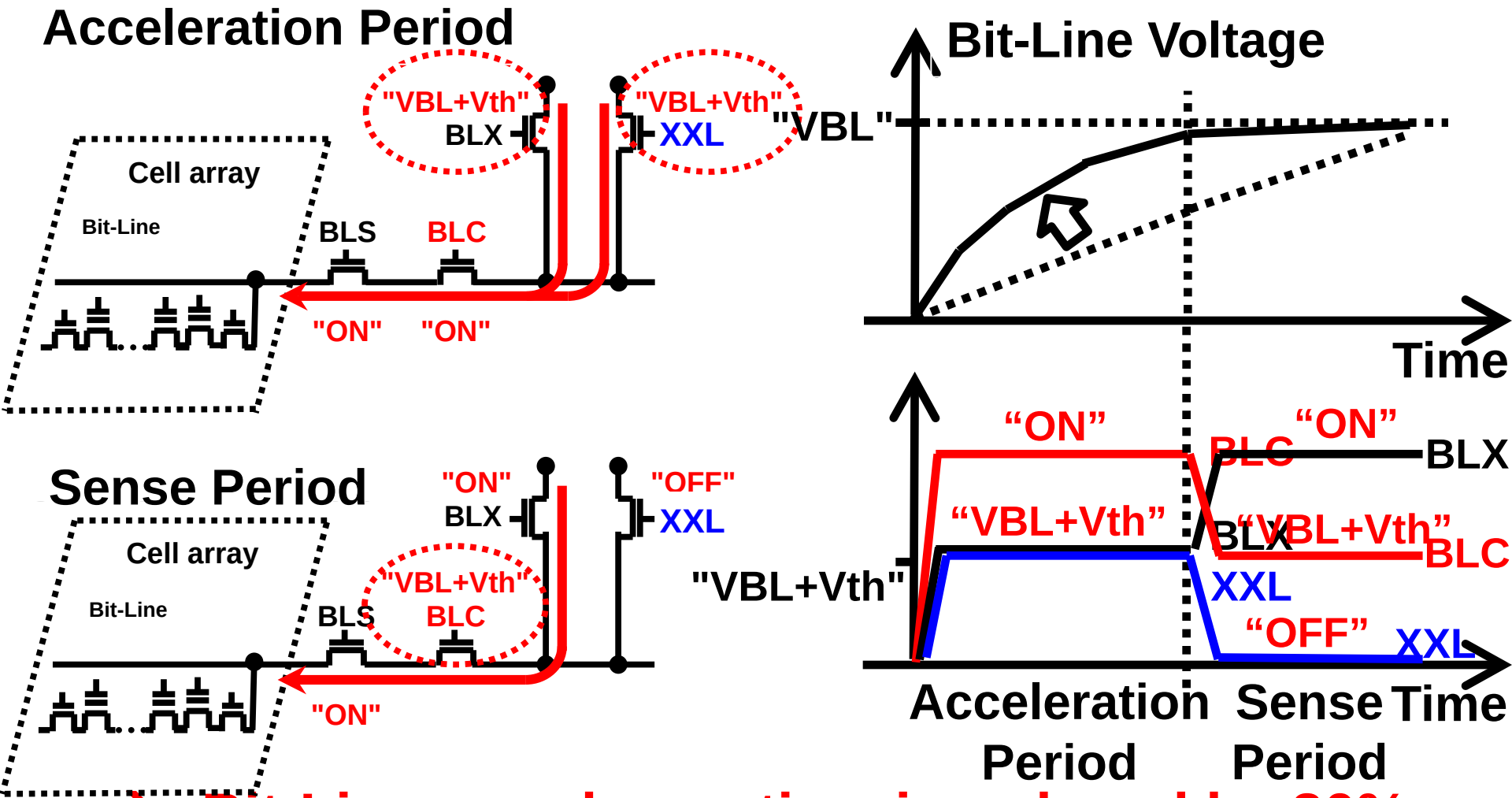


Bit-Line ~ 130,000cells

- Cells connecting to one Bit-Line is doubled

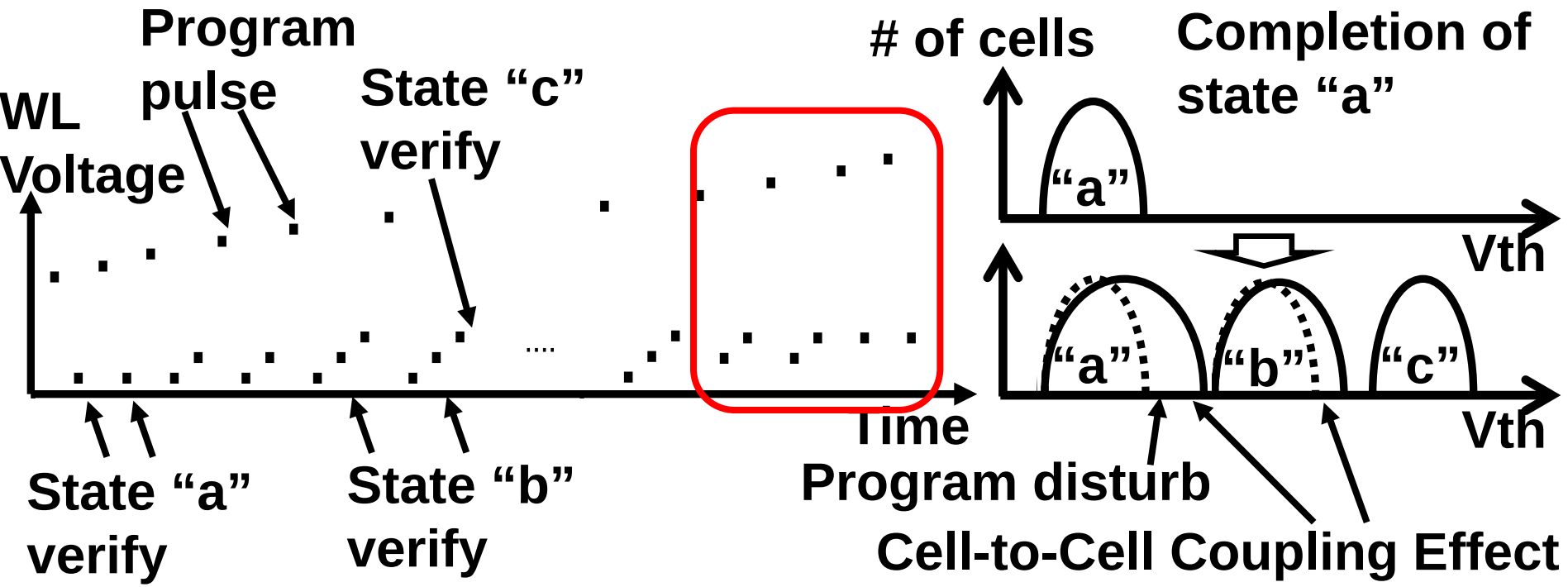
→ Larger Bit-Line (BL) RC

Bit-Line Bias Acceleration (BLBA)



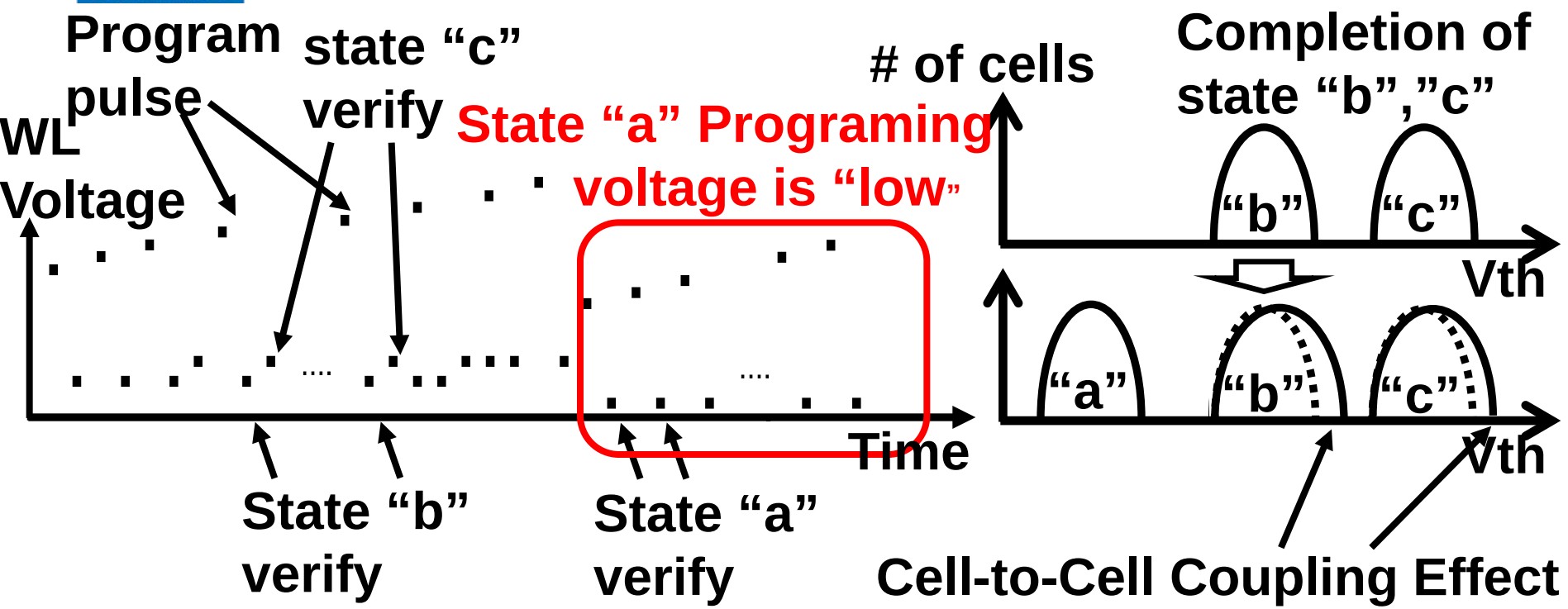
→ **Bit-Line pre-charge time is reduced by 20%**

Conventional-Program Algorithm



State "b" and "c" Programing voltage is "high"

BC-States-First Program Algorithm



→ "Program disturbs" and "cell-to-cell coupling effect" are suppressed

→ Bigger incremental step size can be applied

MLC Program Improvement

- High program throughput with high reliability

	tProg reduction
◆ All-Bit-Line architecture (ABL)	----
◆ Bit-Line Bias Acceleration (BLBA)	(6%)
◆ BC-states-first program algorithm	(8%)
◆ Air Gap technology reduces FG coupling effect and word line(WL) RC	(10%)

Program throughput : 15MB/s(16kB)
tProg : 1.1ms

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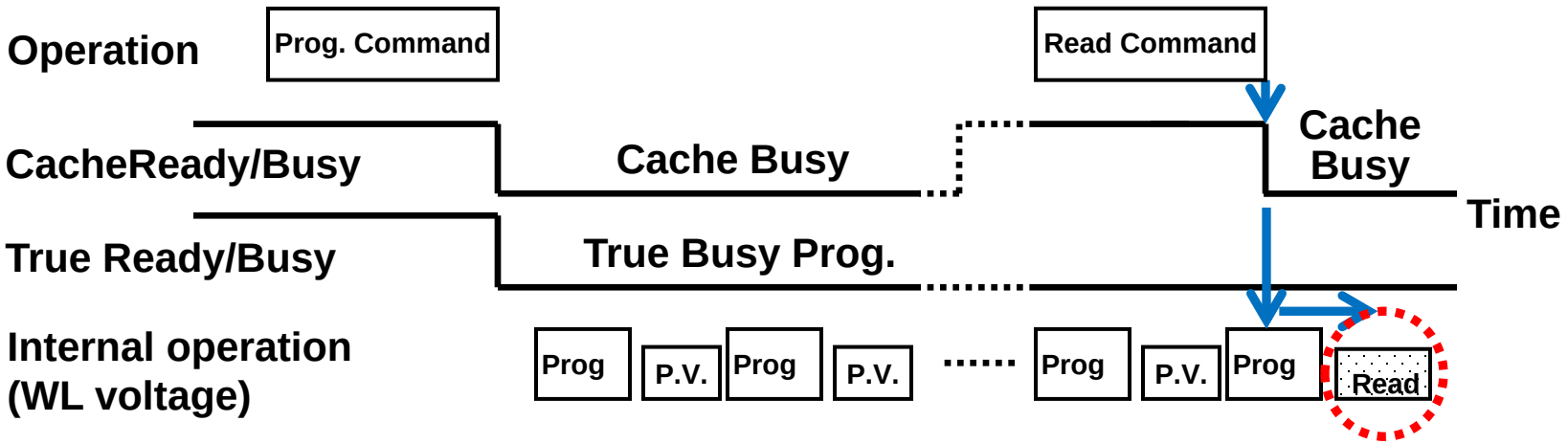
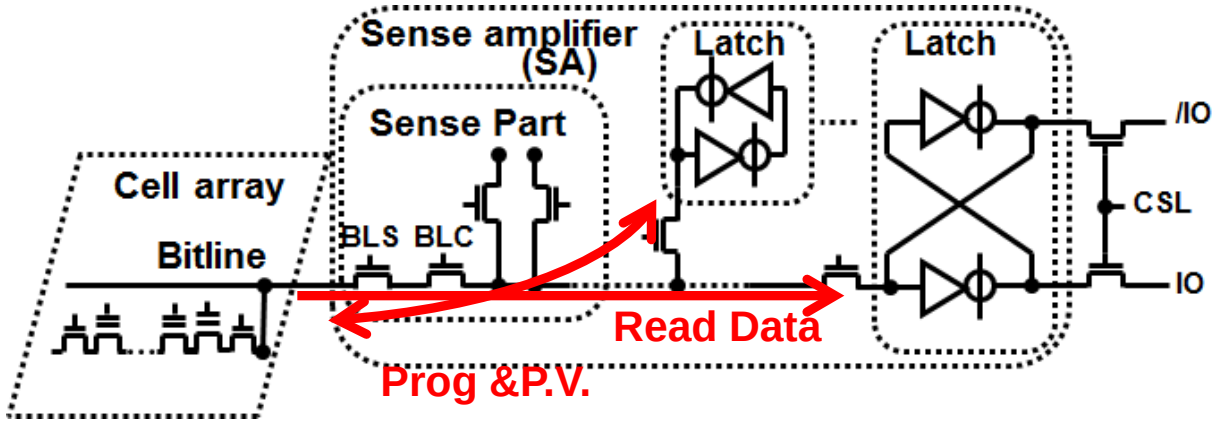
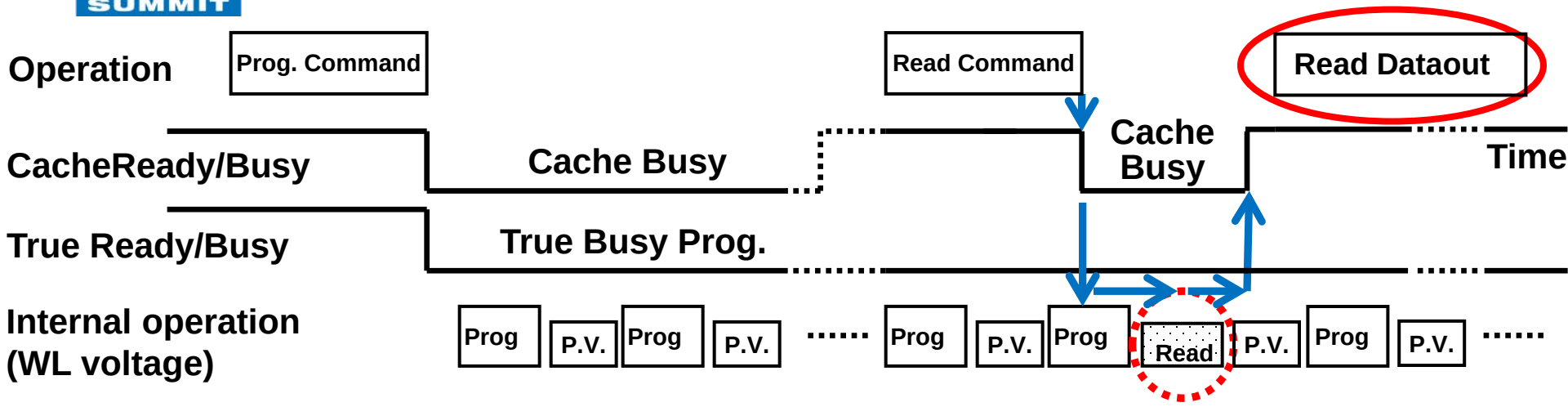
Program-Suspend Function

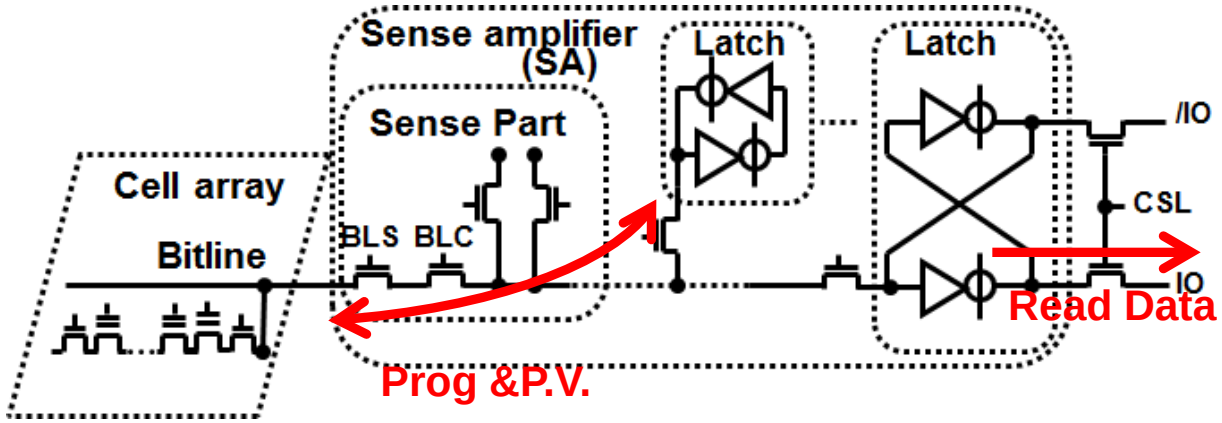




- Any page within any block can be read

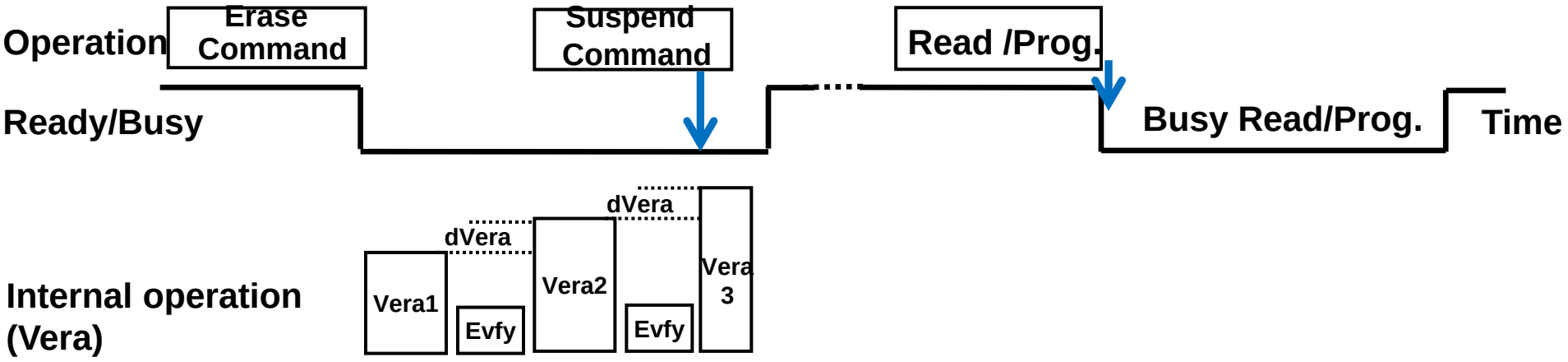
Program-Suspend Function





- Read data shifted out while program resumes

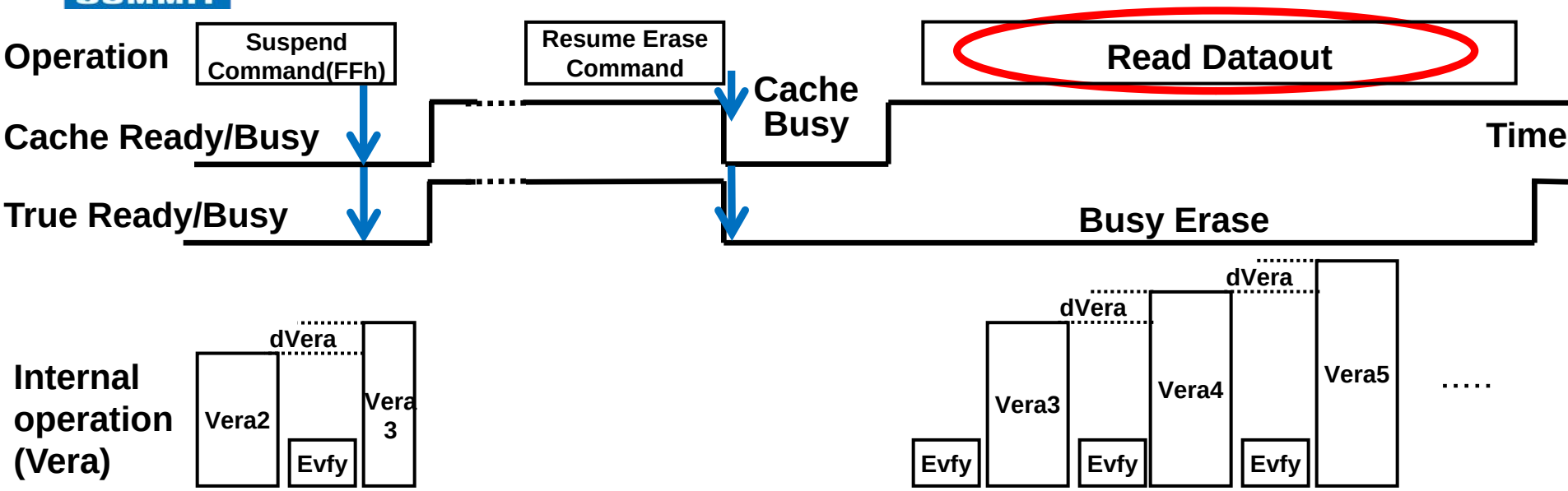
Erase-Suspend Function



- Same sequence as at Reset command.

- Program operation as well as read operation is available without any restrictions on address input

Erase-Suspend Function

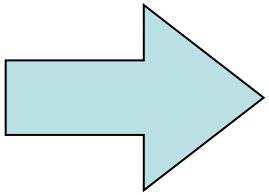


- Read data can be shifted out upon resume of erase sequence.

Read-Latency Reduction

- Read latency at program/erase is improved to 50us, which is comparable to normal read latency(~40us)

1ms at program
4ms at erase



50us

Conventional

This work

- Program-suspend function
- Erase-suspend function

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Summary of Key Features

- Density: 64Gb, 2-bit/cell
- One sided ABL architecture
- Organization
  - 16kB / Page
  - 2 Pages / WL
  - Single-array configuration
- Program Throughput: 15MB/s
- Burst Cycle Time:
  400Mb/s/pin Toggle mode @1.8V
- Power Supply: 2.7V to 3.6V
- Technology: 3-Metal 19nm CMOS
- DieSize: 112.8mm^2

Conclusion

- For the first time, a 112.8mm^2 64Gb Multi-level (2bits/cell) NAND flash memory is developed
  - 19nm CMOS technology
  - Single Array configuration
  - One sided All-Bit-Line
- 400Mb/s/pin 1.8V high speed Toggle Mode interface
- 15MB/s programing throughput with high reliability
  - Bit-Line Bias Acceleration(BLBA)
  - “BC” states-First program algorithm
- Read latency is improved by Program-Suspend and Erase-Suspend functions

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[2]SanDisk Corp., Milpitas, California, USA

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