

Taking Consumer MLC to Extreme Endurance

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- Talking about a formula while keeping it secret
- Why do we need a recipe?
- The recipe ingredients
- Gathering block statistics
- Recipe implementation
- Example results
- Conclusion

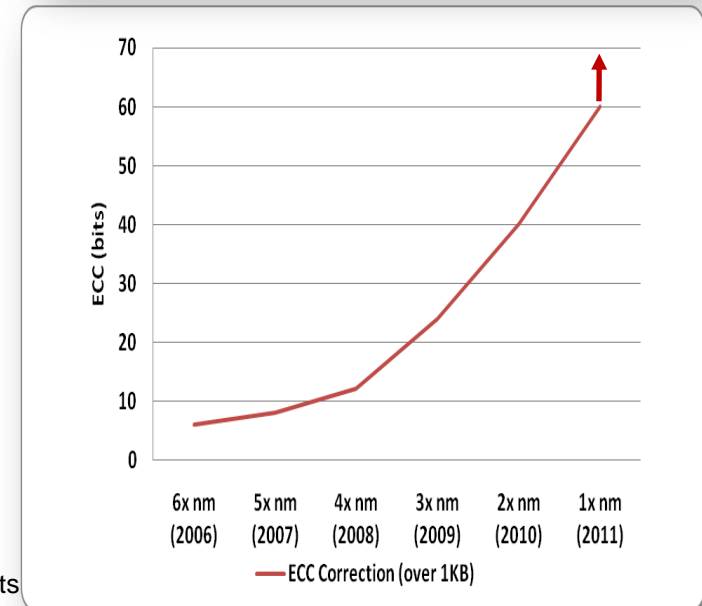
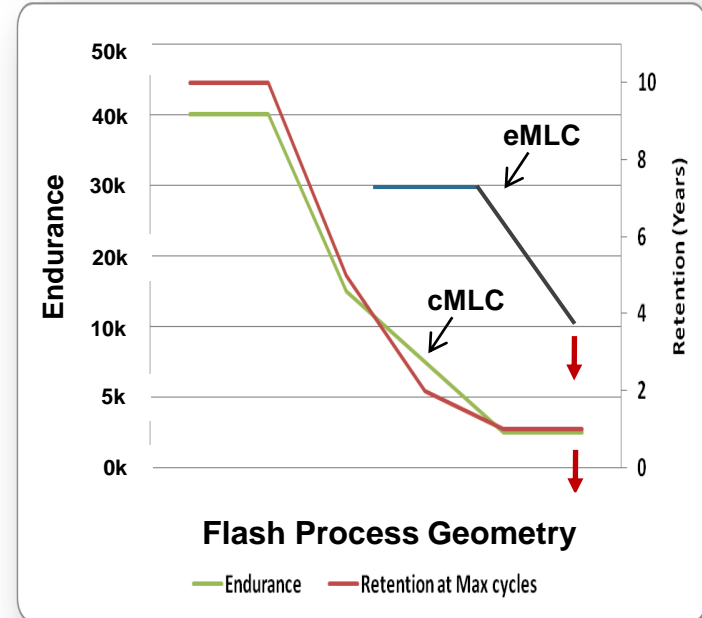
Ahh! That Secret Formula...



You CAN talk about the ingredients while still NOT disclosing the secret formula!

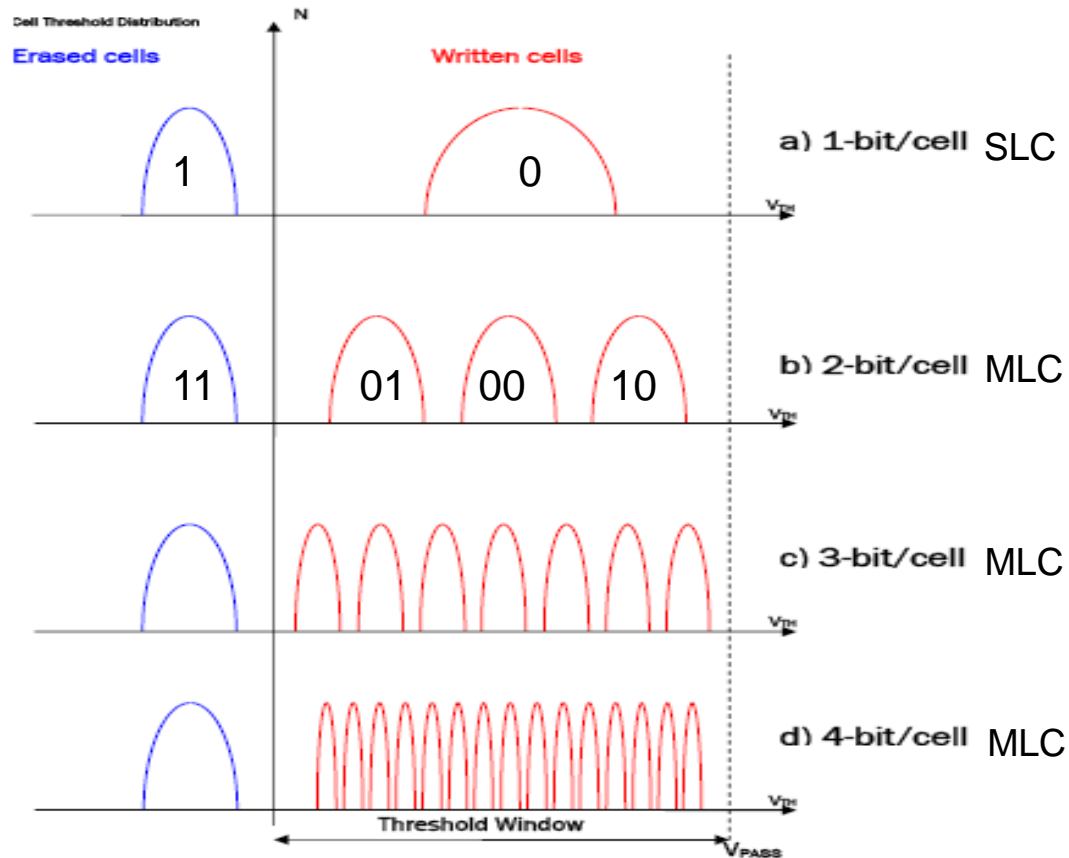
Why do we need a Recipe?

- Flash Endurance (number of cycles) is reduced as flash density increases
- Flash Retention (ability to hold information) is reduced as the flash wears
- We need a way to bridge the gap between what the flash provides and what the SDD requires

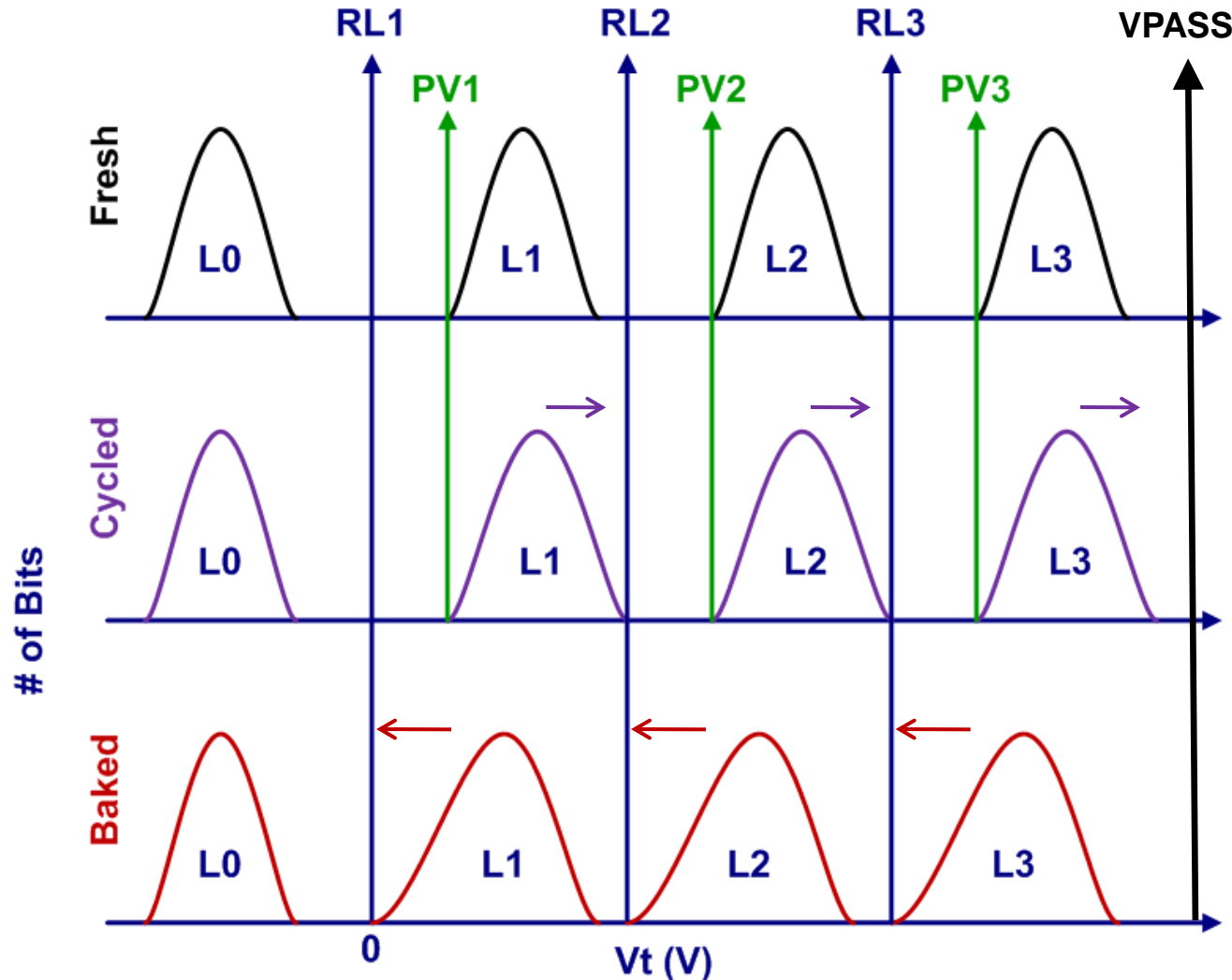


From SLC to n-bit MLC

- Before we show how to bridge this gap, here is a brief tutorial



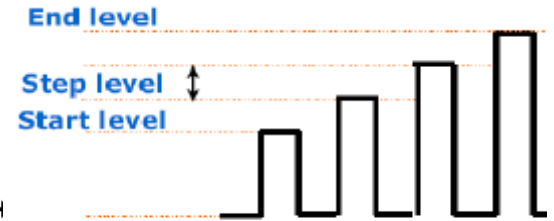
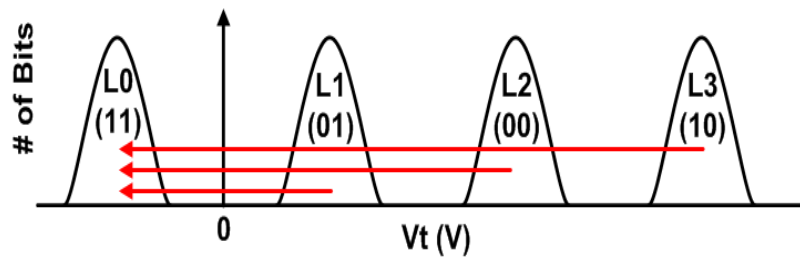
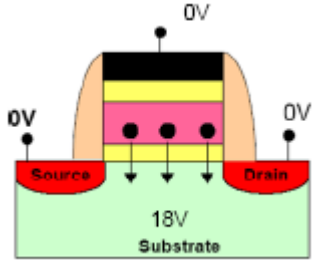
The Recipe Ingredients



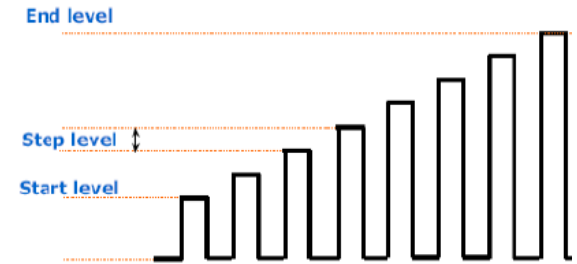
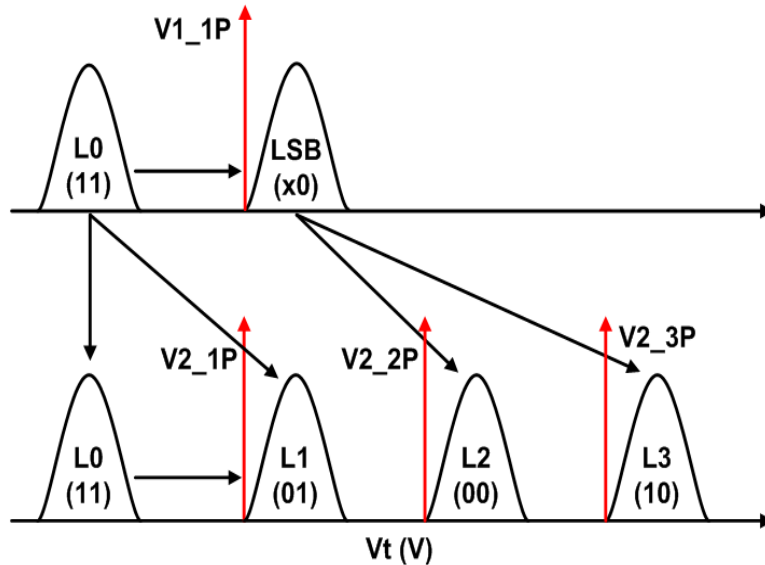
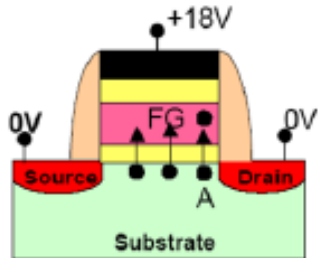
- **Fresh**
 - Narrowest distributions
 - Widest gaps
 - Output is 00, 01, 10, 11
- **Cycled**
 - Wider distributions
 - Width increases with cycle number
 - Narrower gaps
- **Baked**
 - Widest distributions
 - Distributions shift to left ($\Delta L3 > \Delta L2 > \Delta L1$)
 - Shift increases with number of cycles, higher PR/ER stress, bake time & temp

The Recipe Ingredients

ERASE

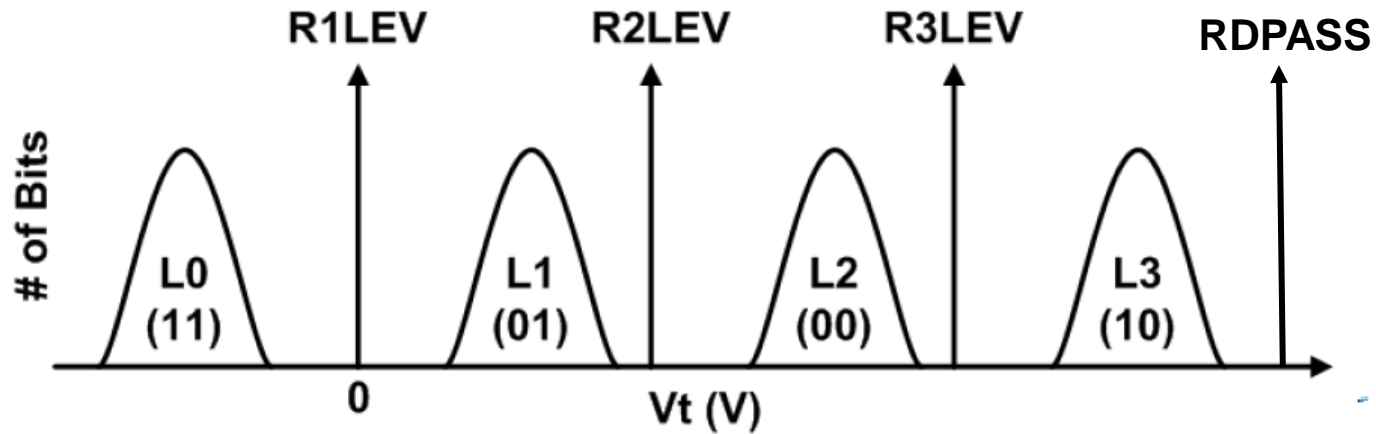
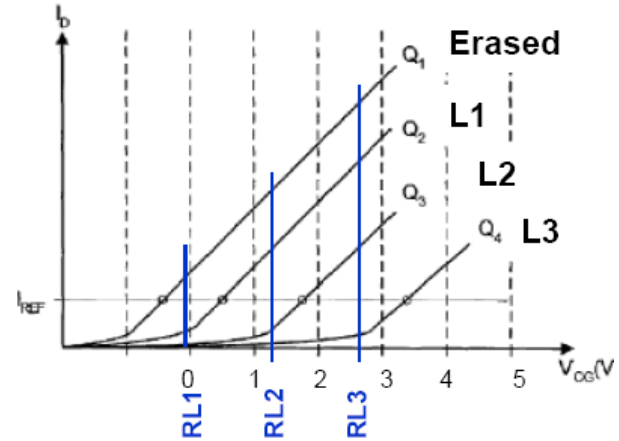
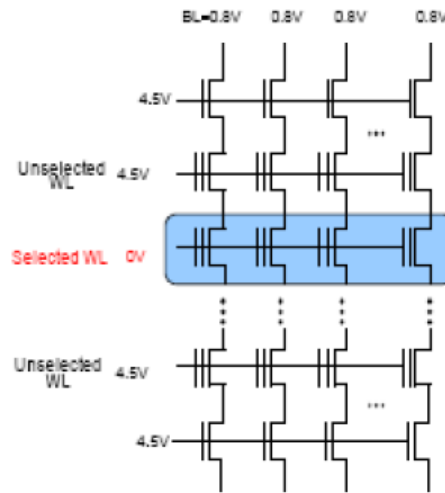


PROGRAM



The Recipe Ingredients

READ

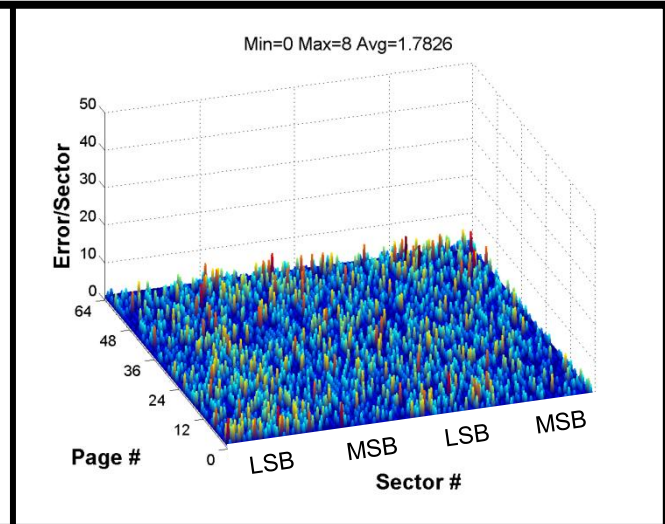
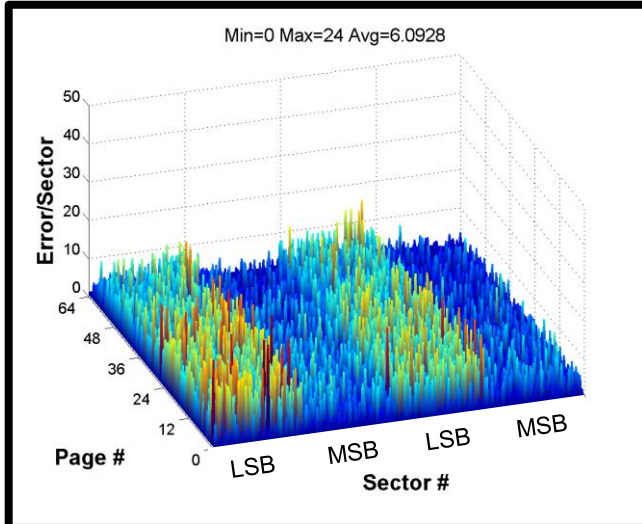


Gathering Block Statistics

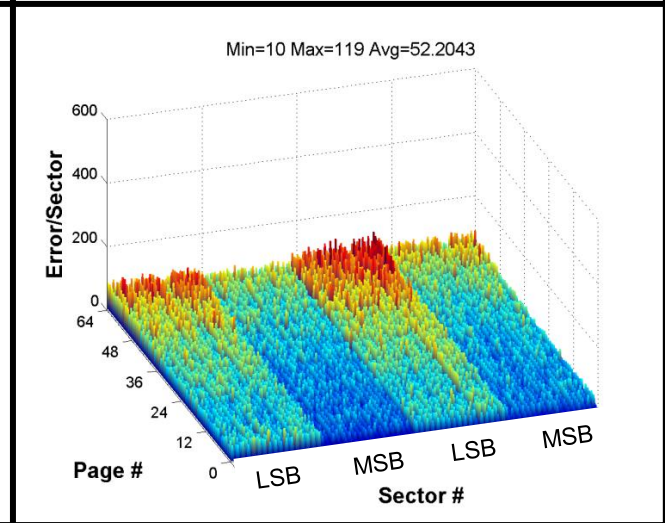
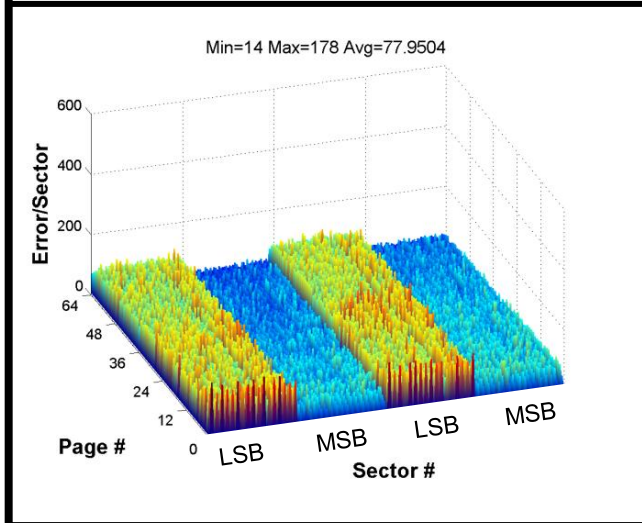
Default RLs

Optimized RLs

5k
Cycles



50k
Cycles

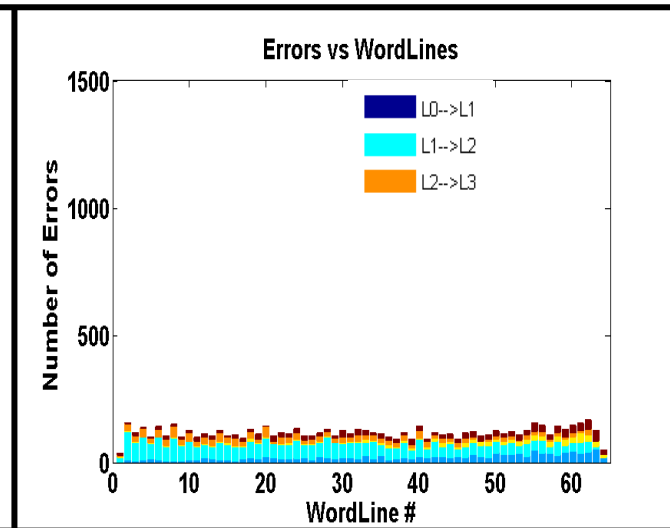
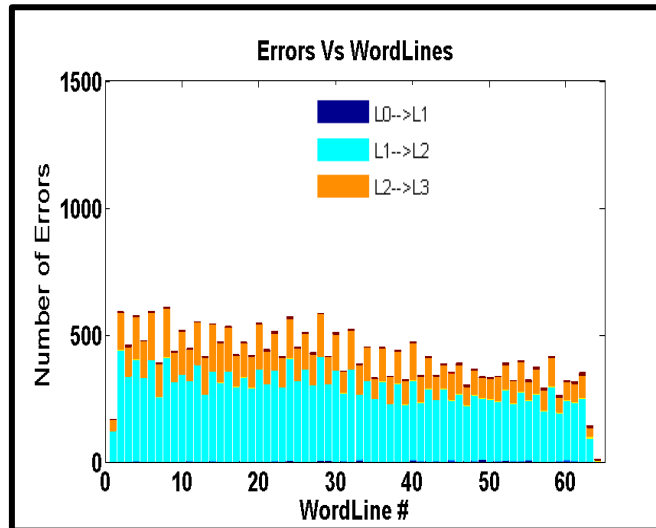


Gathering Block Statistics

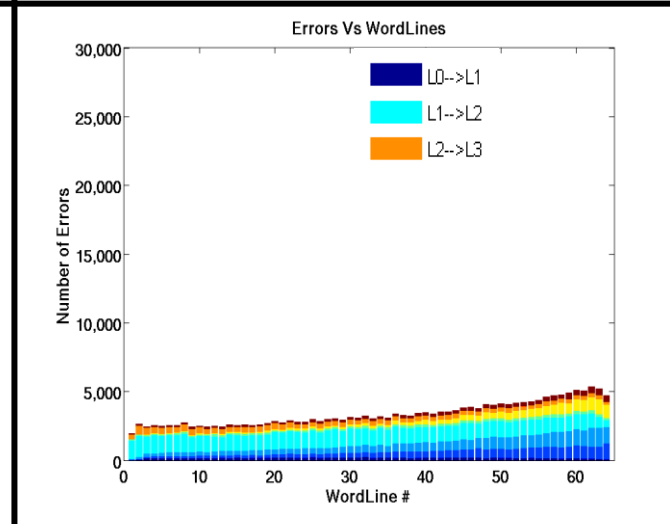
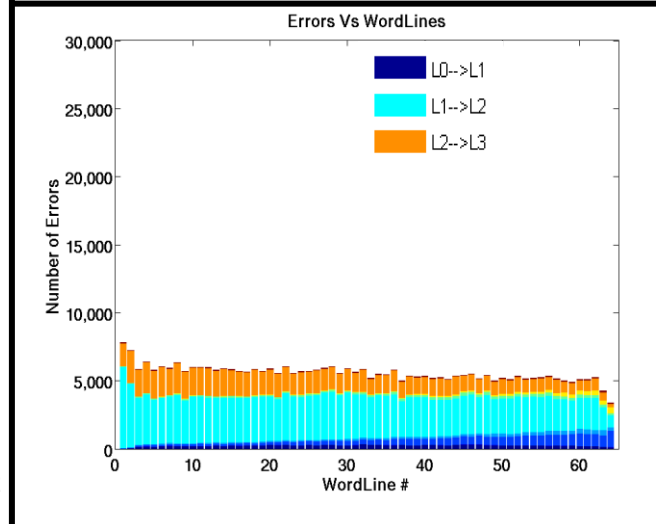
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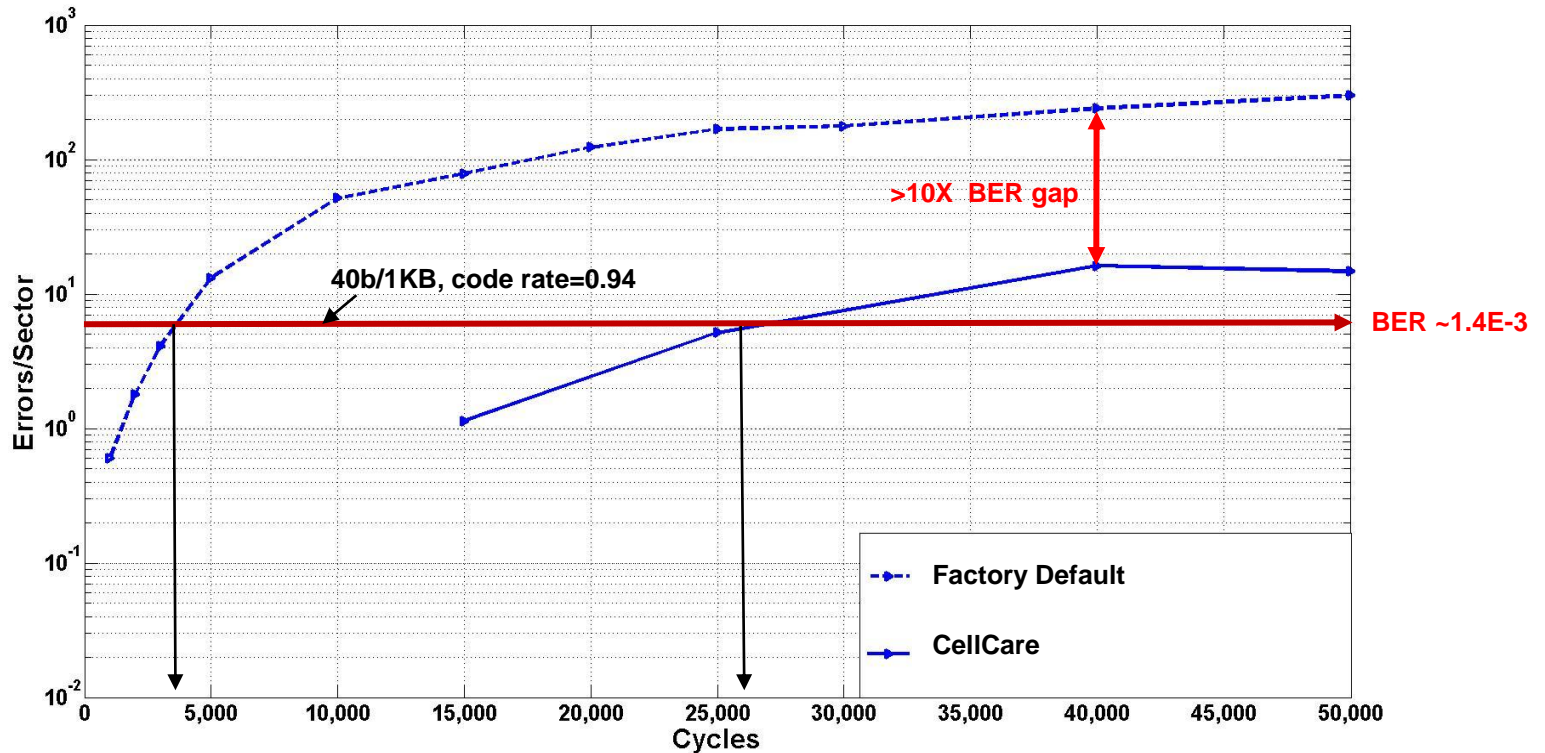


Recipe Implementation

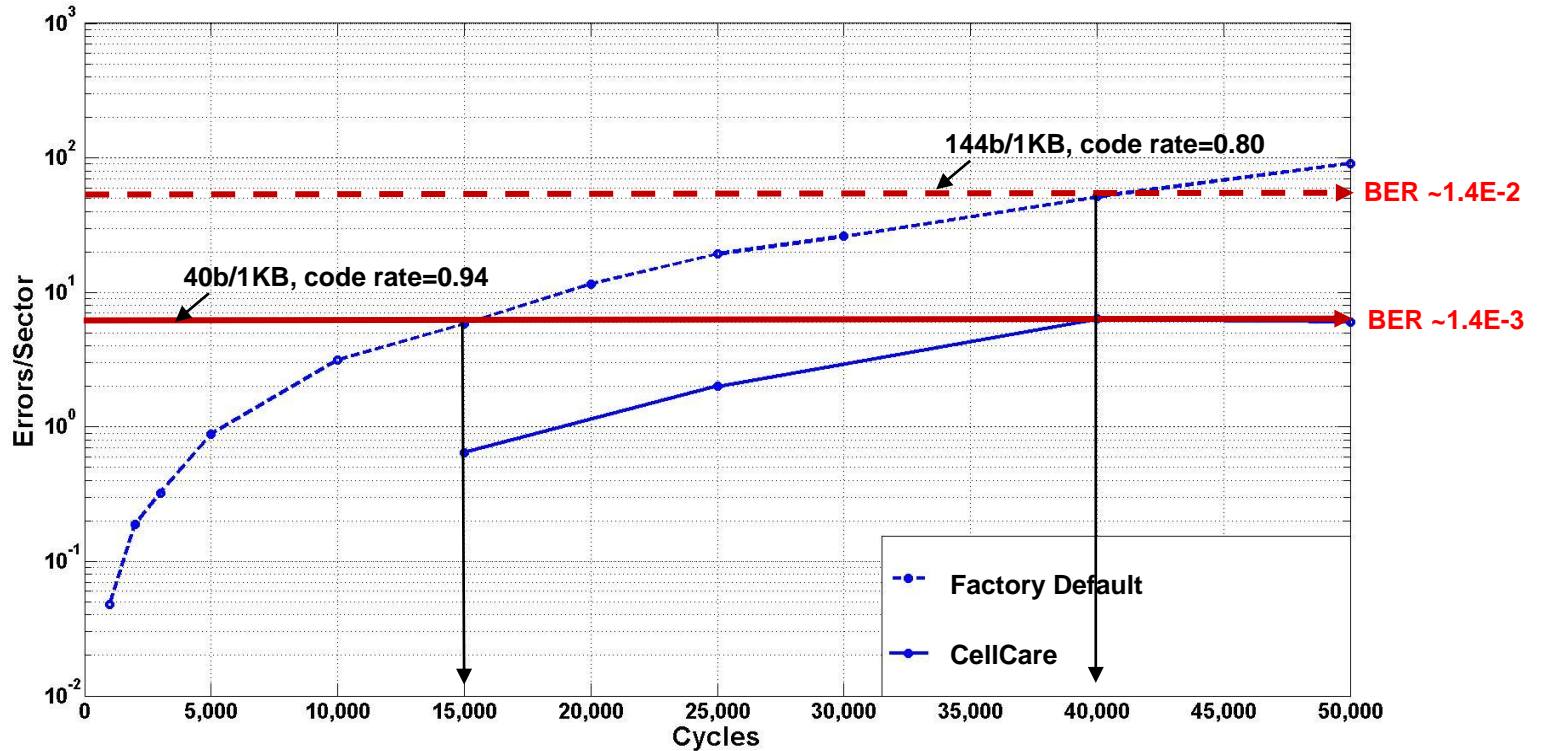
- HW & FW working together in the ASIC controller to improve MLC flash reliability throughout the life of the drive
 - Flash trimming for SSD application
 - Flash management through flash lifetime
 - Advanced error correction with DSP



2xnm cMLC: Default Read Levels (3mo@40C retention)



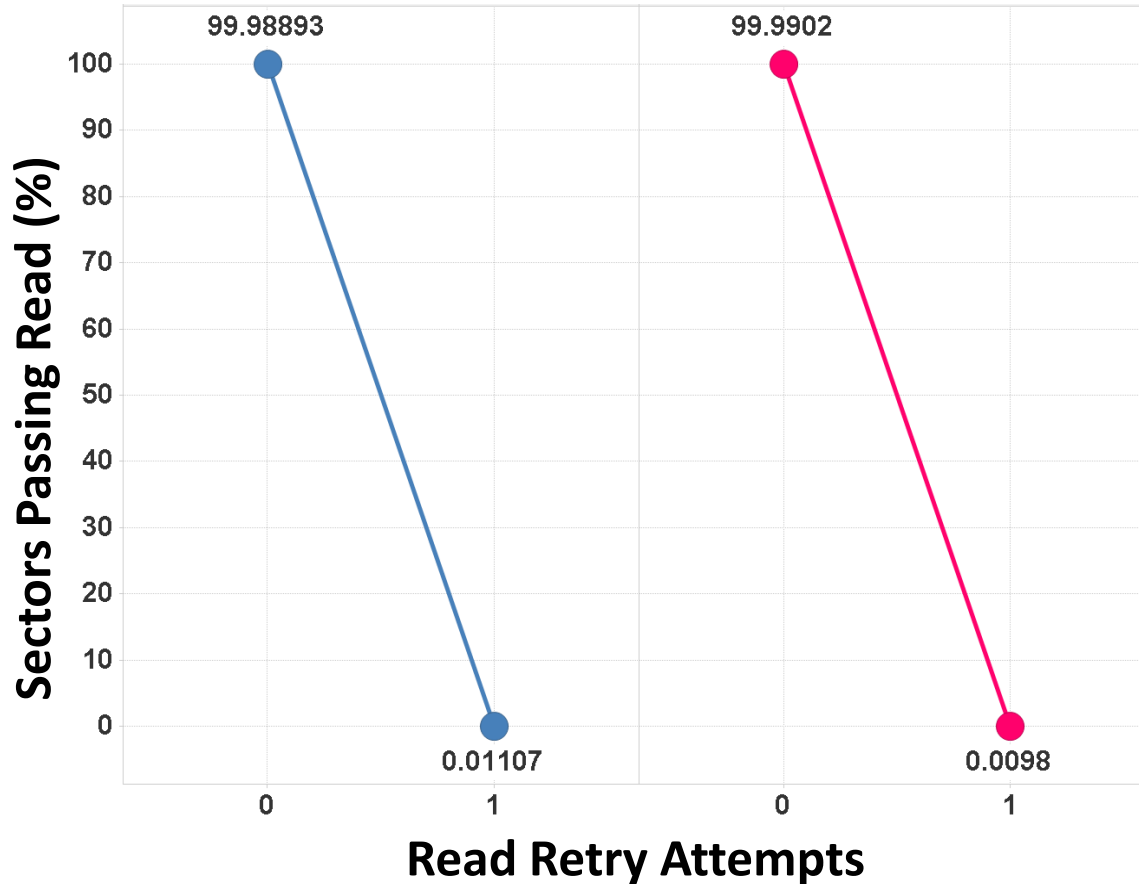
24nm cMLC: Optimized Read Levels (3mo@40C retention)



Minimization of Read Retry


After Endurance Cycling

After Retention Bake



- Total of 2,357,248 sectors read
- 0.0111% of sectors required Read Retry after Endurance
- 0.0098% of sectors required Read Retry after Retention
- Maximum of 1 Read Retry attempt required after Endurance and Retention

2xnm cMLC Qualification Results

Key Performance Metrics	2xnm cMLC Datasheet Spec	2xnm cMLC CellCare Results 
Endurance Cycles	3,000	40,000
Retention (EOL)	1Y@40C	3mo@40C
Read Retry Rate (EOL)	Unspecified	<<1%

Conclusion

- Adding ECC by itself does is not enough to reach extreme endurance
 - More ECC overhead works against you as it increases write amplification, therefore increasing the actual endurance target
- Taking consumer MLC to extreme endurance requires
 - Specialized flash trimming at least on a per-die basis
 - Management of flash as it ages, making adjustments as necessary
 - DSP and ECC techniques



THANK YOU!

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