Increasing NAND Flash Endurance Using Refresh Techniques

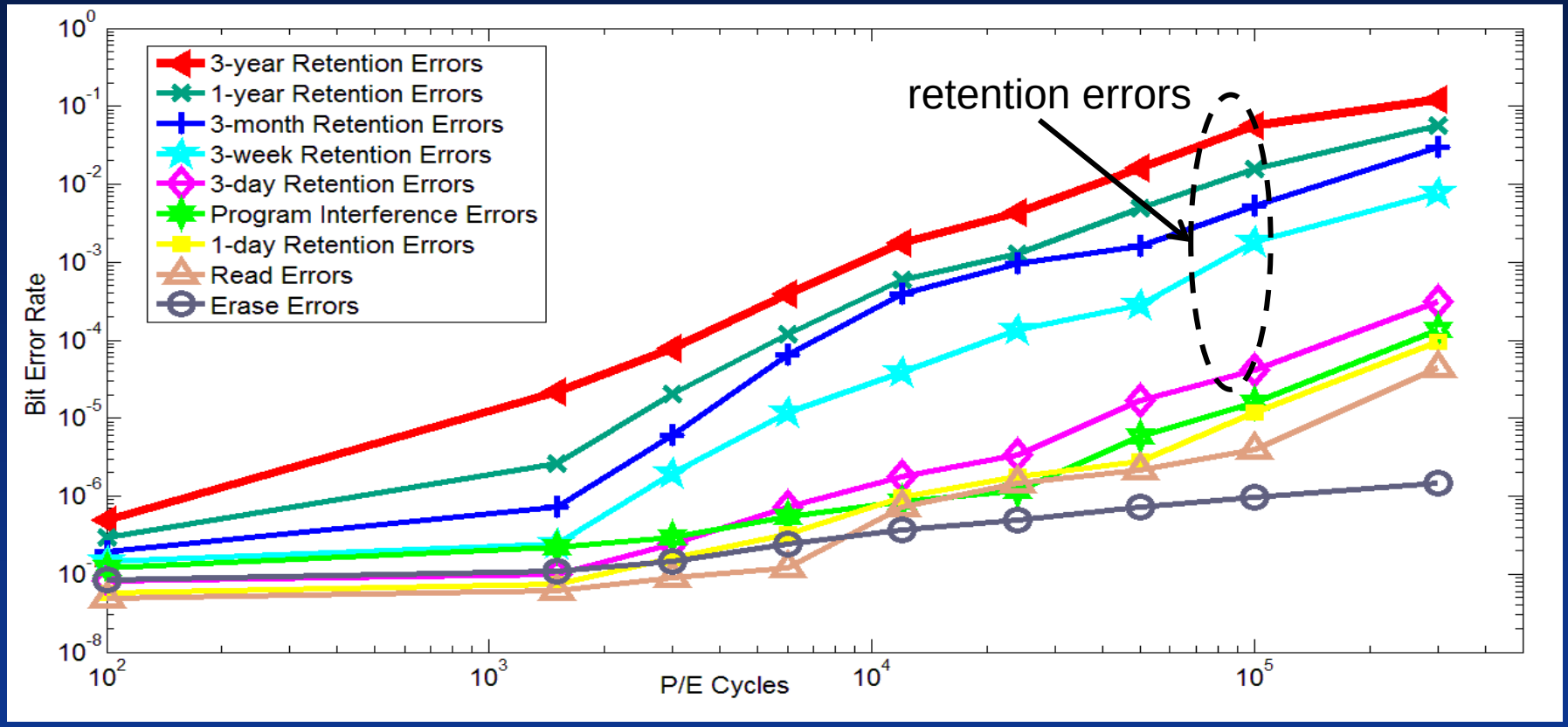
Yu Cai[1], Gulay Yalcin[2], Onur Mutlu[1], Erich F. Haratsch[3], Adrian Cristal[2], Osman S. Unsal[2] and Ken Mai[1]

DSSC, Carnegie Mellon University[1]

Barcelona Supercomputing Center[2]

LSI Corporation[3]

Errors in NAND Flash Memory



- Error rate increases with P/E cycles
- Retention errors are the most dominant errors
- Retention error rates increase as retention time increase

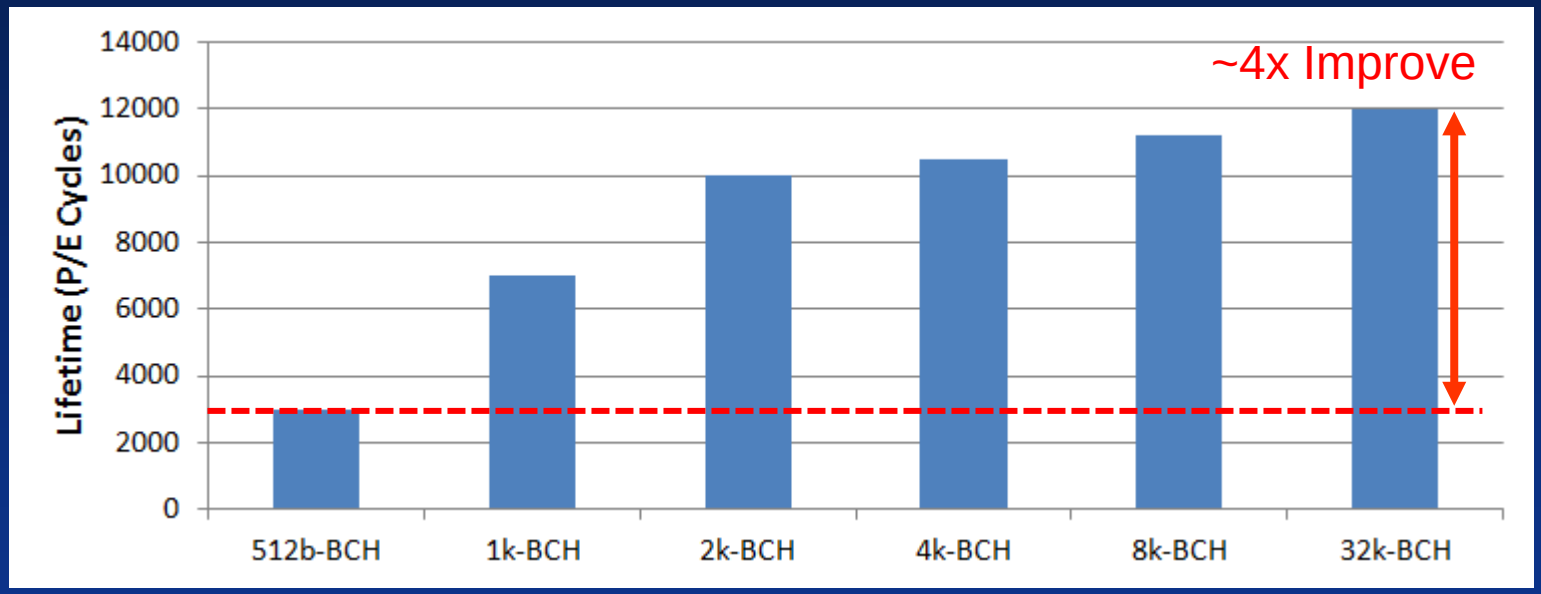
BER and ECC Analysis for NAND Flash Memory

- ECC (n, k, t) selection guidelines
  - Efficiency: >0.89 coding rate (k/n)
  - Reliability: $<10^{-15}$ uncorrectable error rate after ECC
  - Code length: segment of one flash page (e.g. 4k-bytes)
- Characteristics of various error correction codes (BCH)

Code length (n)	Correctable Errors (t)	Acceptable Raw BER	Norm. Power	Norm. Area
512	7	$1.3x10^{-4}$ (1x)	1	1
1024	12	$5.5x10^{-4}$ (4x)	2	2.1
2048	22	$1.0x10^{-3}$ (7.7x)	4.1	3.9
4096	40	$1.1x10^{-3}$ (8.5x)	8.6	10.3
8192	74	$1.2x10^{-3}$ (9.2x)	17.8	21.3
32768	259	$2.0x10^{-3}$ (15.4x)	71	85

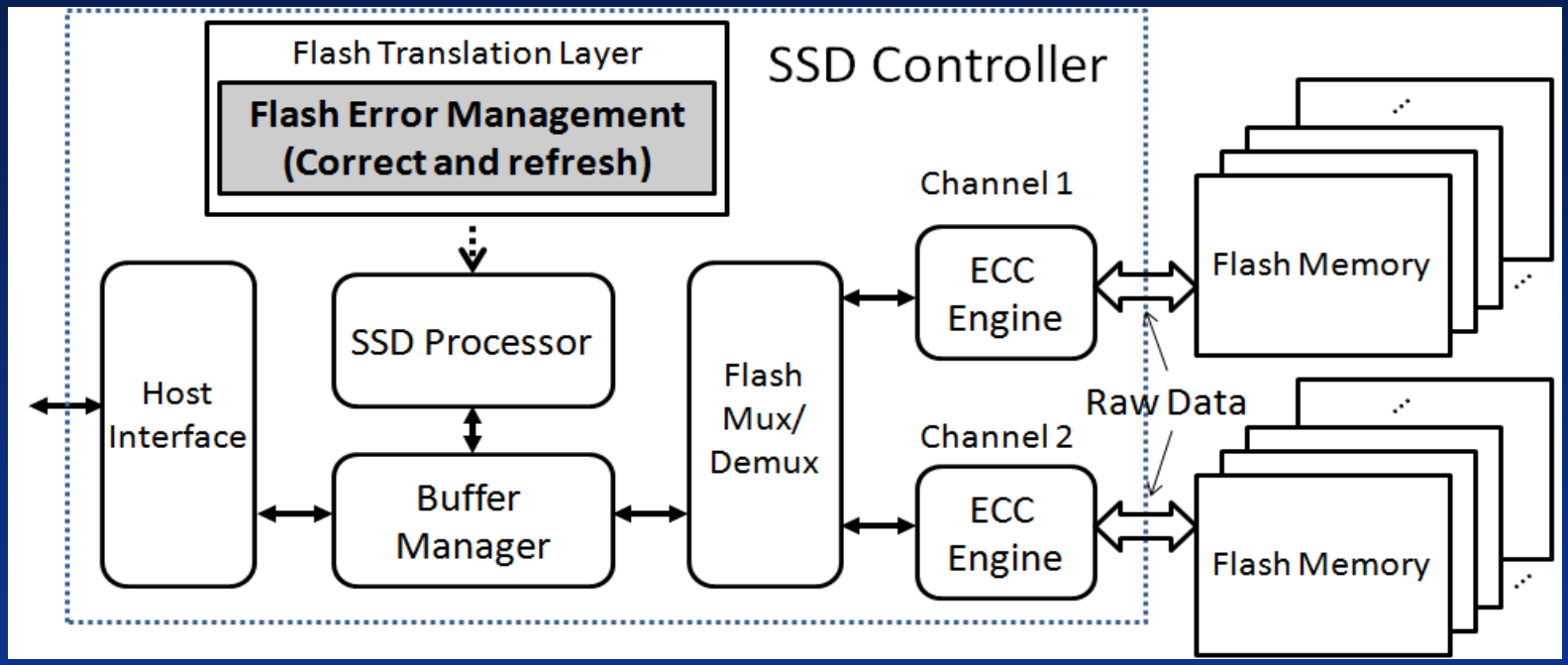
BER & ECC Analysis for NAND Flash Memory (cont)

- Lifetime improvement comparison of various BCH codes



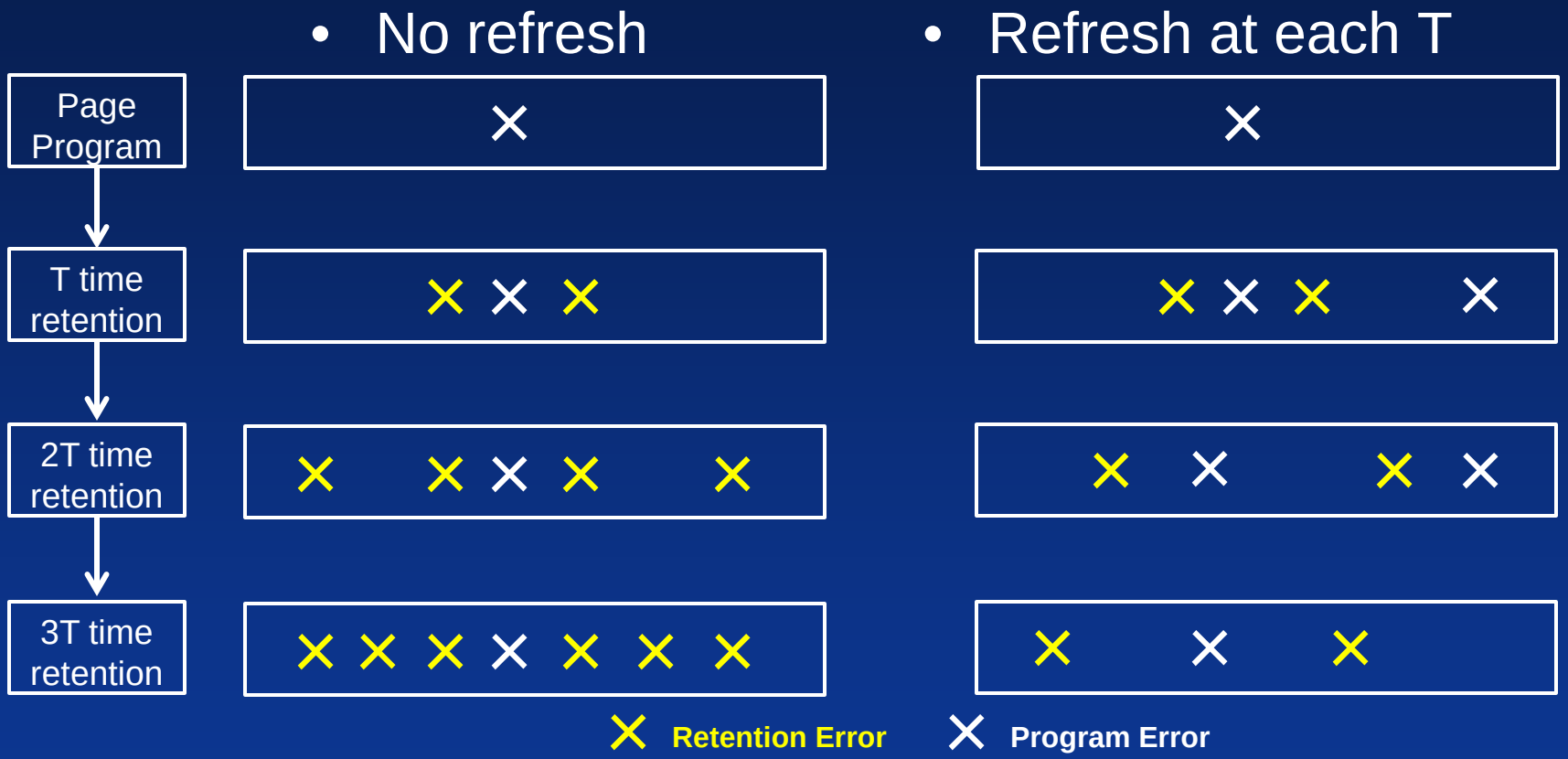
- Summary
  - Raw BER of NAND flash increases exponentially as P/E cycles
  - Stronger ECC improves flash lifetime with diminishing returns
  - Raw BER MUST be decreased to achieve lifetime improvement

Using Refresh Techniques to Improve the Flash Lifetime



- Flash Correct-and-Refresh (FCR)
  - Read, correct, and refresh the stored data before flash accumulates more retention errors than can be corrected by simple ECC

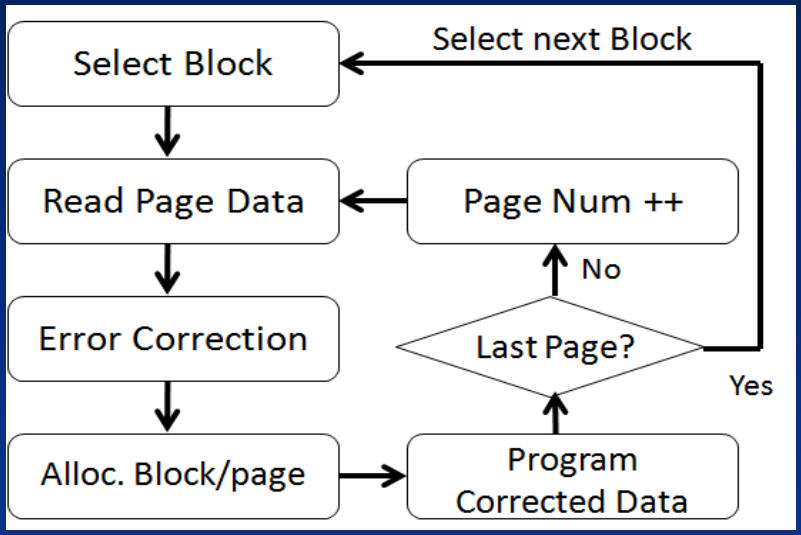
Raw flash errors under refresh and no-refresh



- Refresh can control the number of bit errors
- Two key questions
  - (1) How to refresh? Remapping, In-place or Hybrid
  - (2) When to refresh? Periodically or Adaptively

Remapping Based FCR

- Work flow



- Error Model

refresh period Number of refresh periods

$$E_{total}^{no-refresh} = E_{retention}(T \times N) + E_{program} + E_{read} + E_{erase}$$

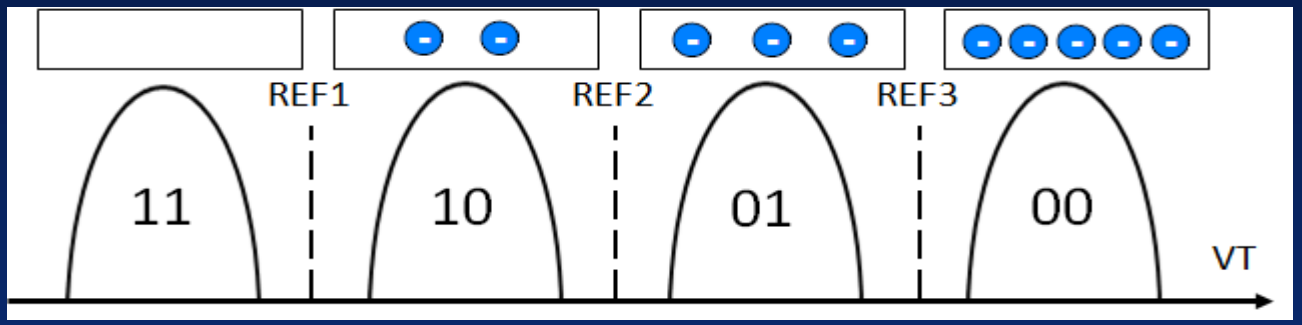
$$E_{total}^{remap} = E_{retention}(T) + E_{program} + E_{read} + E_{erase}$$

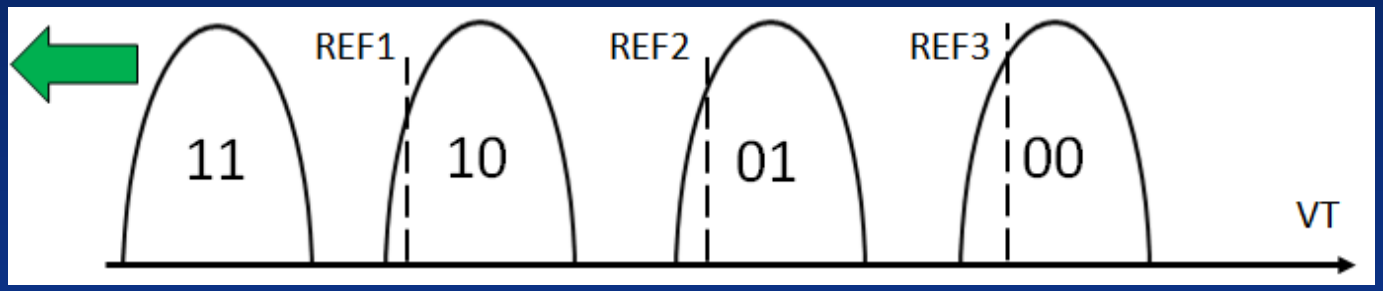
Error Rate Ratio

$$\frac{E_{total}^{no-refresh}}{E_{total}^{remap}} \approx \frac{1}{N}$$

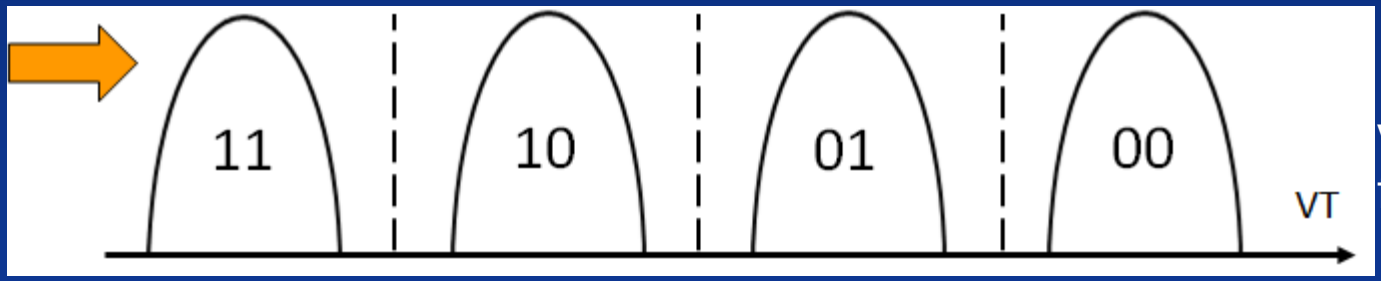
- Summary
  - Overall error rate can be decreased by increasing the refresh rate
  - Periodic remapping of block introduces additional erase operations
    - More frequent the remap, more erase and more wear out

In-place refresh without erase





Retention errors are caused by threshold voltage shifting to left

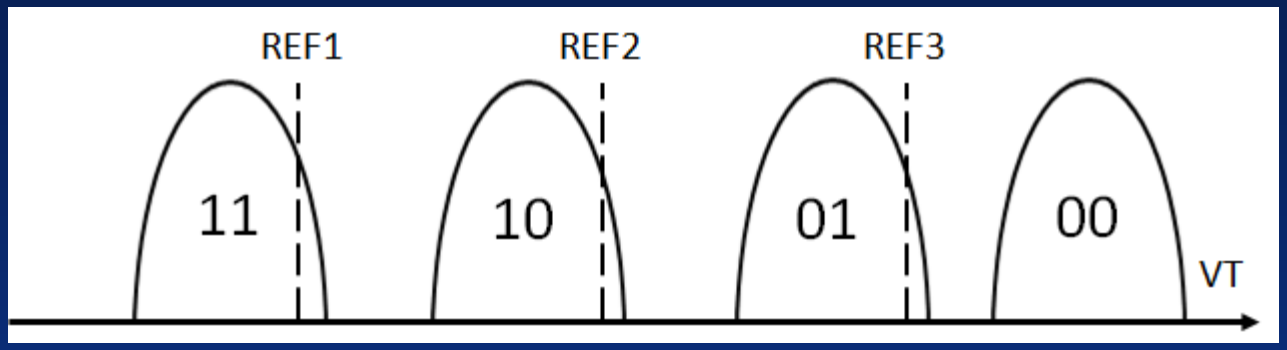


ISPP shift threshold voltage to the right and fix retention errors

- Basic in-place reprogramming based FCR mechanism can be implemented without remapping data to other new blocks

Problems of in-place refreshing

- Program interference causes threshold voltage shift to right

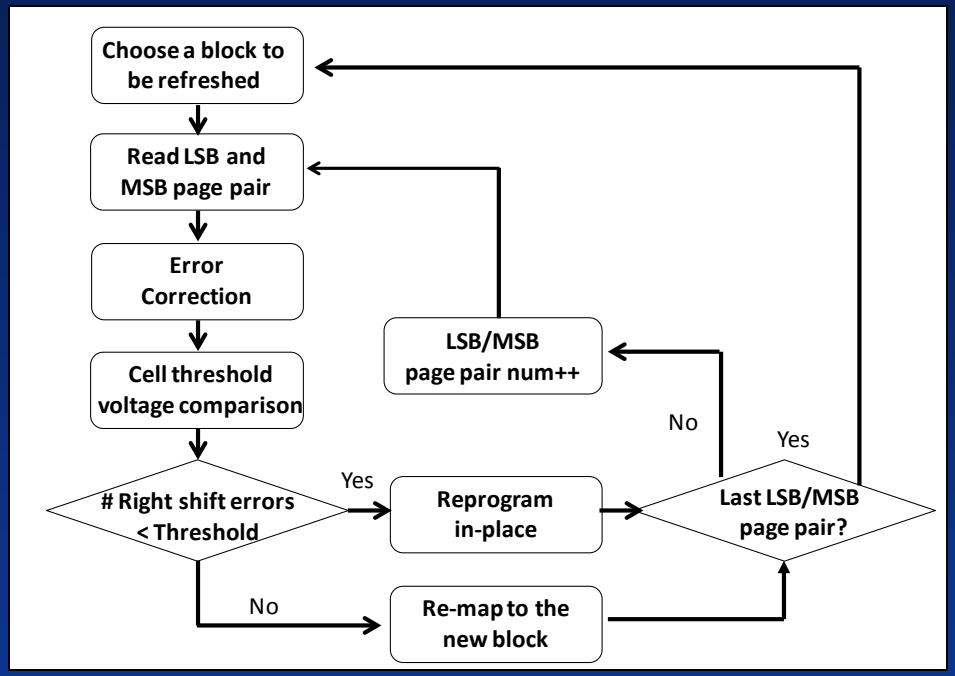


- Example of in-place reprogramming

Original data to be programmed	...	00	11	01	00	10	11	00	...
Program errors after initial programming	...	00	**10**	01	00	10	11	00	...
Retention errors after some time	...	**01**	**10**	**10**	00	**11**	11	**01**	...
Errors after in-place reprogramming	...	00	**10**	01	00	10	**10**	00	...

Hybrid FCR

- Hybrid FCR work flow



- Error model

Basic in-place refresh

$$E_{total}^{in-place} = E_{retention}(T) + E_{program} + E_{read} + E_{erase} + N \times E_{reprogram}$$

N uncontrolled

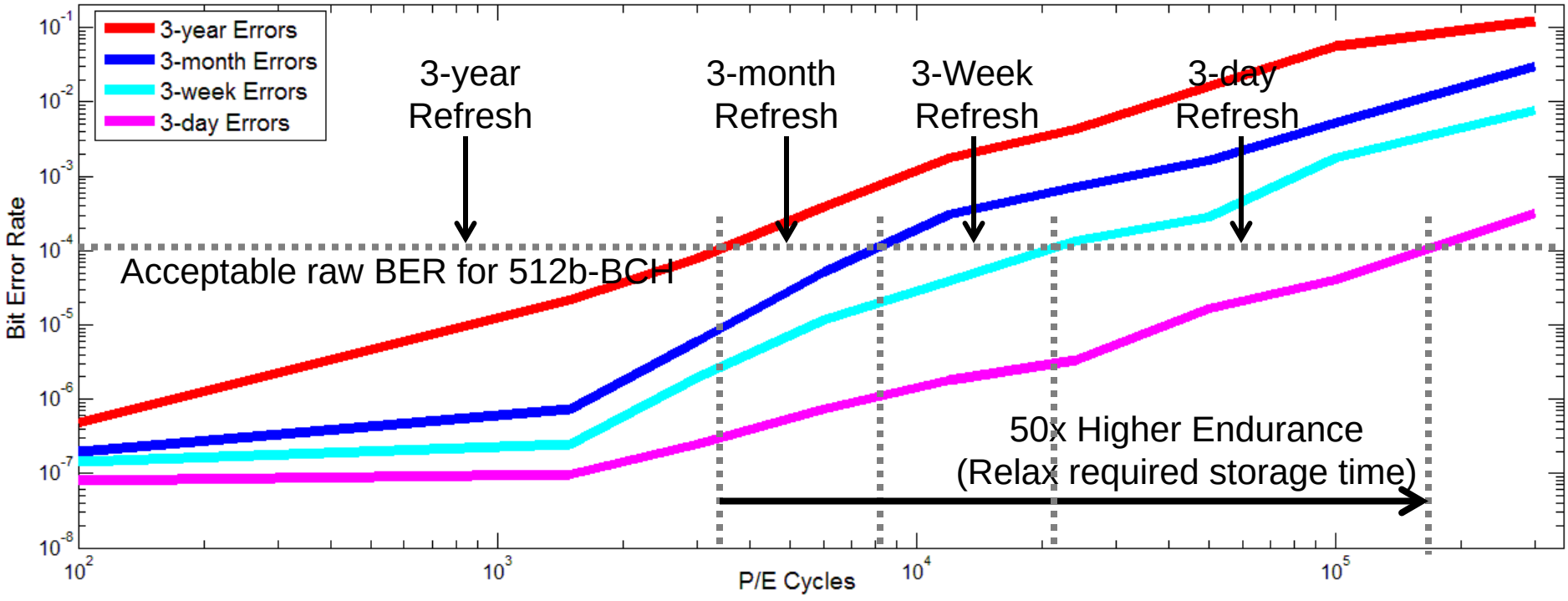
Hybrid FCR

$$E_{total}^{hybrid} = E_{retention}(T) + E_{program} + E_{read} + E_{erase} + N \times E_{reprogram}$$

N < Controlled threshold

- Hybrid FCR
  - If right shift program error count is less than a threshold, in-place reprogram the block; otherwise, remap to a new block
  - Greatly reduce additional erase operations due to remapping

Adaptive-Rate FCR



- Trigger refresh operations only when necessary by tracking the number of P/E cycles of each block

Considerations for FCR techniques

- Implementation cost
  - Do not require hardware changes, only changes FTL software
  - Per-block P/E cycle information maintained in existing flash systems
- Power supply continuity
  - Proposed for enterprise storage, which are continuously powered on
- Response time impact
  - Trigger refresh operations whenever idle
  - Refresh operations can be interrupted by normal operations
  - Refresh period is at least a day, and can be finished within the period
- Additional erase operations
  - Hybrid FCR and adaptive rate FCR can greatly reduce additional erase operations

Evaluation Methodology

- Simulation framework
  - Disksim with SSD extensions
- Workload with various write ratios
  - File system applications: iozone (>99%), postmark(17%), cello99 (62%), MSR-Cambridge (20%)
  - Database application: oltp (48%)
  - Web search application: websearch (<1%)
- Lifetime evaluation

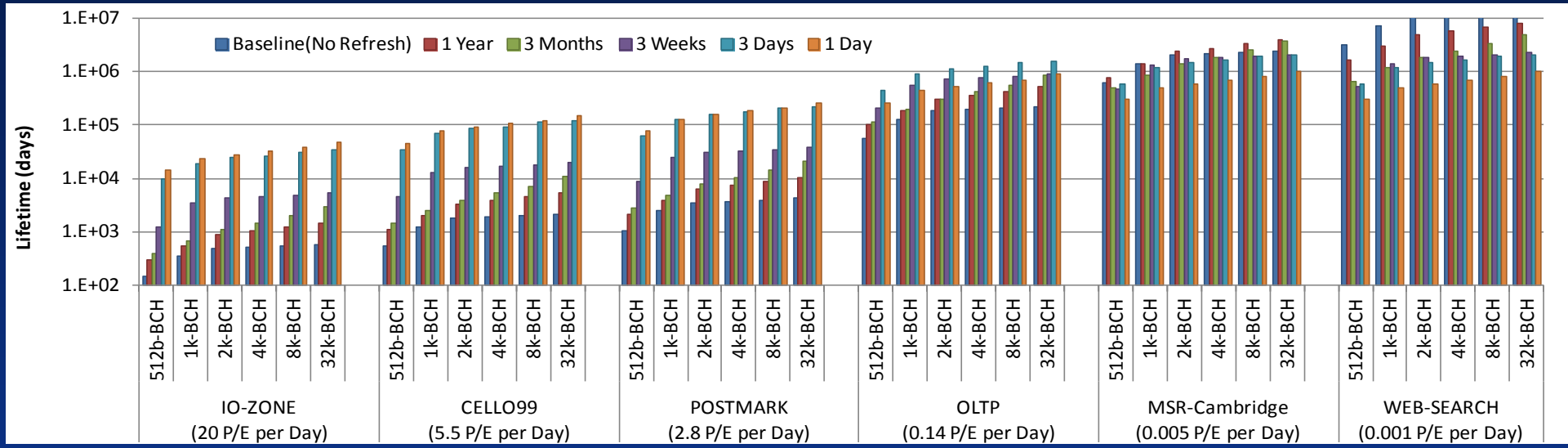
$$\frac{\text{Maximum Full Disk P/E Cycles}}{\text{Total full disk P/E Cycle Given Application}} \times \text{\# of Days of Given Application}$$

Experimental Testing Data

Simulated Data

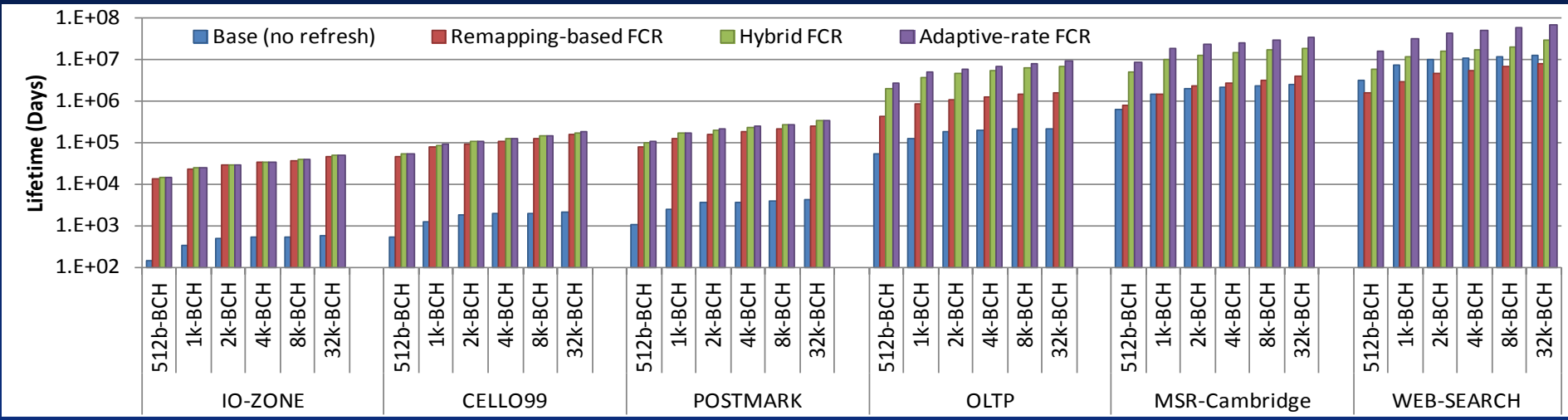
Announced time of each benchmark

Flash Lifetime with Remapping-Based FCR



- Given the same workload and the same refresh interval (or no-refresh), stronger ECC always provides a longer lifetime than weaker ECC
- Remapping based FCR provides significant lifetime improvements for write-intensive applications
- For heavily read-intensive applications (i.e., web search, MSR-Cambridge),remapping based FCR reduces lifetime (The additional erase cycles lead to decreased lifetime)

Flash Lifetime with Adaptive-Rate FCR



- Adaptive-rate FCR improves lifetime over both periodic FCR mechanisms for all workloads as it avoids unnecessary refreshes
- Adaptive-rate FCR can improve lifetime for read-intensive workloads
- Average lifetime improvement over no-refresh
  - Adaptive 46x, Hybrid FCR 30x and remapping FCR 9x

Conclusions

- Stronger ECC has diminishing returns on improving endurance and lifetime of NAND flash based data storage
- Retention-aware error management need to be applied to reduce raw BER of NAND flash memory
  - Re-map based FCR
  - Hybrid in-place and out-place FCR
  - Adaptive-rate FCR
- Adaptive FCR techniques can improve the lifetime of NAND flash memory by ~46x on average with minor overhead

Thank You

Questions?