An LDPC-Enabled Flash Controller in 40 nm CMOS

Marvell Semiconductor

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Outline

- Error correction requirements
- LDPC Codes
- ECC architecture
- SOC integration
- Conclusion

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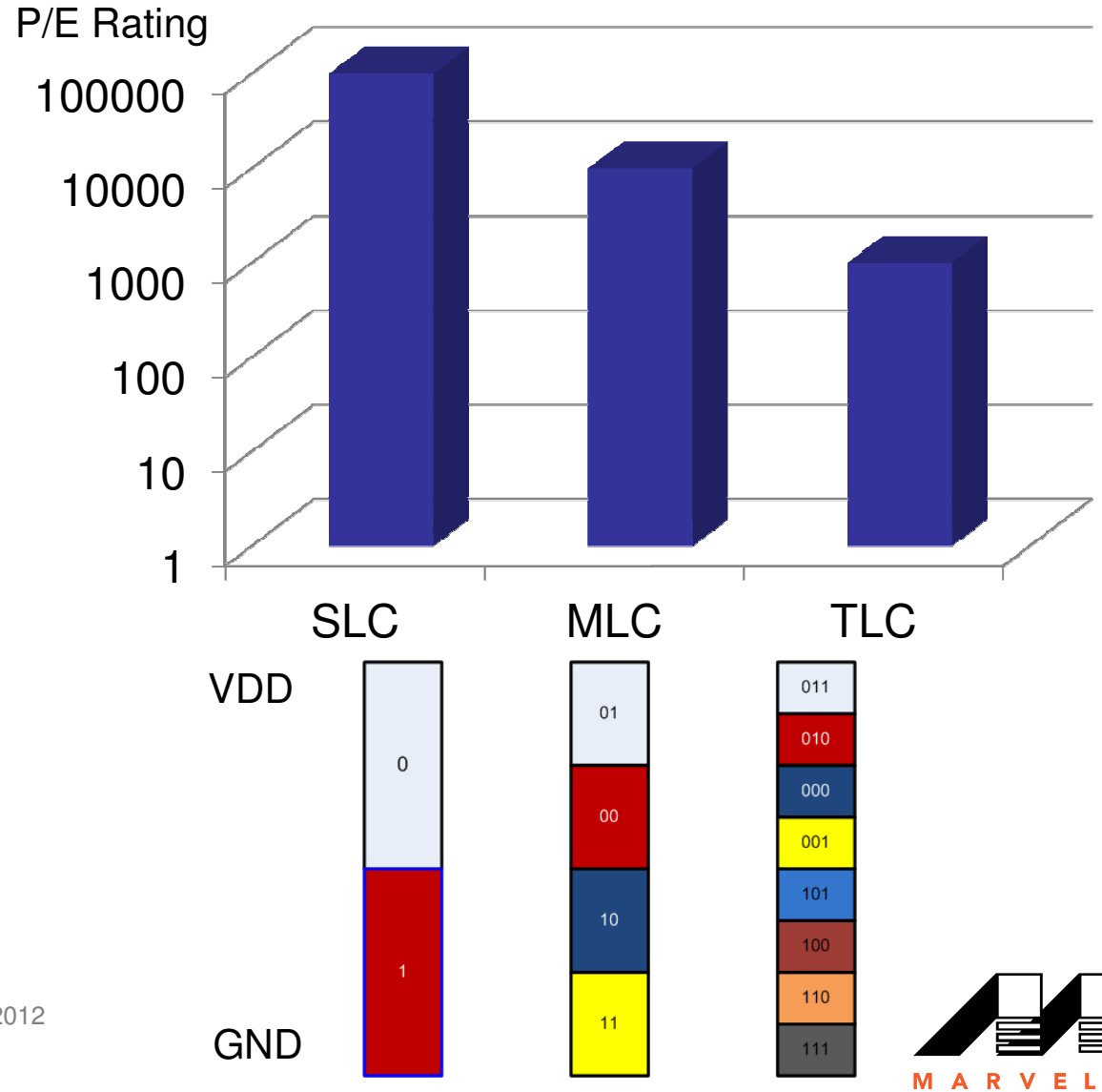
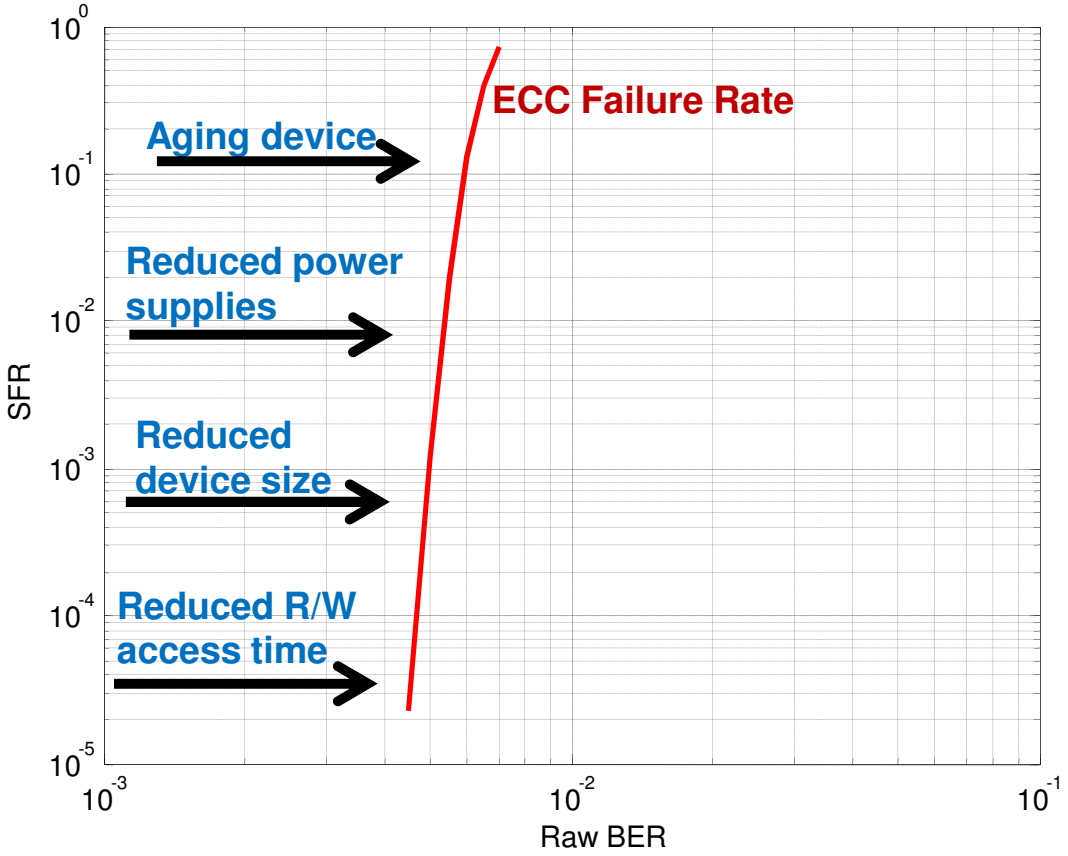
Diminishing P/E Ratings

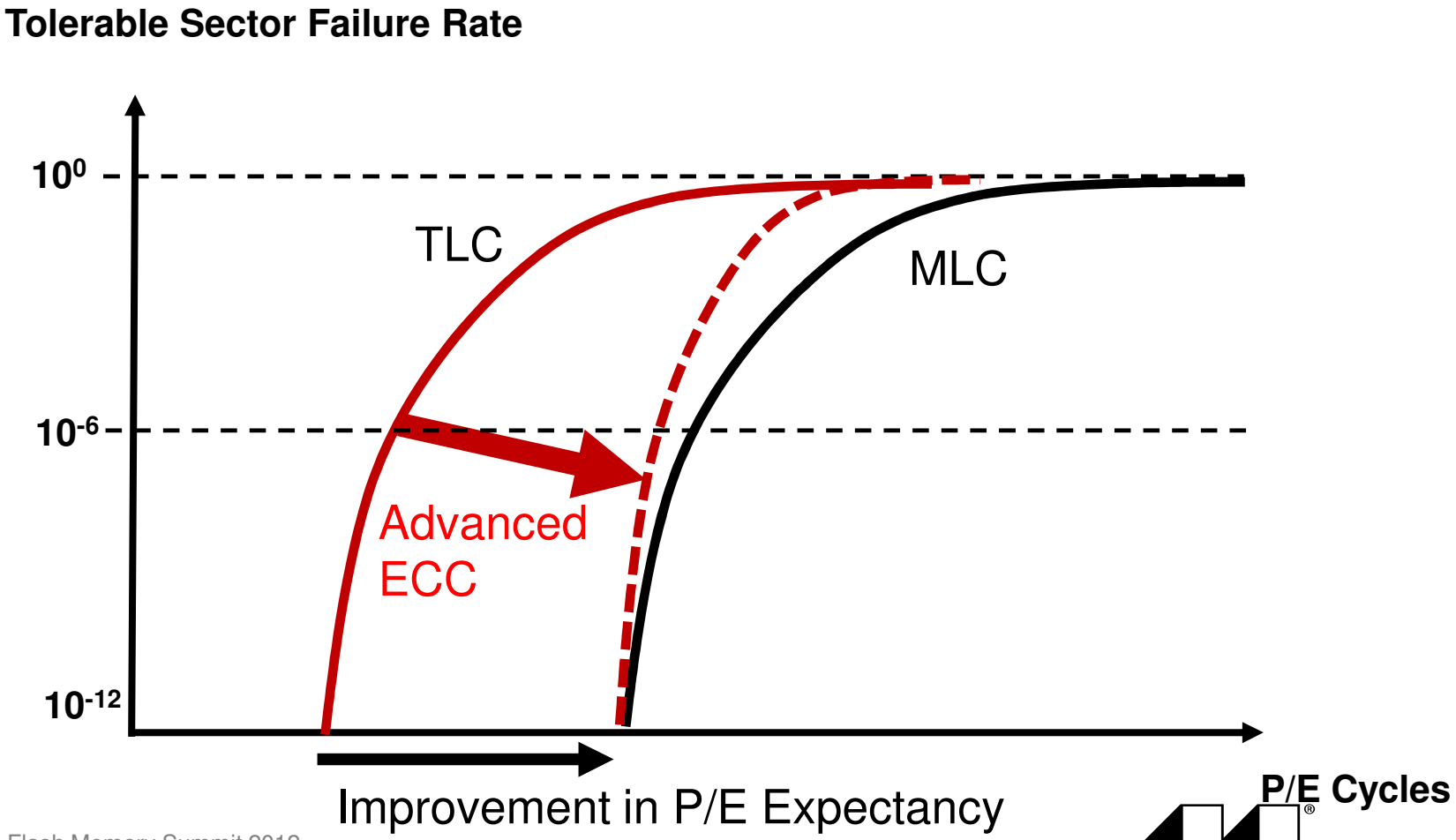


ECC Affects Many Parameters



- Raw BER of device progressively decreases as a result of :
  - Reduced device sizes
  - Reduced power supplies
  - Reduced R/W access time
  - Aging device
- Performance of BCH(t=76) decoder
  - Achieves SFR < 10^{-6} @ RBER= 4 $\times 10^{-3}$

P/E Cycle Expectancy As Function of Sector Failure Rate



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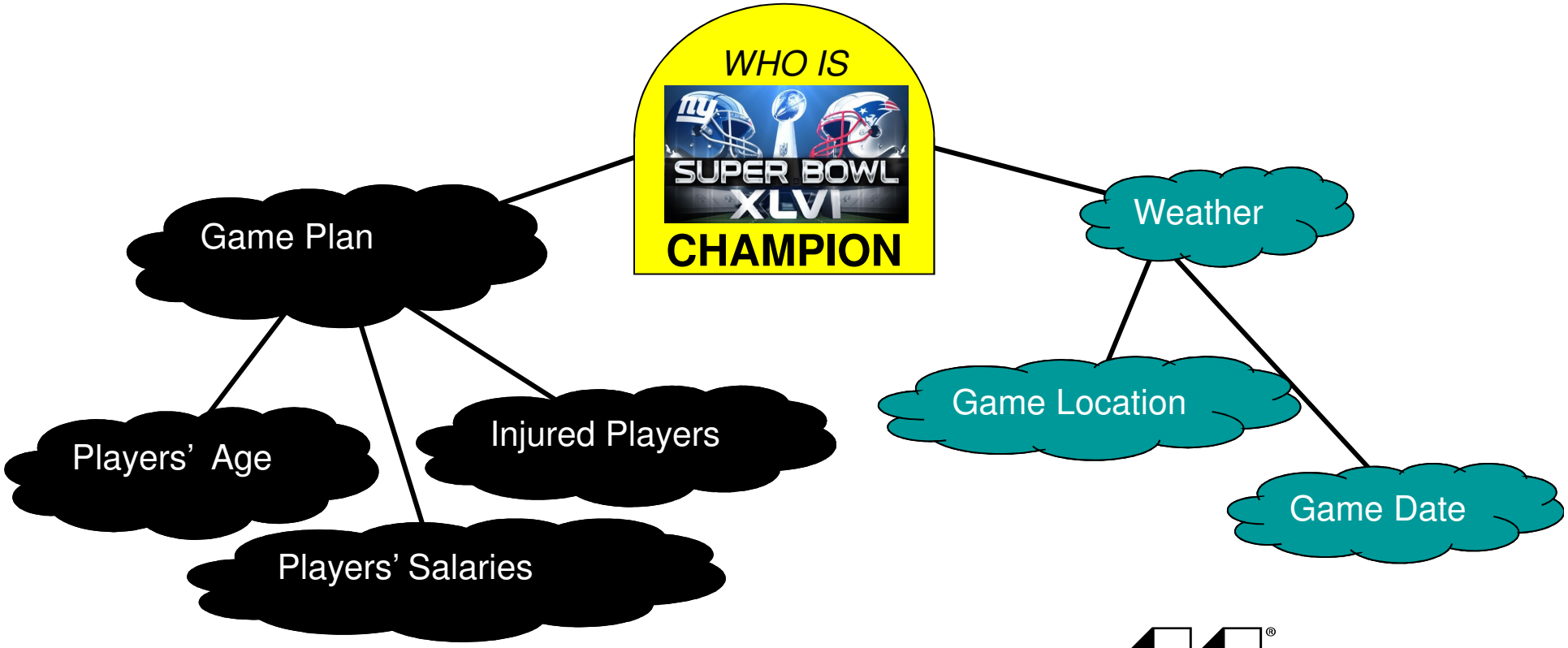
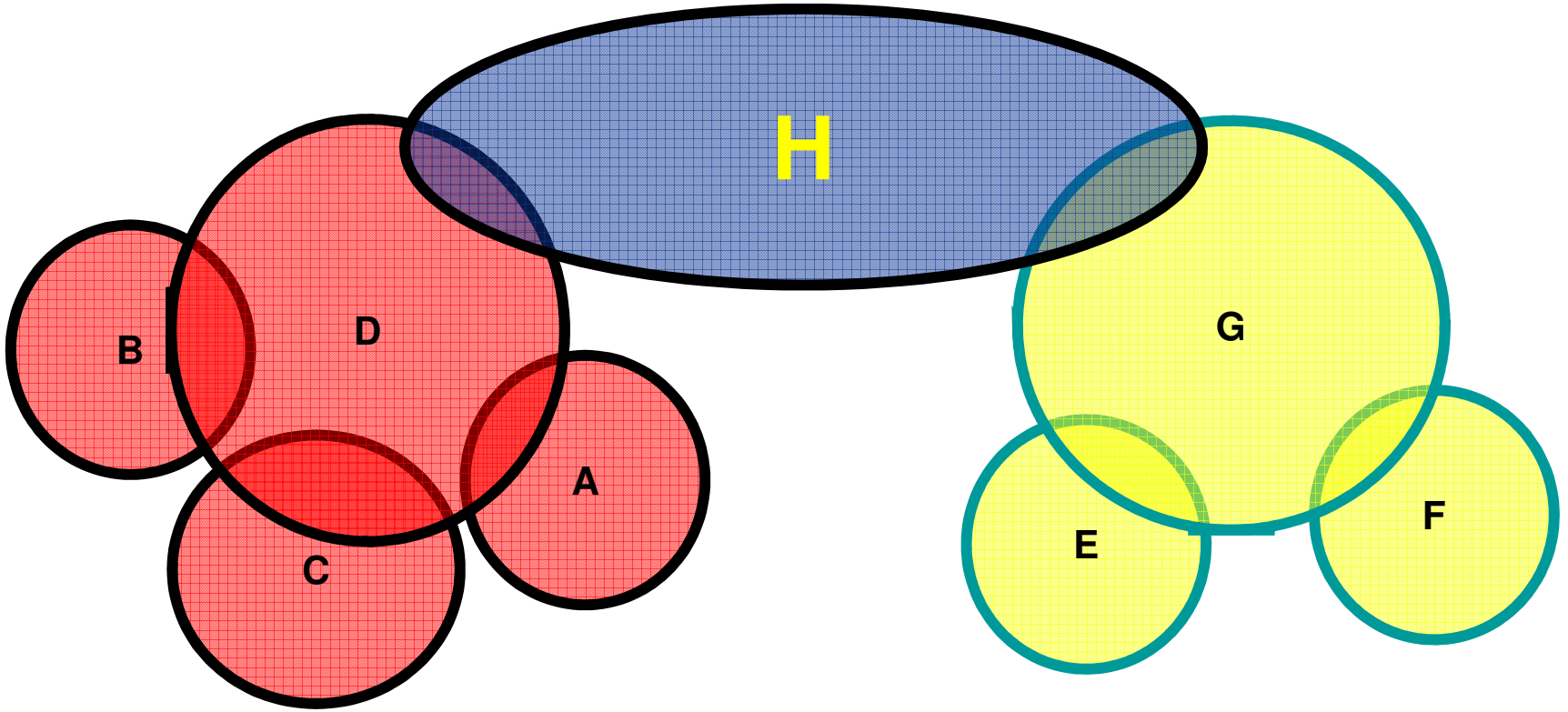
LDPC Decoding: Belief Propagation

- Each event occurs with some prior probability.
- Posterior probability based on inference from a number of related events.



Constrained Coding and LDPC Decoding

- Each set represents a group of constrained bits
  e.g. even parity, cyclic codewords
- Decoding based on inferences passed between adjacent neighbors



Low Density Parity Codes

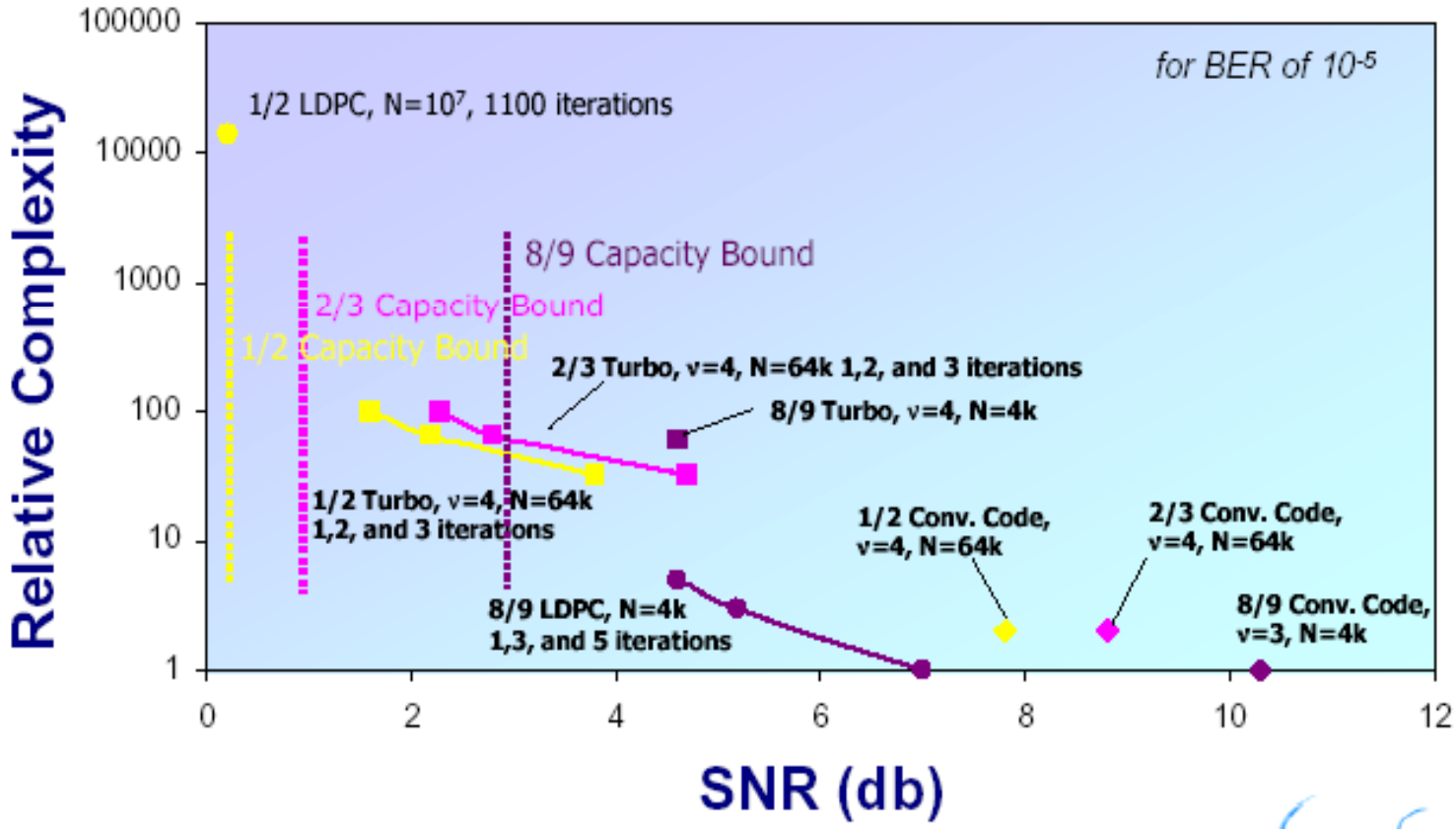
- Advantages:
  - Best class of codes to approach theoretical limits of error correction strengths.
  - Well-studied theoretical approaches in the last decade.
  - Has been deployed in magnetic storage since 2007.
  - Choice error correction codes e.g. IEEE 802.11N, AC, ITU G.hn, 10GBase-T, DVB-S2, etc.
- Disadvantages:
  - Difficult and intractable VLSI implementations.
  - Higher power dissipation than traditional BCH solutions.

Why LDPC?

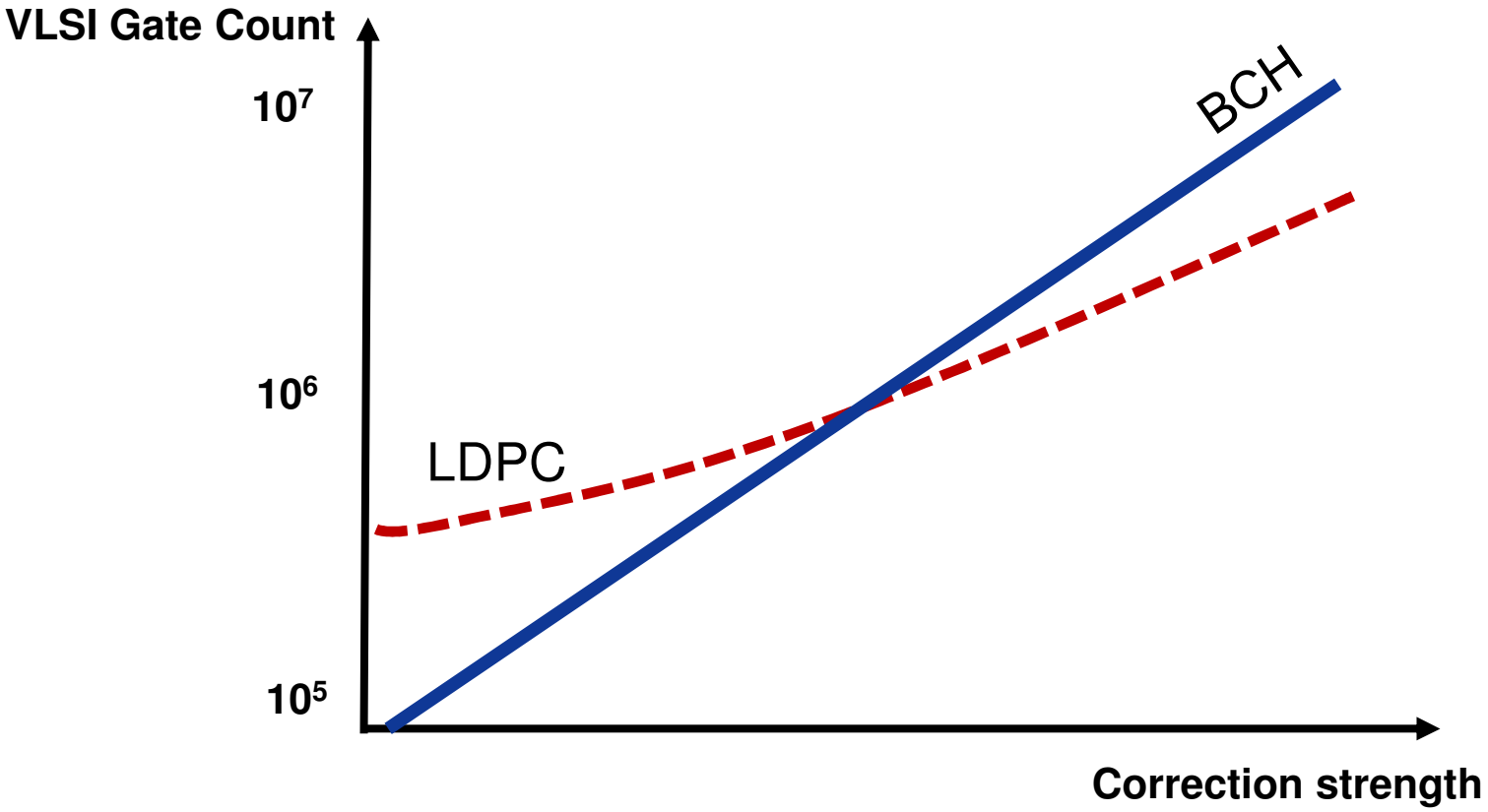
- More stringent demands for error correction capabilities tips the favor towards LDPC decoder.

- LDPC Decoders can provide flexibility in:
  - Throughput. Exploit inherent parallel nature of LDPC decoding
  - Complexity. Tradeoff decoding complexity against error correction strength.

Relative Complexities



Decoder Complexity Comparison



- LDPC decoders have a higher initial barrier, but complexity does not increase as quickly as BCH decoders at higher correction strengths.

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Reliability-Aware ECC Architecture (RAECC)

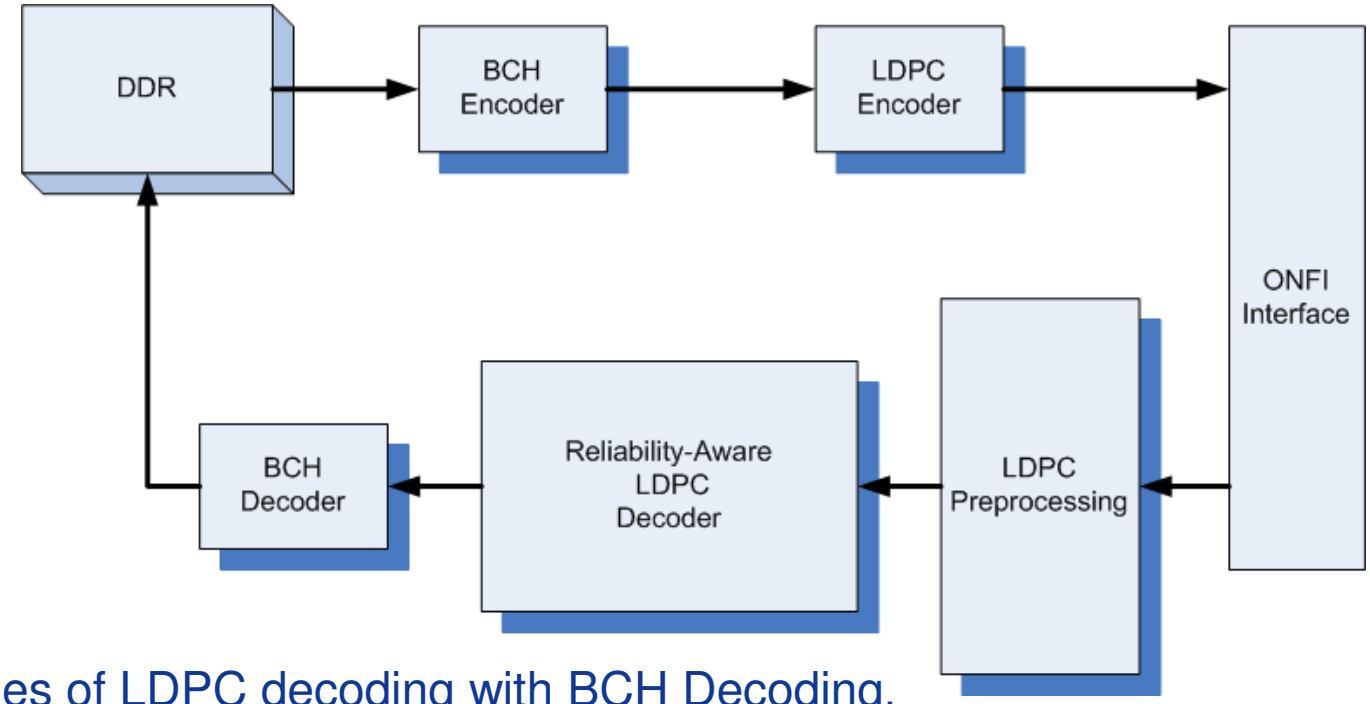
- Exploits unique characteristic of Solid State Memory:

  Data reliability degrades as device ages.

- At the beginning of life, reliability is typically very good.

- However, towards the end of life, the number of blocks that require extensive ECC operation to recover the data becomes higher.

Reliability-Aware LDPC Architecture

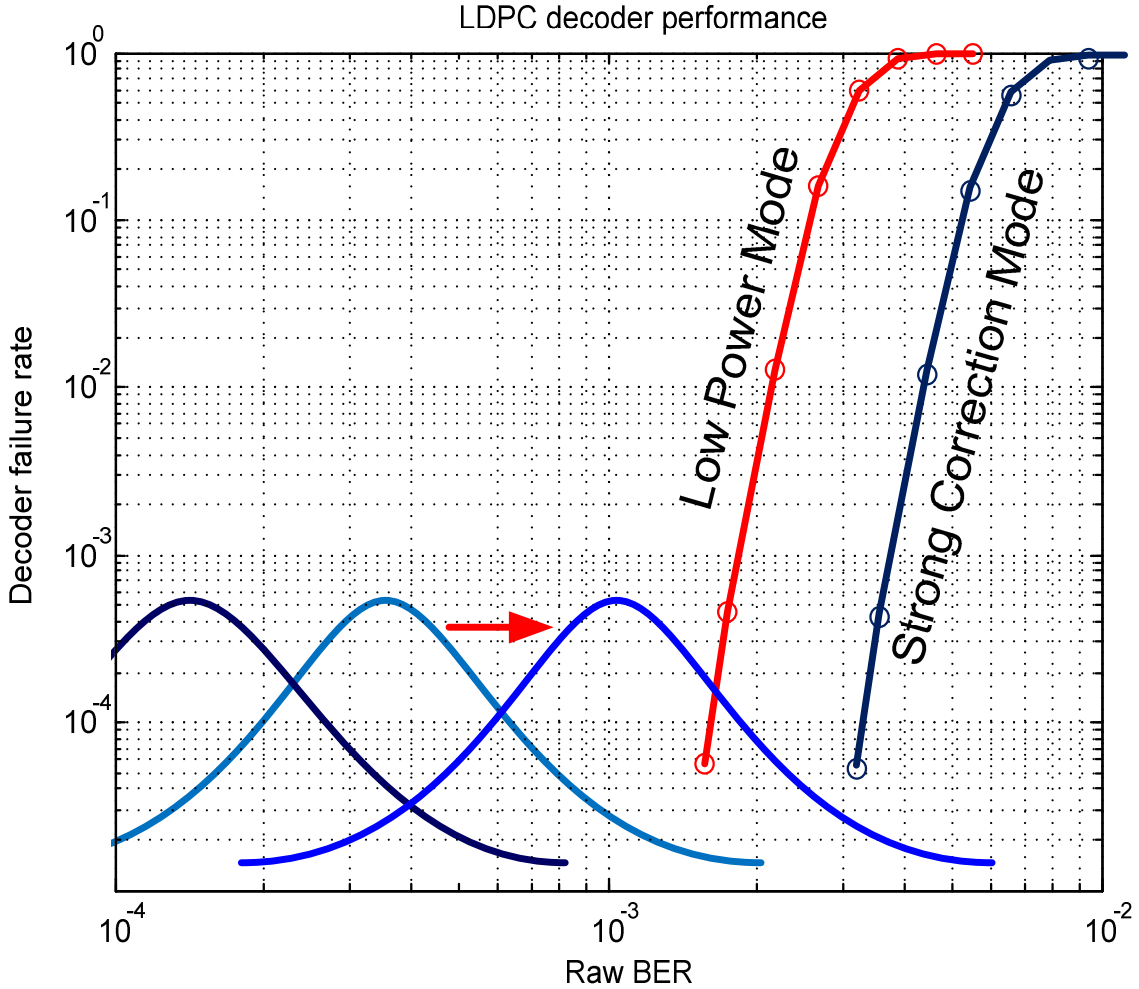


Two modes of LDPC decoding with BCH Decoding.

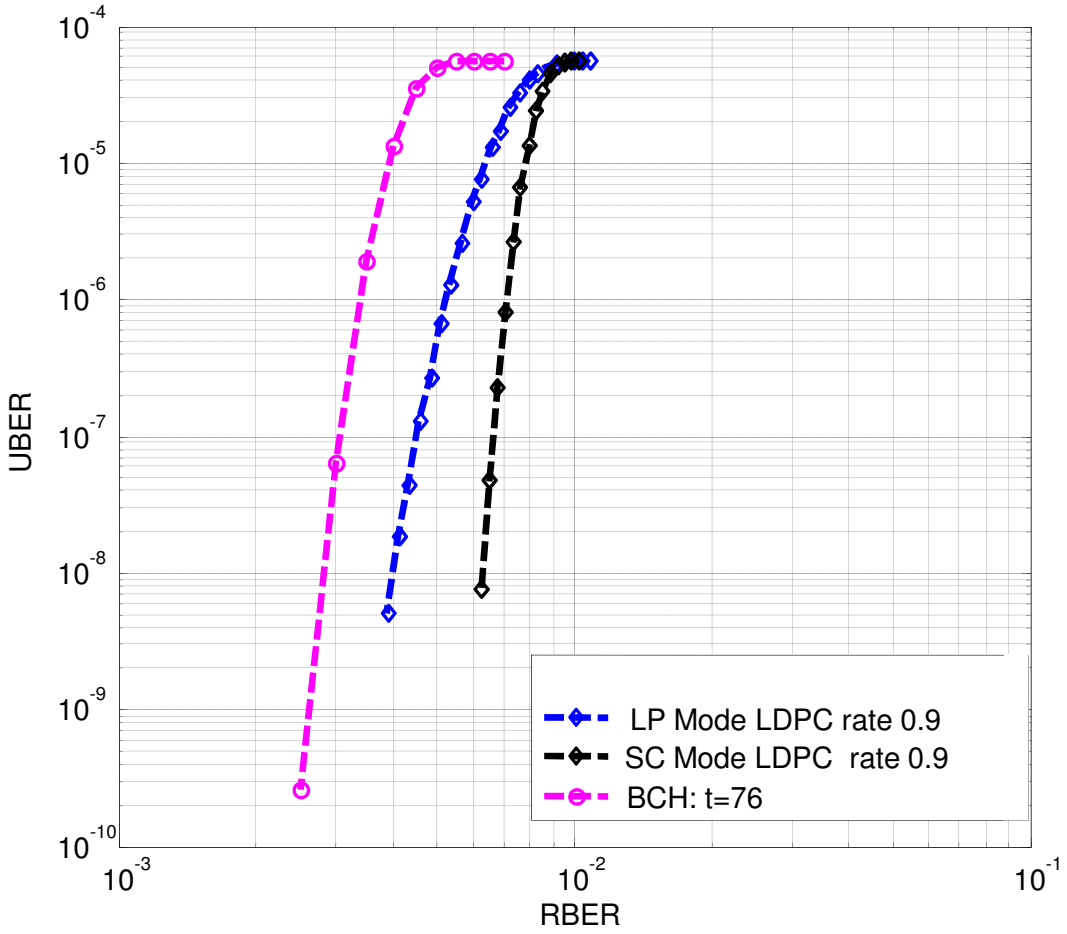
1. Low Power mode (LP-LDPC) can be used with high reliability data (RBER < 10^{-3}).
2. Strong Correction mode (SC-LDPC) provides more error correction, with increased power consumption
3. A low-correction BCH decoder provides guard against weaker performance of LP-LDPC decoder.

Reliability-Aware ECC Architecture (RAECC)

- Pros:
  - low power
  - low complexity,
- Cons:
  - Possible performance degradation at the end of life.



LDPC Performance against BCH t=76



LDPC-based ECC outperforms existing BCH code

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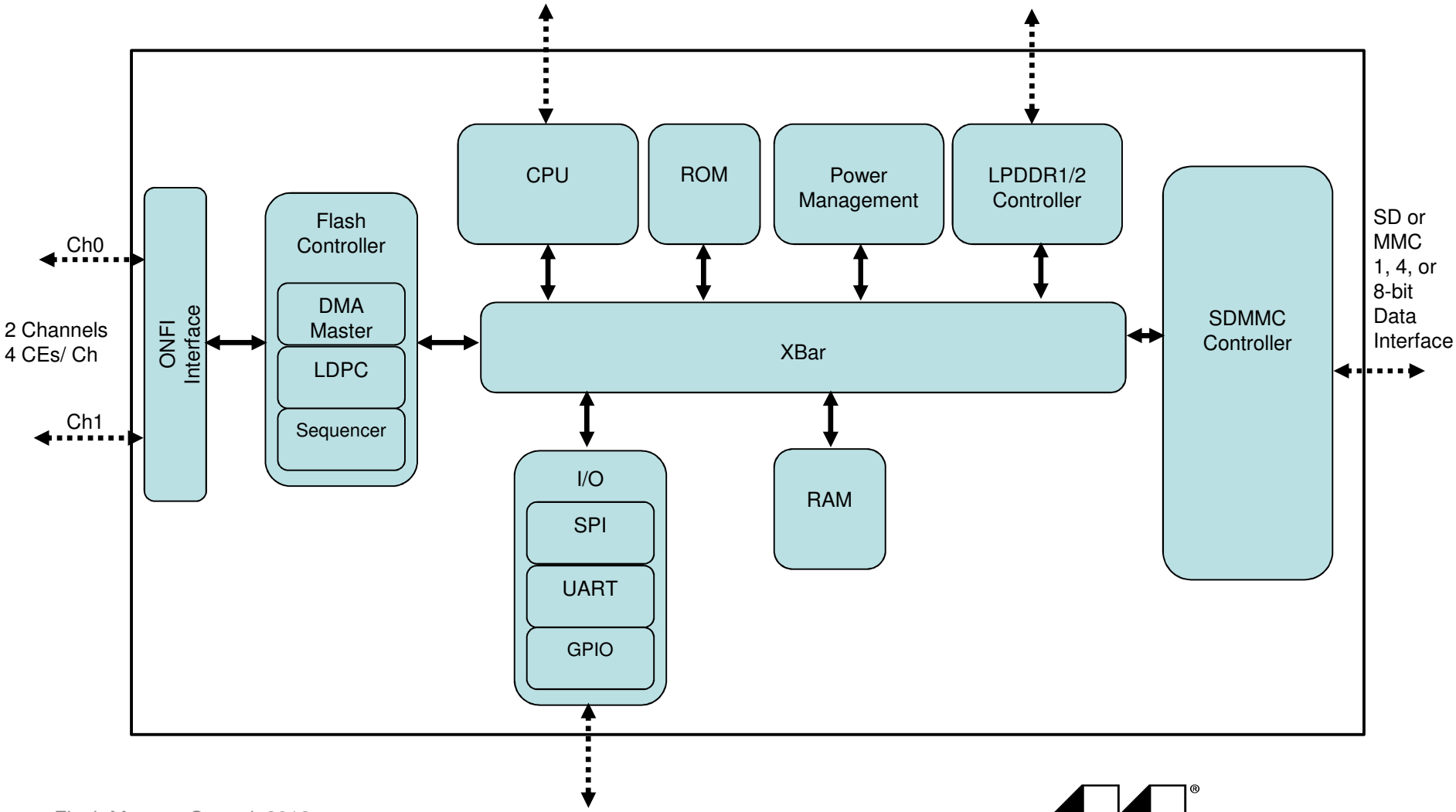
Coeus Flash Controller SOC

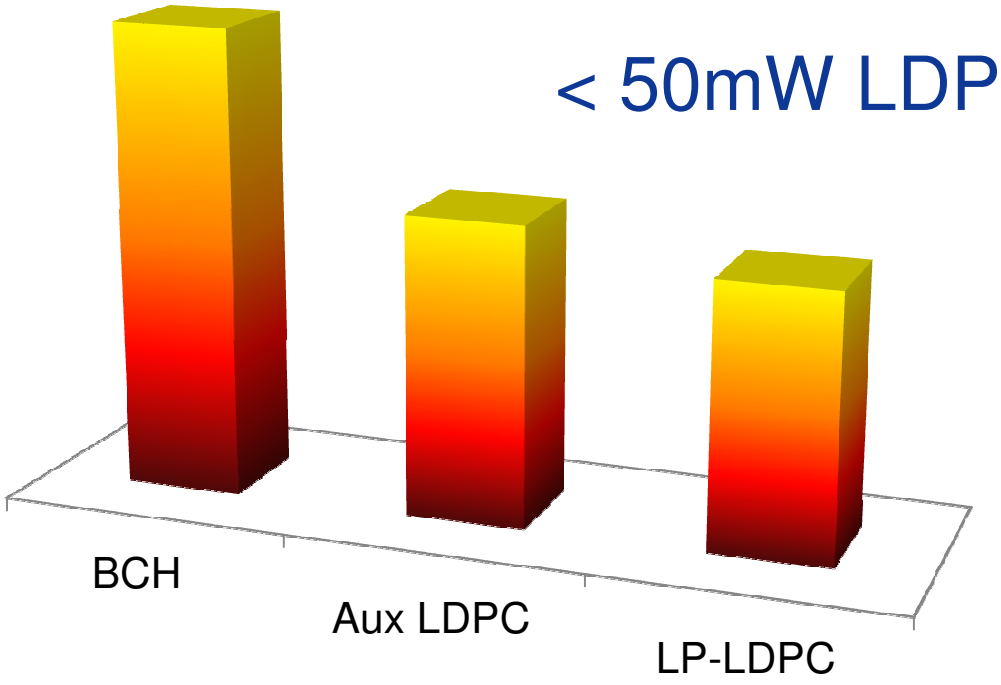
- 40 nm CMOS process
- Enhanced Reliability-Aware LDPC ECC engine
- Support for two channels of NAND flash devices with 4 Chip Enable (CE) per channel
- Support for ONFI 1, ONFI 2.0, ONFI 2.2, ONFI 2.3, and Toggle mode
- Support for MMC and embedded MMC (eMMC) host interfaces
- Embedded ARM CPU core
  - ARM V6T2 architecture with Thumb-2 support

Coeus Architecture

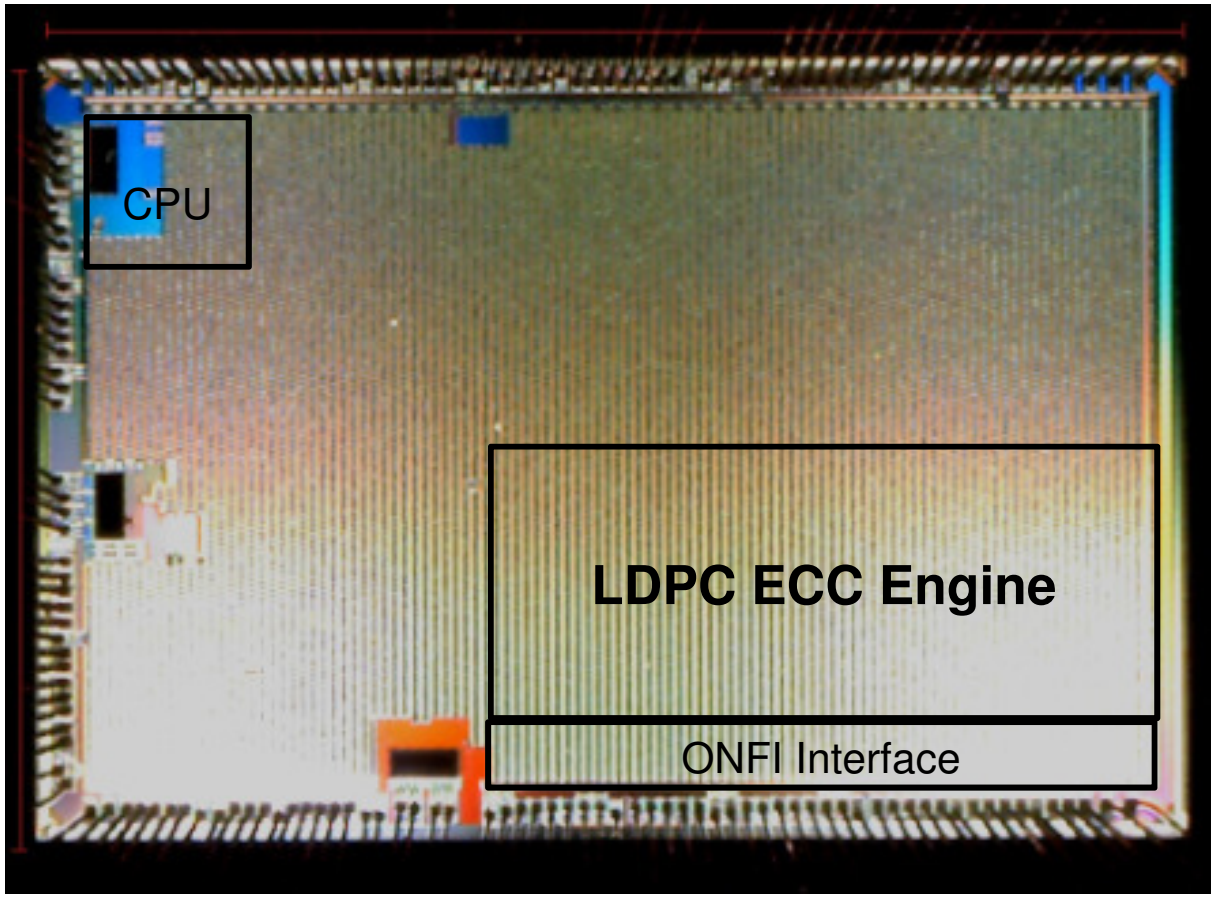


LDPC consumes less power than BCH at the same correction strength

< 50mW LDPC Read Power



Coeus NAND Flash Controller SOC



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Conclusion

- Reliability-aware LDPC architecture combines a low-power mode with a strong correction mode to provide optimal correction-power tradeoff at various stage of NAND life cycle.
- Lower power dissipation than traditional BCH ECC.
- See you at Marvell Semiconductor Booth 800-802