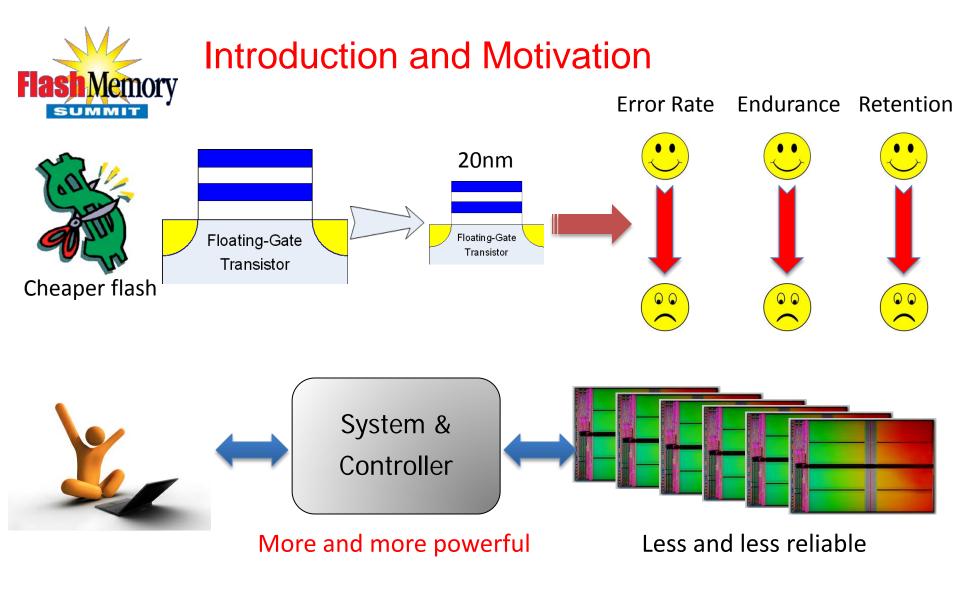


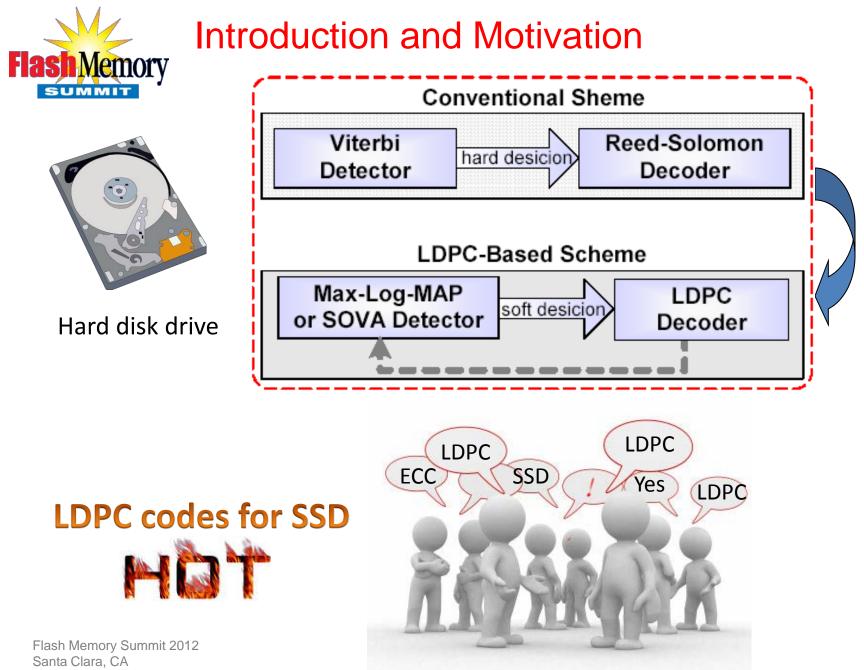
Using LDPC Codes in SSD ---- Challenges and Solutions

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Stronger Error Correction Codes





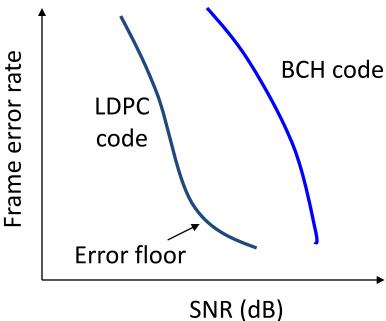
LDPC for SSDs: Challenges

? Error floor of LDPC codes

- ? Memory read latency overhead
- ? Low-cost, high-speed LDPC decoder implementation



Error Floor of LDPC Codes



Nature of iterative codes

lacksquare Impossible to eliminate error floor $oldsymbol{arepsilon}$

Sufficient coding gain in practically interested frame error rate region



Construct LDPC code with sufficiently low error floor





♦ General-purpose Parallel Computing Facility

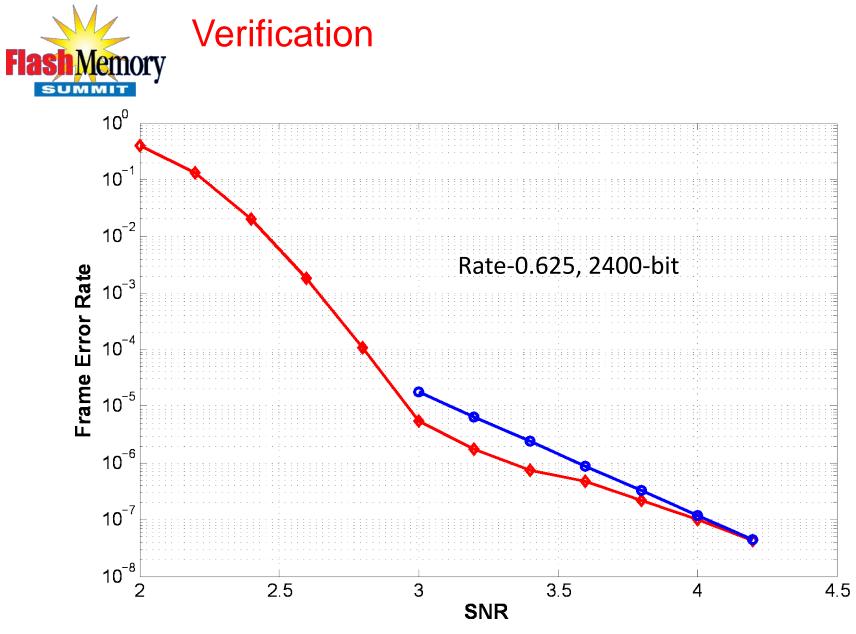
□ A software tool set for LDPC code error floor estimation

□ Fully tested by running on 8192 cores in a super computer cluster

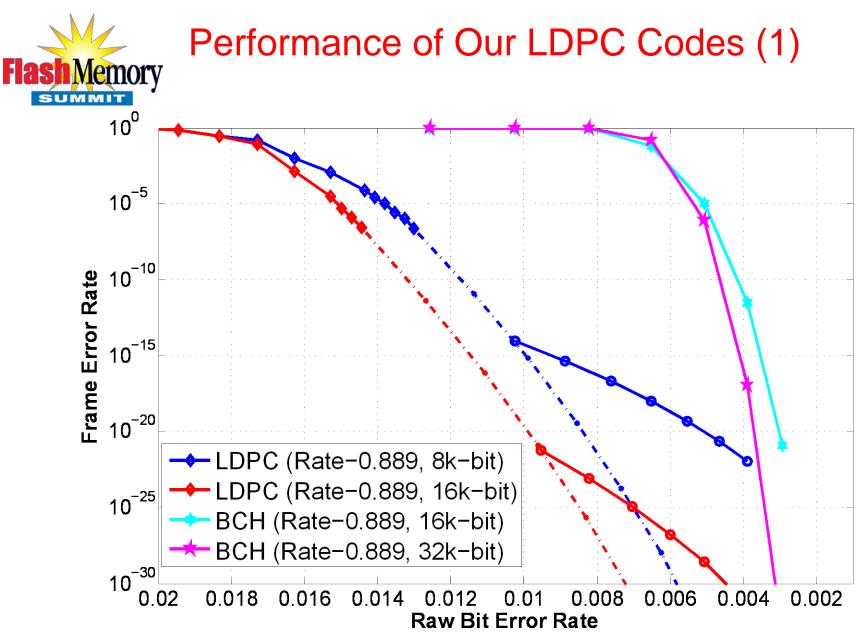
□ Many algorithms/techniques to improve both <u>accuracy</u> and <u>speed</u>

Estimate the error floor of a 16k-bit LDPC code in just one day

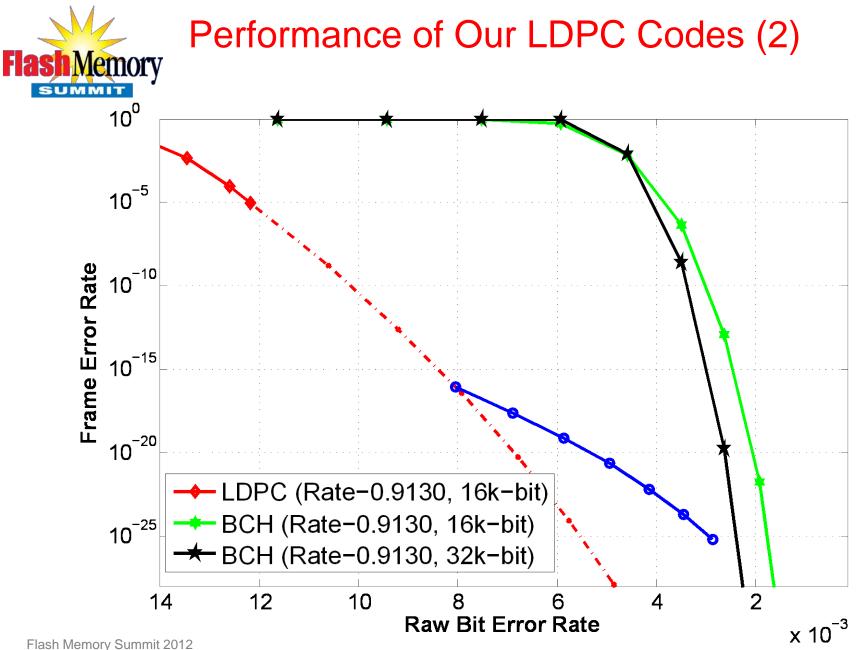
A tool set to construct LDPC codes with low error floor

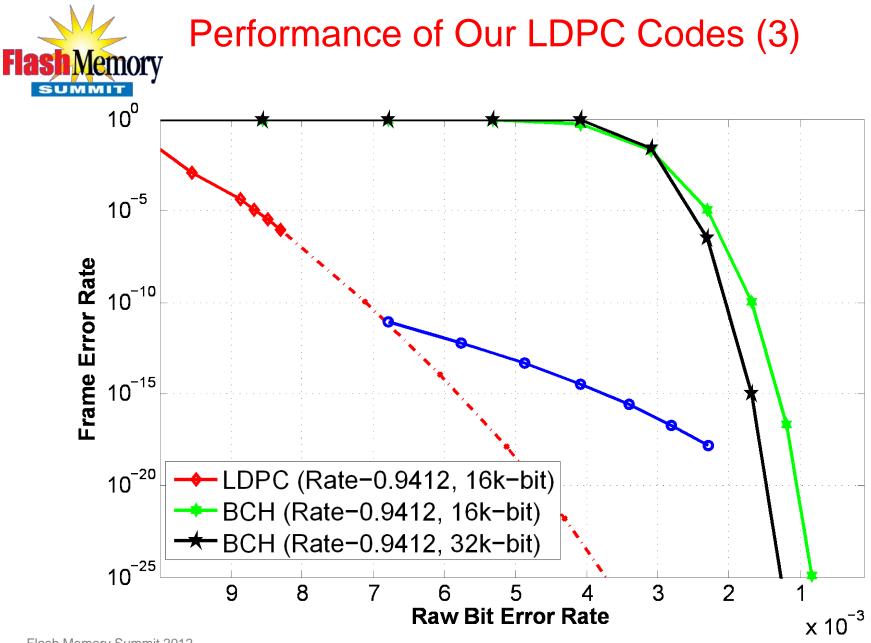


Flash Memory Summit 2012 Santa Clara, CA



Flash Memory Summit 2012 Santa Clara, CA





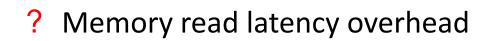
Flash Memory Summit 2012 Santa Clara, CA

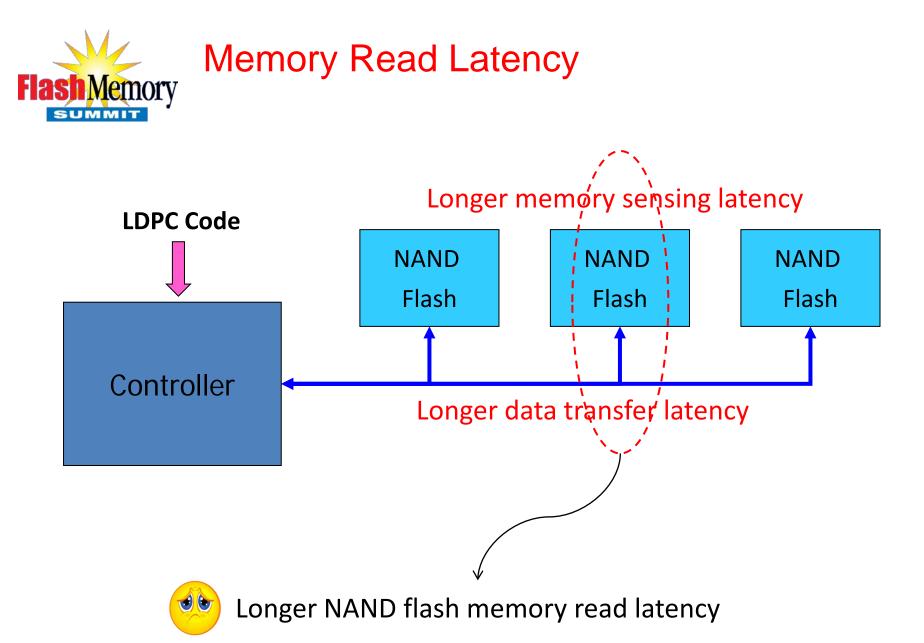


Estimation of LDPC code error floor

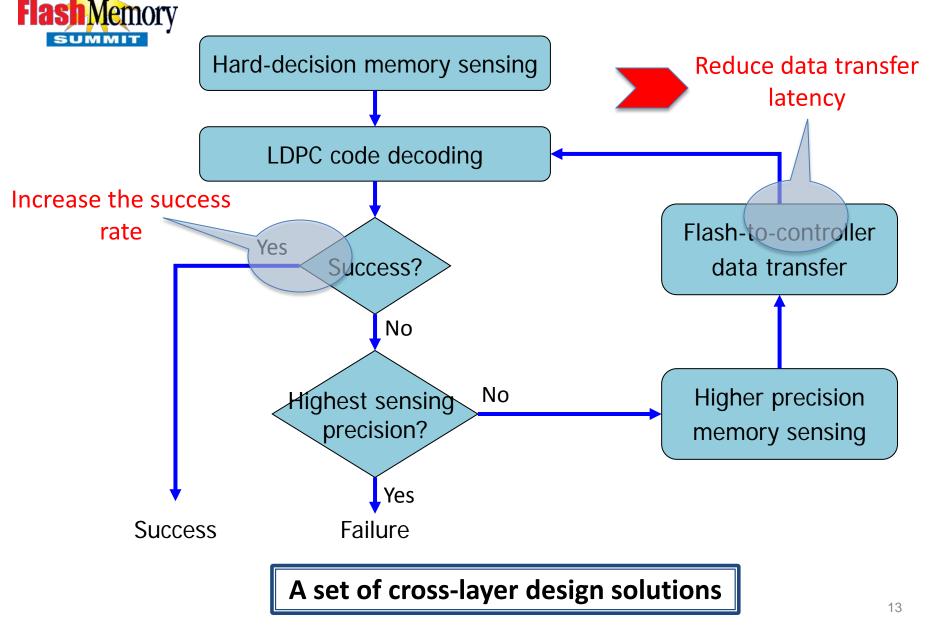








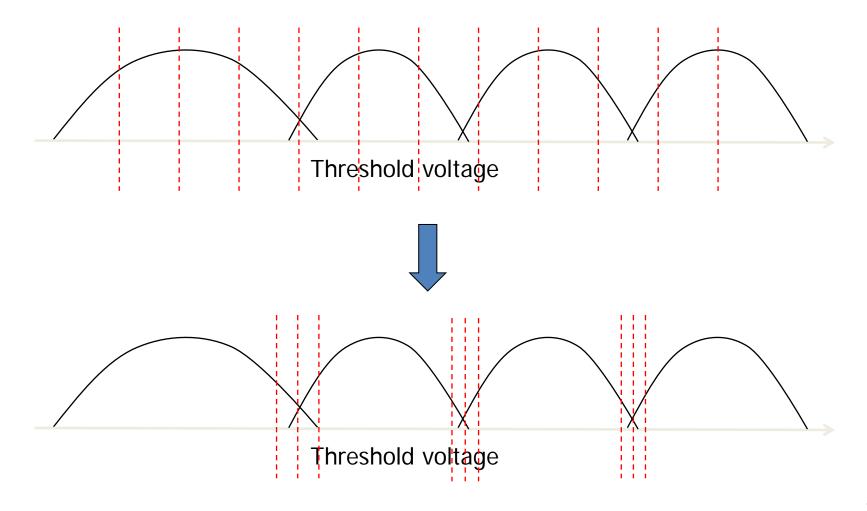
Progressive Soft-Decision Memory Sensing

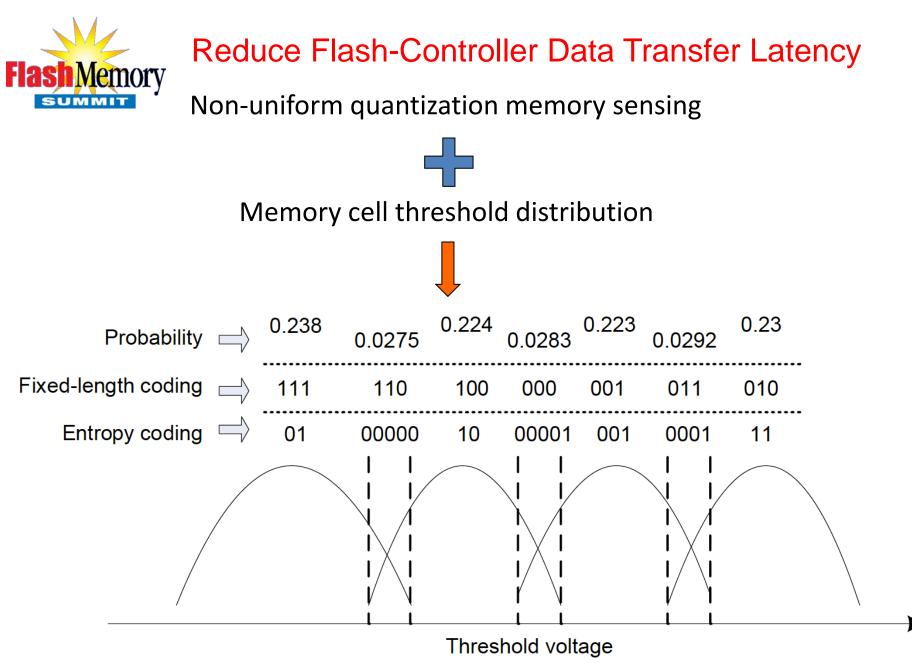




Reduce Read Latency Overhead

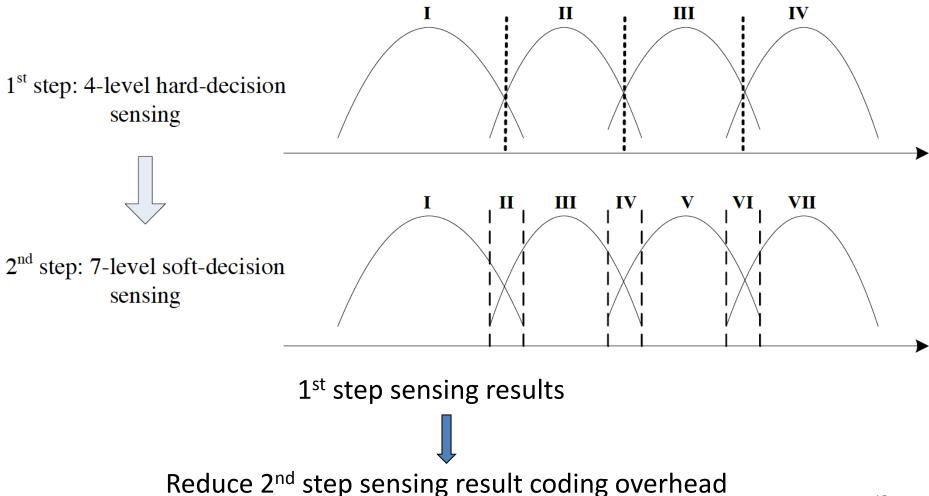
□ Non-uniform quantization memory sensing





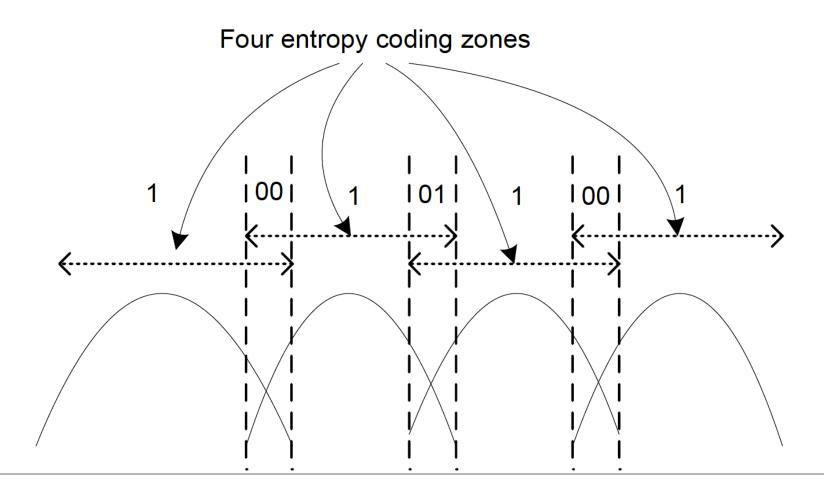


Progressive soft-decision sensing





Progressive soft-decision sensing \rightarrow zoned entropy coding



Threshold voltage



Probabilities and codewords of 2nd-step soft-decision sensing results.

Level	Probability	Fixed-length	Entropy	Zoned
index		coding	coding	Entropy
		-		Coding
Ι	0.2397	111	01	1
II	0.0255	110	00000	00
III	0.2255	100	10	1
IV	0.0263	000	00001	01
V	0.2245	001	001	1
VI	0.027	011	0001	00
VII	0.2315	010	1.1 /	

20.4% reduction of transfer latency <

64.8% reduction of transfer latency <

LDPC for SSDs: Challenges & Solutions

? Error floor of LDPC codes

- ✓ A tool set for LDPC code error floor estimation
- ✓ A tool set for low-error-floor LDPC code construction
- ? Memory read latency overhead
 - ✓ A set of cross-layer design solutions to
 - 1. Increase decoding success rate at lower sensing precision
 - 2. Reduce soft-sensing data transfer latency

