Mechanism of Switching and Related Challenges in Transition Metal Oxide Based RRAM Devices

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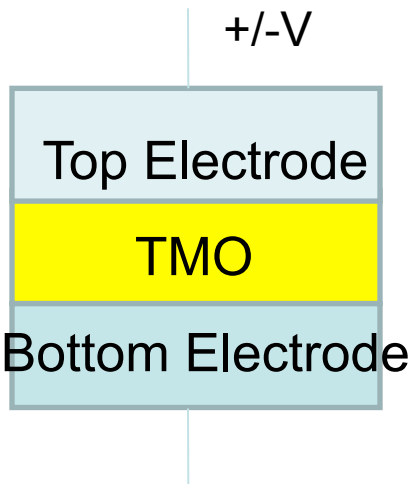
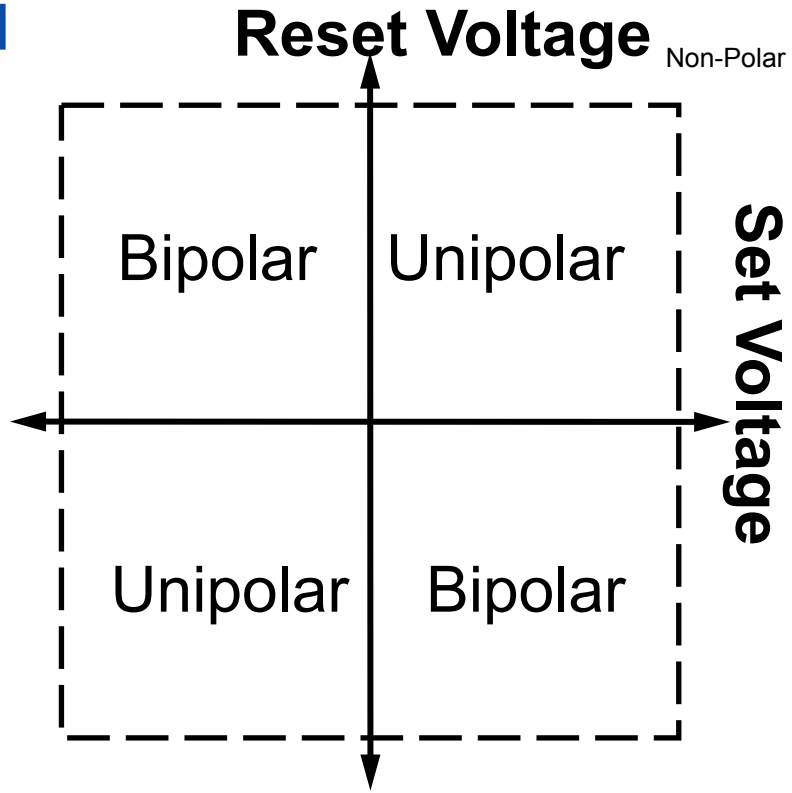
ReRAM Materials and Switching

- Switching Transition Metal Oxides (TMO): HfO_2, TaOx, TiOx, NiOx, CuOx, AlOx, AlON
- Electrodes: Pt, Au, Ru, TiN



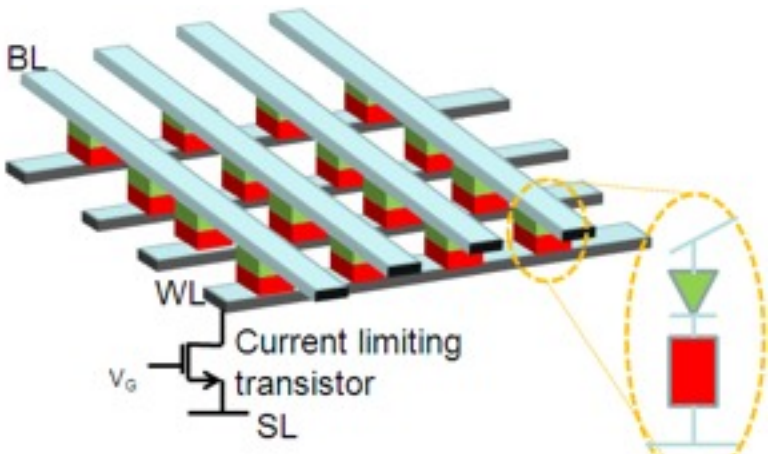


•*Govoreanu et. al., IEDM, 2011*
•*Kim et. al. VLSI Symp. 2011*
•*Waser et. al. , Nature Materials, 2007*

ITRS Roadmap for Non-Volatile Memories

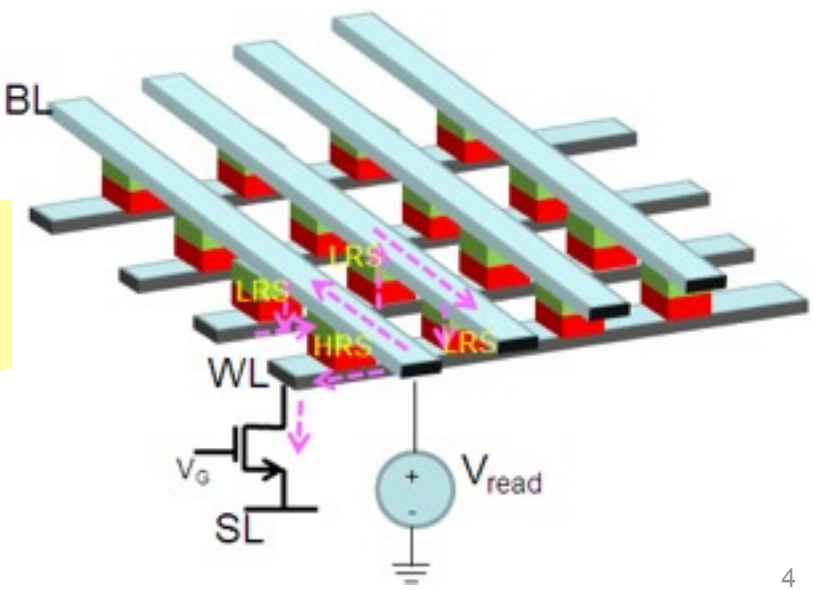
	DRAM	NAND Flash	PCM	FeRAM	STT-MRAM	ReRAM
Feature Size (nm)	36	22	45	180	65	<65
Cell Area	$6F^2$	$4\ F^2$	$4F^2$	$22F^2$	$20F^2$	$4F^2$,$8F^2$
W/E Time	<10 ns	1/0.1 ms	100 ns	65 ns	35 ns	<10 ns
Retention	64 ms	10 y	>10 y	10 y	>10 y	>10 y
Durability	> 1E16	1E4	1E9	1E14	>1E12	**1E12**
W/E Voltage (V)	2.5	15	3	1.3-3.3	1.8	<1
Read Voltage (V)	1.8	1.8	1.2	1.3-3.3	1.8	<1
Write Energy (J/bit)	4E-15	>2E-16	6E-12	3E-14	2.5E-12	**1E-13**

Crossbar Memories with ReRAM



Programming

Reading



Bidirectional Diode is needed to avoid the sneak current.

- *Huang et. al., IEDM, 2011*

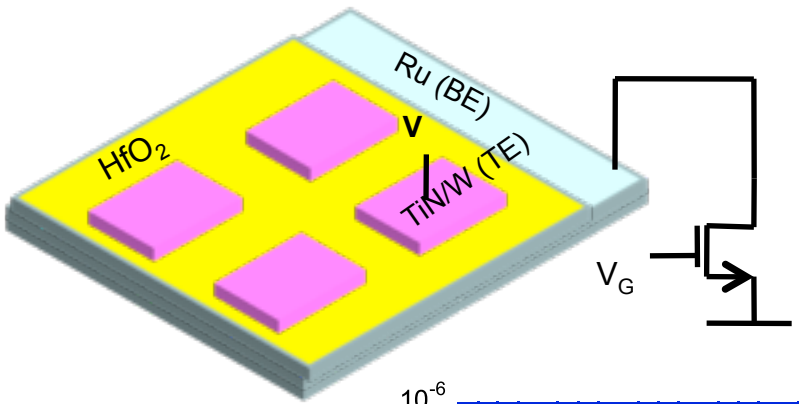
Target Device Specifications

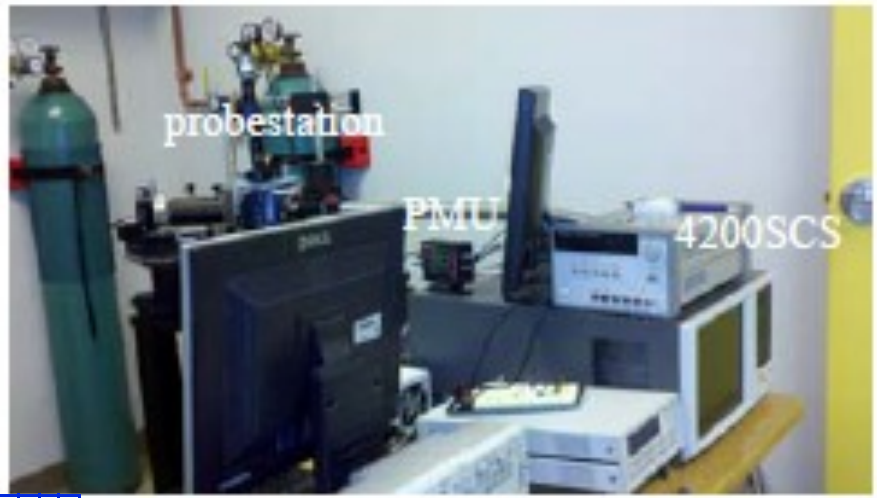
Parameters	ReRAM
V_{set}	~1V
I_{set}	1μA
V_{reset}	-1V
I_{reset}	1μA
T_{switch}	~10-100 ns
ROFF/RON	10-1000
Energy (J/bit)	~$1x10^{-15}$
Endurance	>$1x10^{6}$
Temperatures	85°C

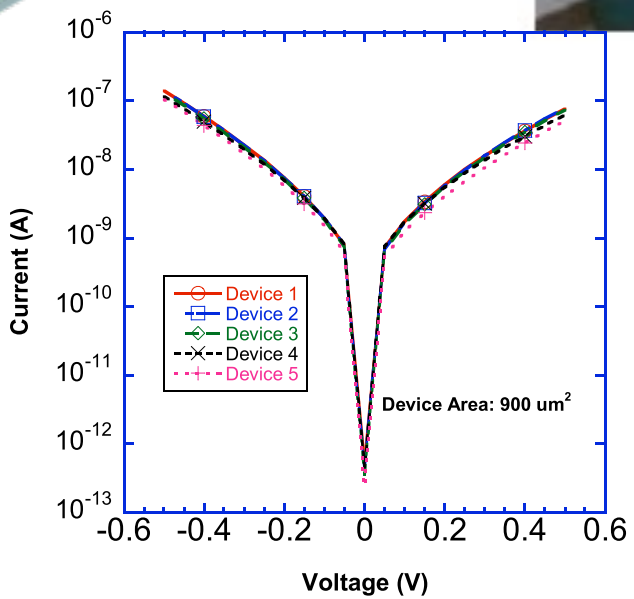
Parameters	Diode
V_{T+}	<1V
I_{ON+}	1μA
V_{T-}	<-1V
I_{ON-}	1μA
I_{ON}/I_{OFF}	>$1x10^{4}$
Temperatures	85°C

ITRS, 2011

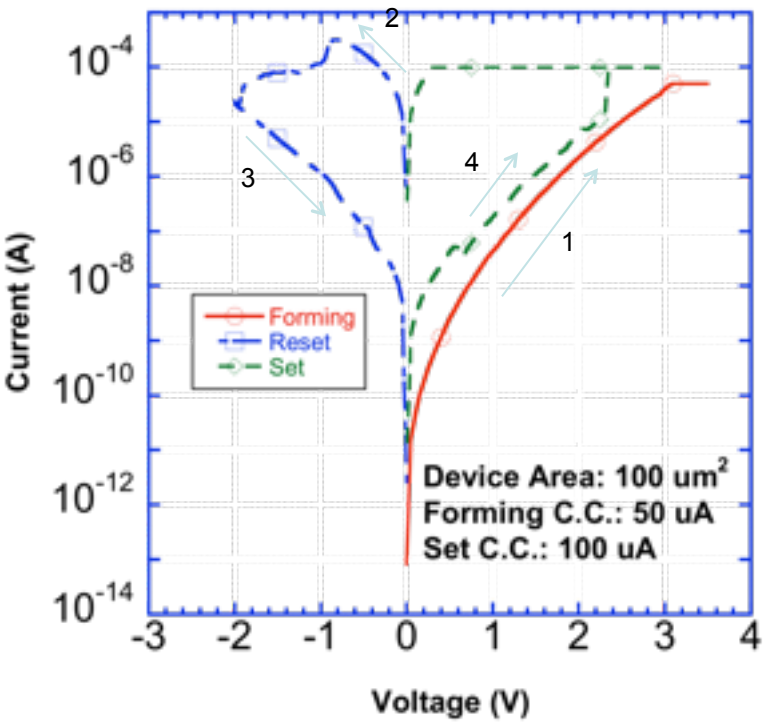
ReRAM Fabrication & Electrical Characterization

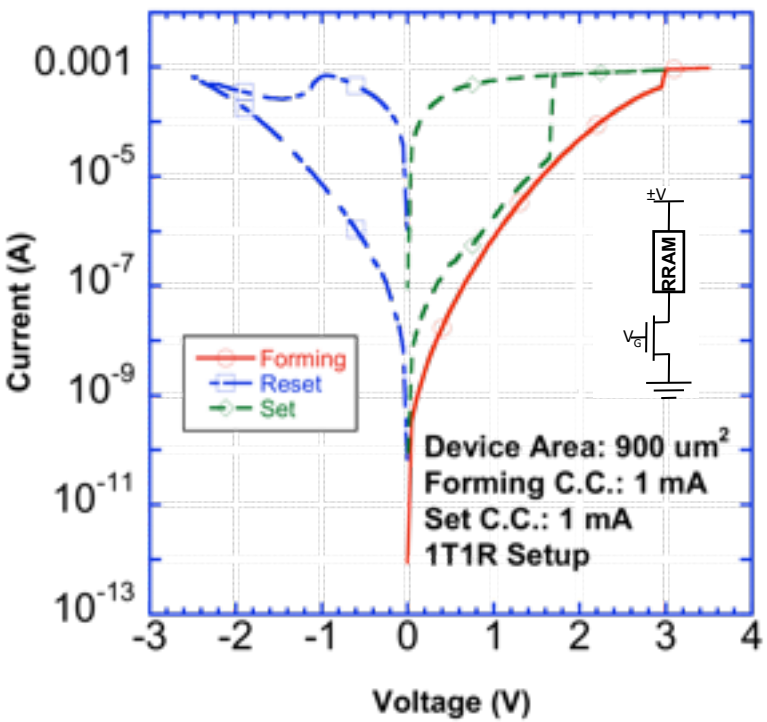




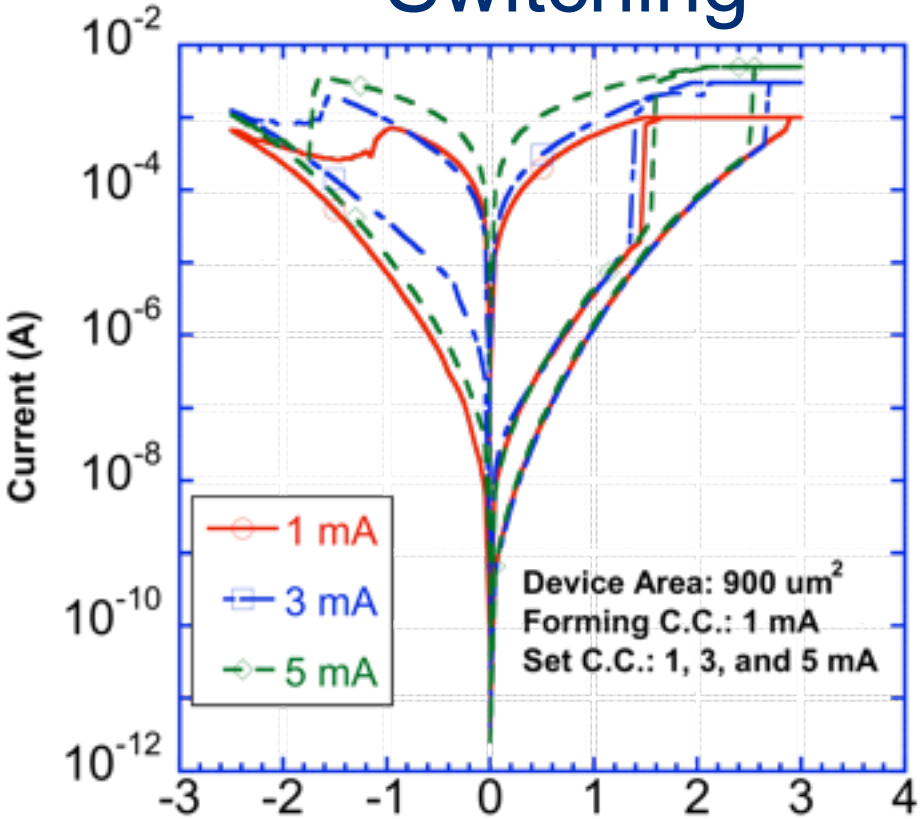


DC Switching Characteristics



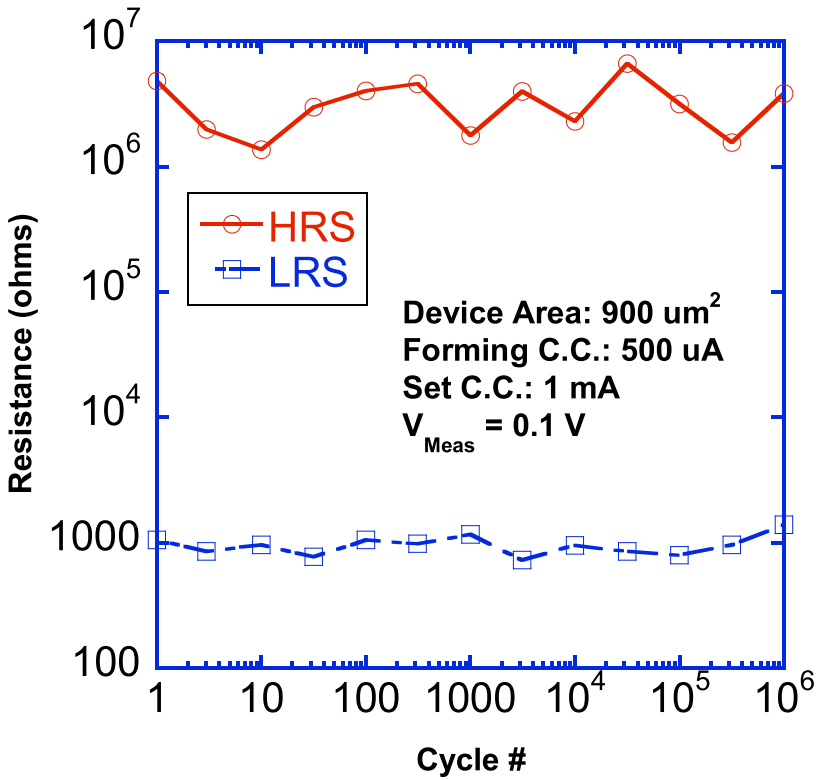


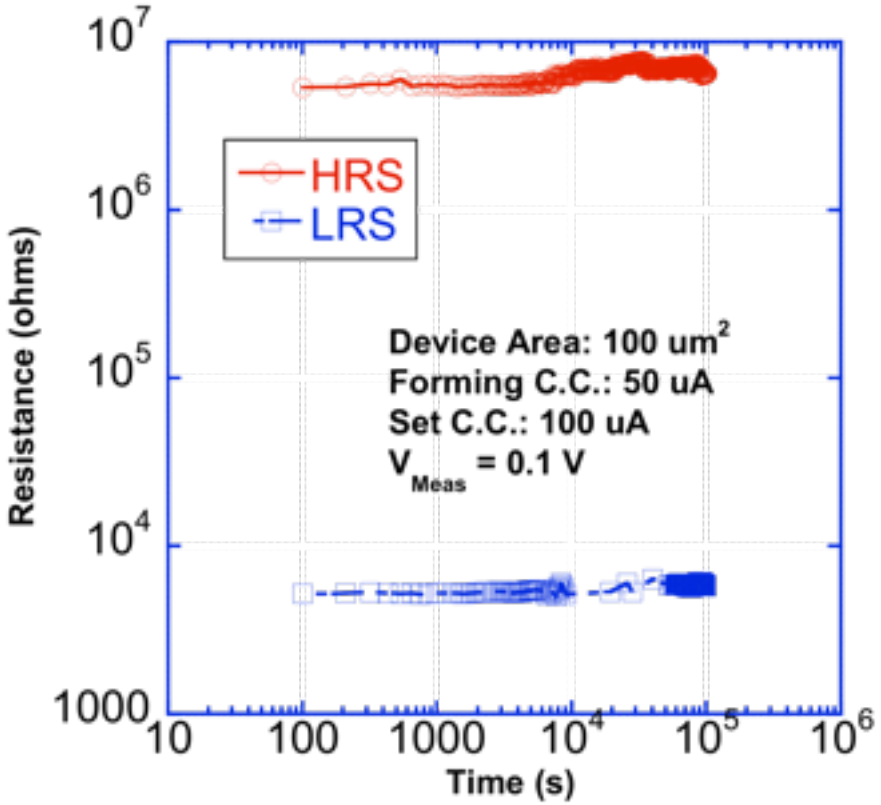
Role of Compliance Current on ReRAM Switching



Compliance current (I_{cc}) plays a major role in governing resistance in LRS, V_{reset}, I_{reset}.

Durability and Retention Testing

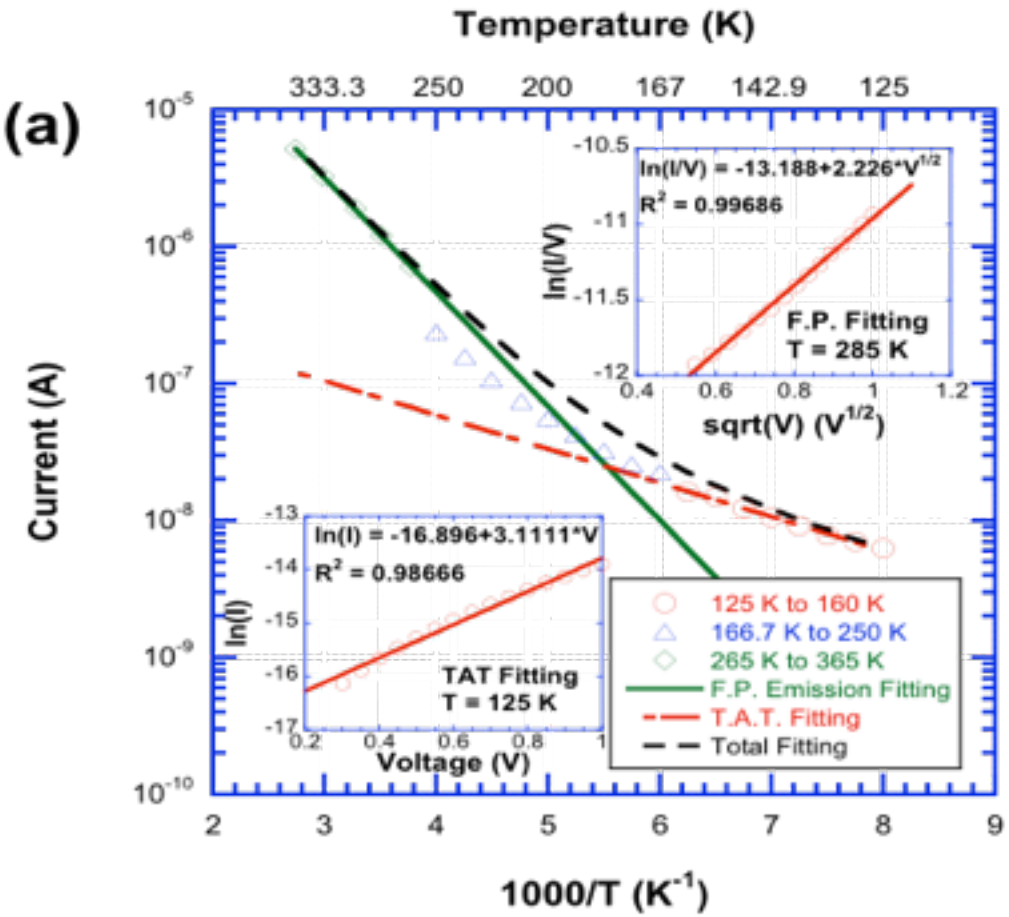




Pulse specifications:

- Rise/Fall Time: 10 µs
- Set Voltage: 3 V
- Reset Voltage: -2.5 V

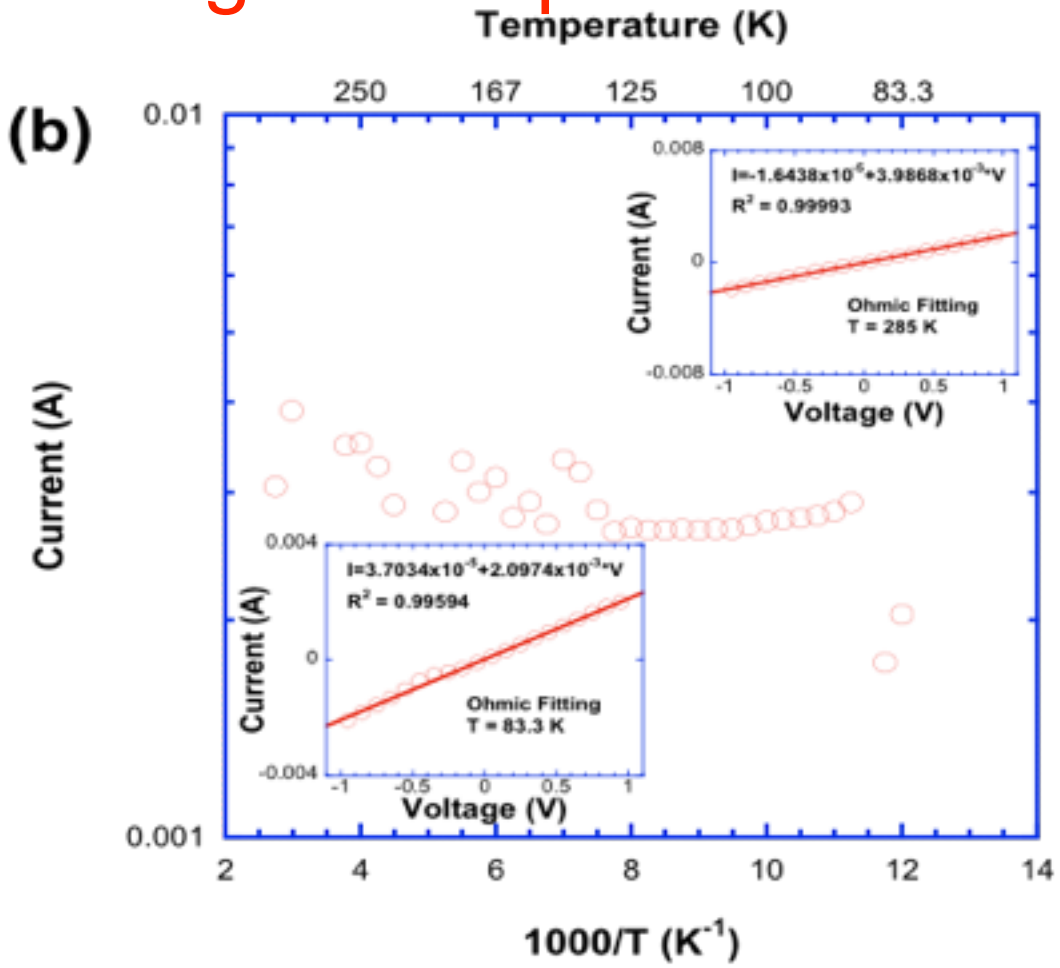
Charge Transport Mechanism: VRS



Conduction mechanism in as-fabricated (VRS) samples is governed by a combination of F-P and TAT through dielectric.

Long et. al, accepted for publication, App. Phys. Lett., 2012

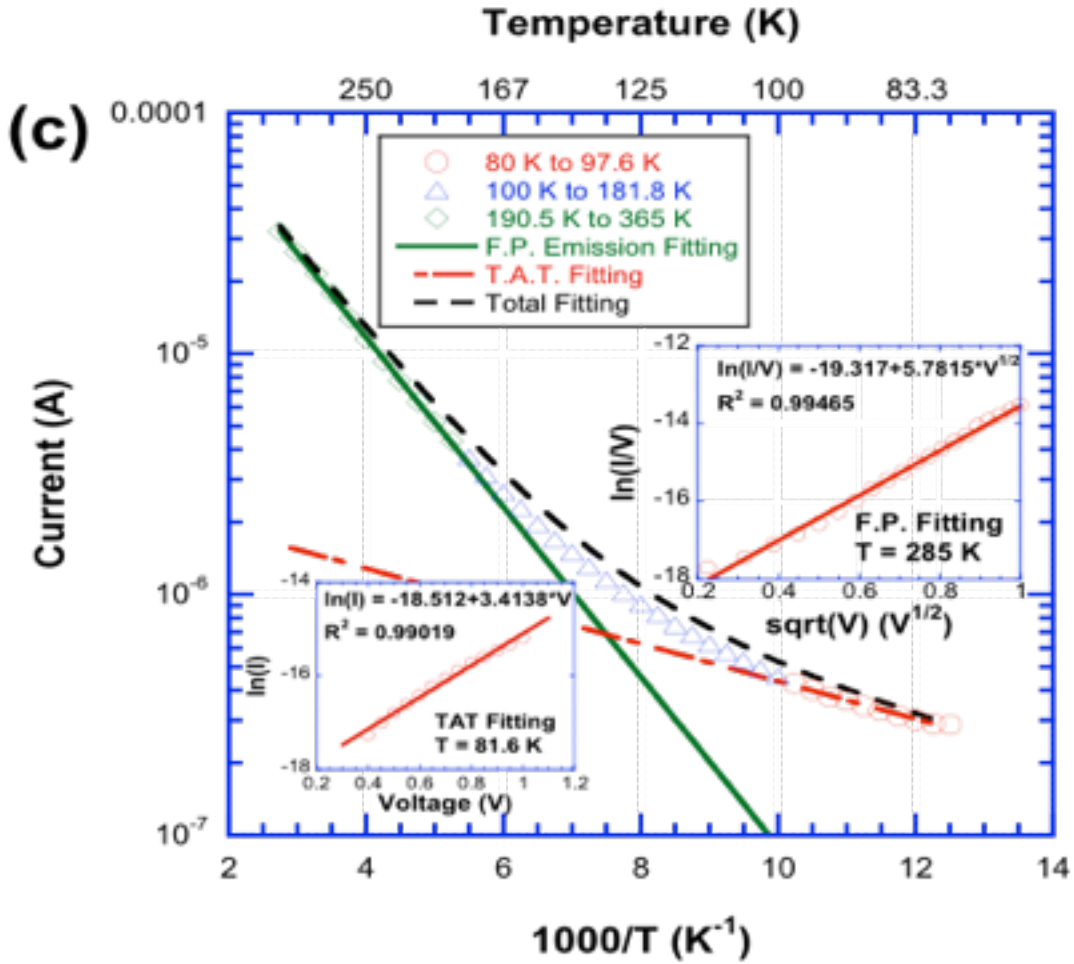
Charge Transport Mechanism: LRS



Conduction mechanism in Low Resistance State(LRS) is governed by Ohmic conduction through dielectric.

Long et. al, accepted for publication, App. Phys. Lett., 2012

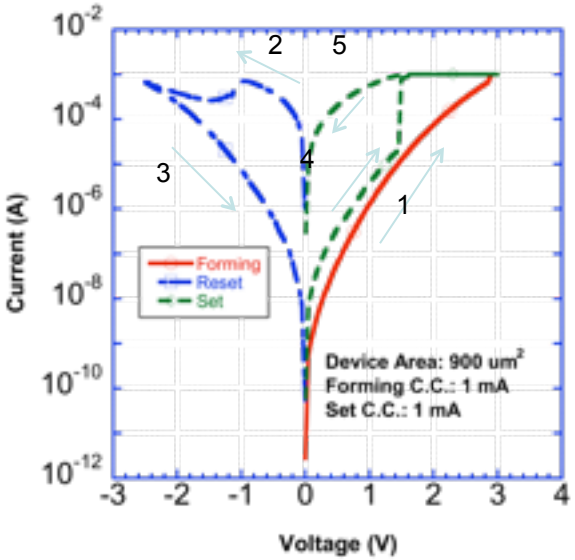
Charge Transport Mechanism: HRS

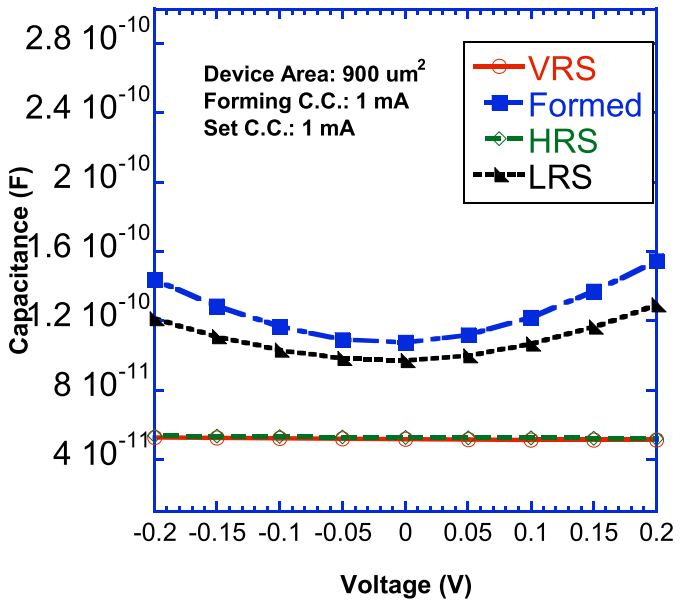


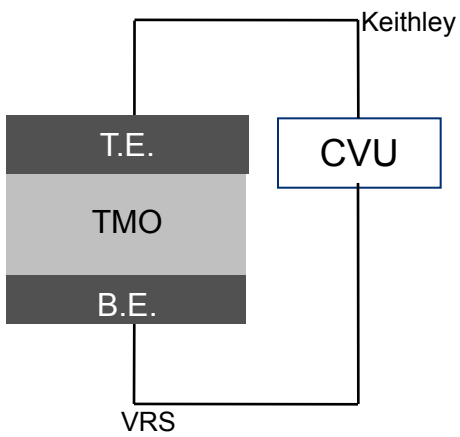
Conduction in High Resistance State(HRS) is governed by a combination of F-P and TAT mechanisms in dielectric.

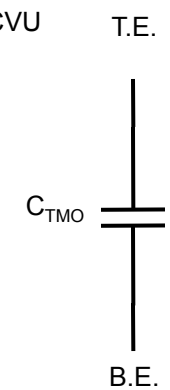
Long et. al, accepted for publication, App. Phys. Lett., 2012

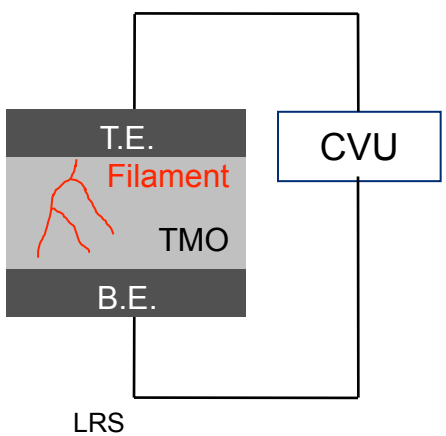
Capacitance in Different Resistive States

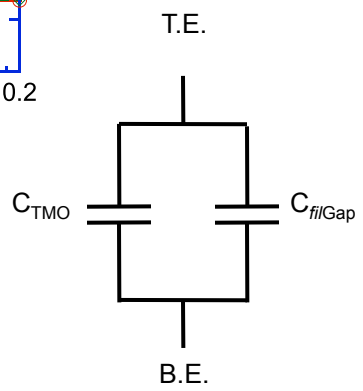












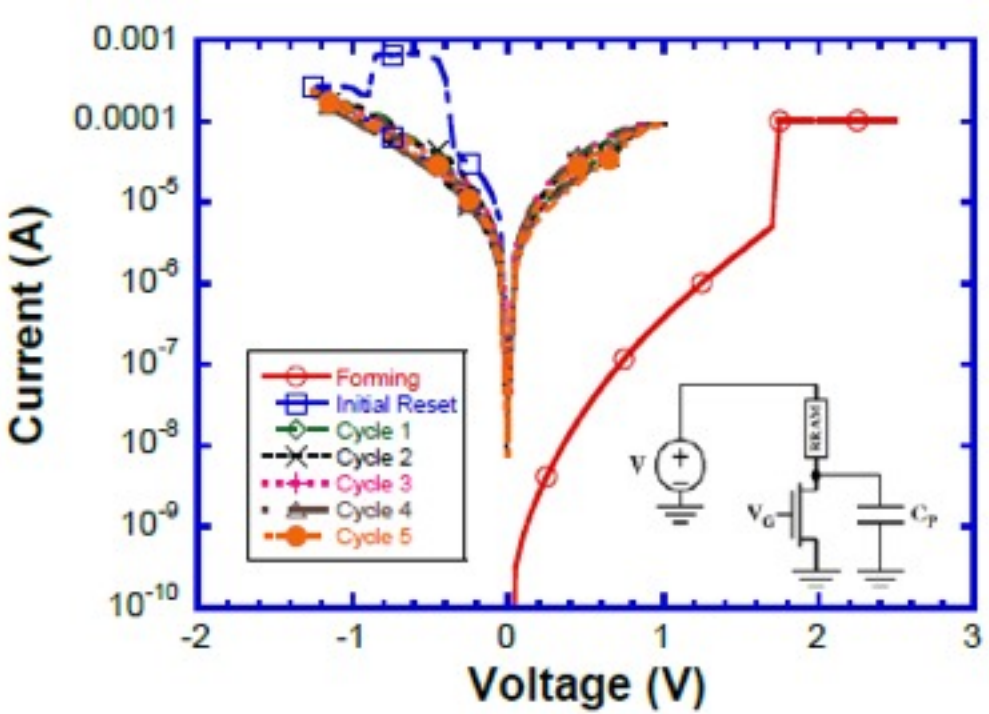
$$C = C_{TMO} + C_{filGap}$$

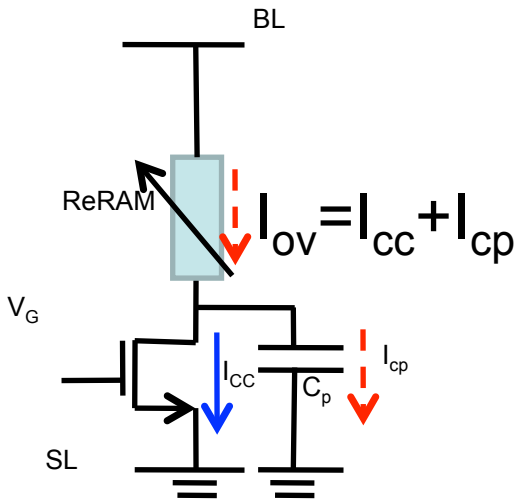
$$C_{filGap} = \frac{\varepsilon A_{filament}}{t_{Gap}}$$

Challenges for ReRAM Devices

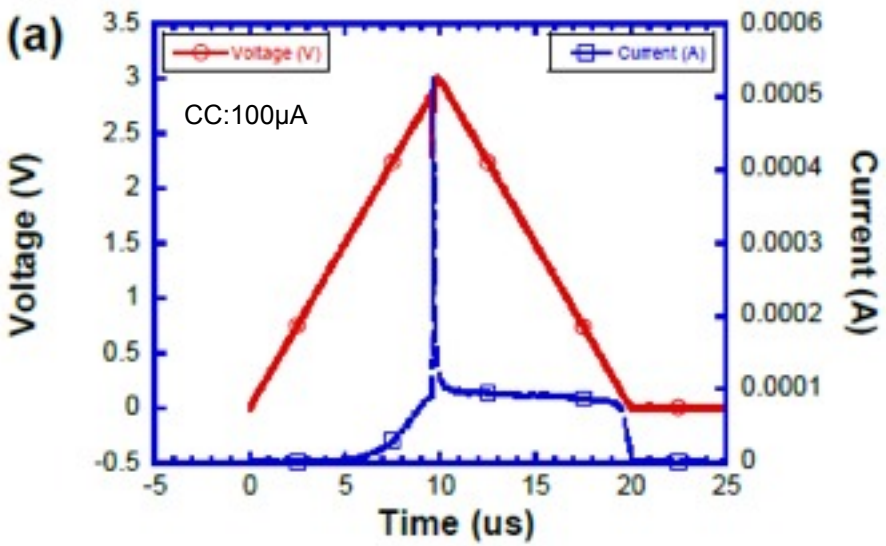
- Necessity for Electroforming
- Parasitic Capacitance (C_p) and Current Overshoot
- High Reset Currents
- Variability
- Need for a bidirectional selector diode

Electroforming,Cp,Current Overshoot



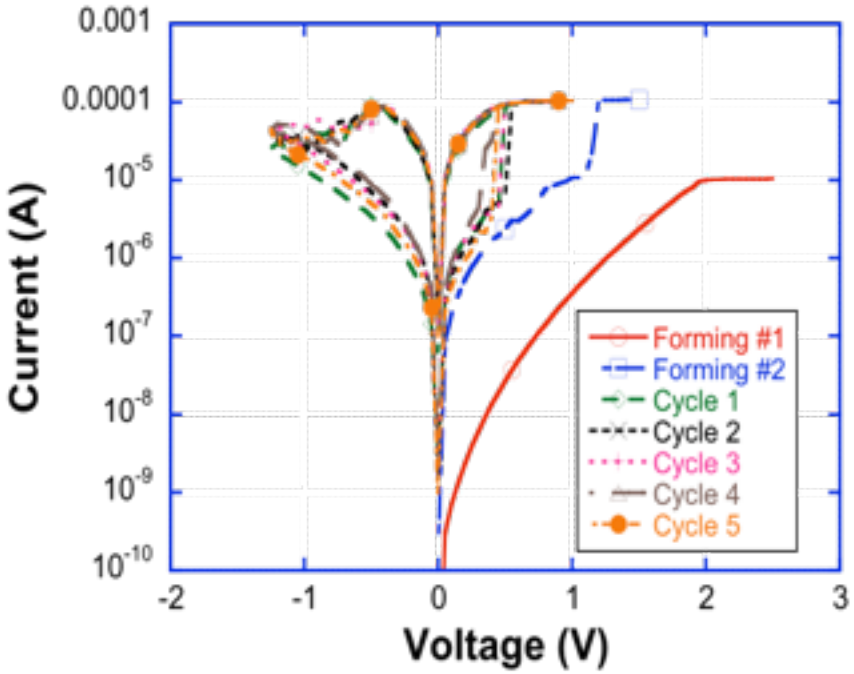


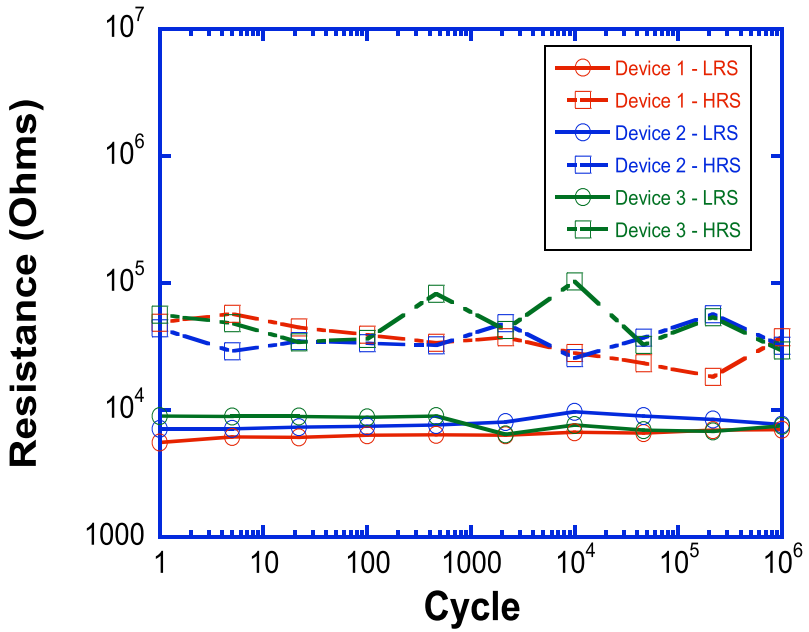
C_p and Overshoot Current



Overshoot in current over the compliance current due to C_p can lead to uncontrolled filament dimensions which can be a primary cause of variability.

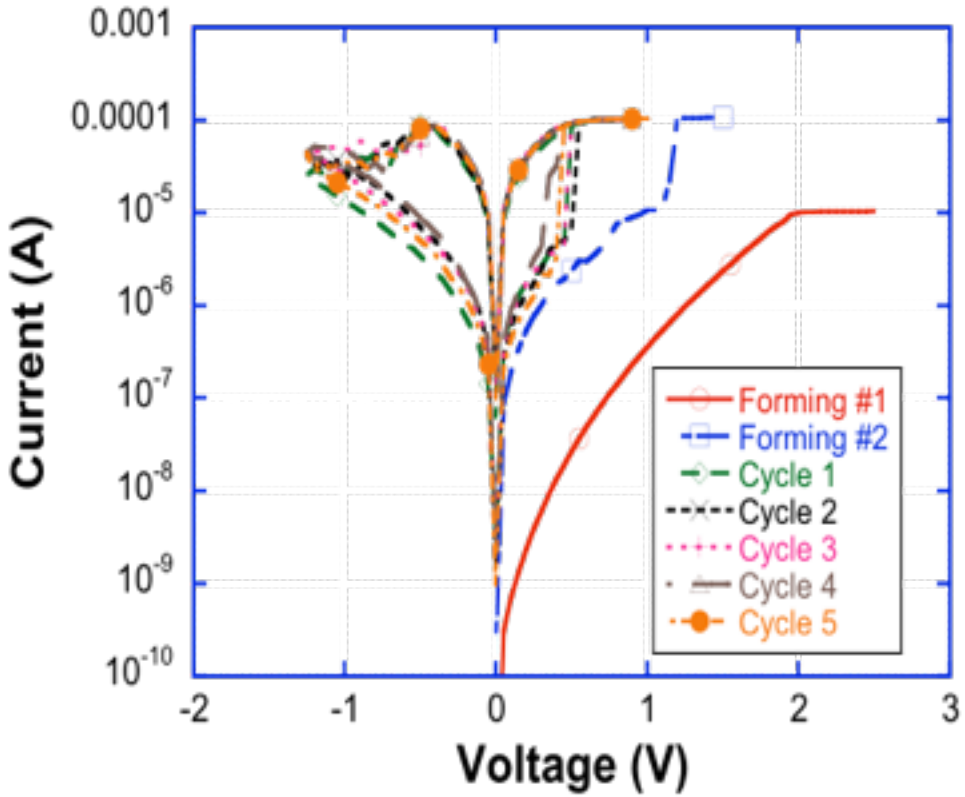
Novel Dual-Step Forming Process





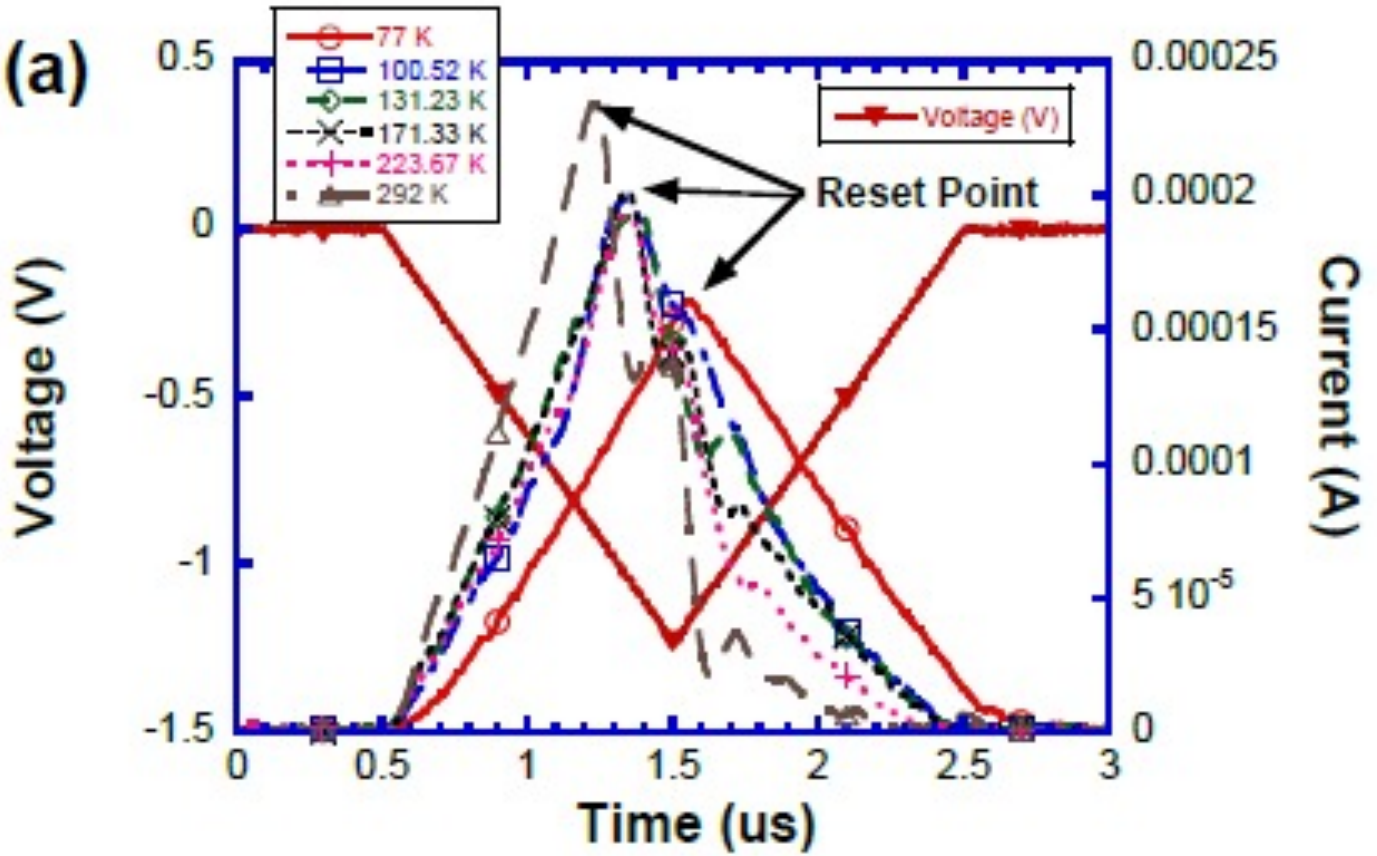
A careful forming can mitigate this issue. However forming-free switching will be an ideal choice.
Graduate student Branden Long has a poster in Flash Memory Summit on forming-free options.

Reset Mechanism in ReRAM



RESET voltage, current, and time is a function of temperature.

Reset Mechanism in ReRAM



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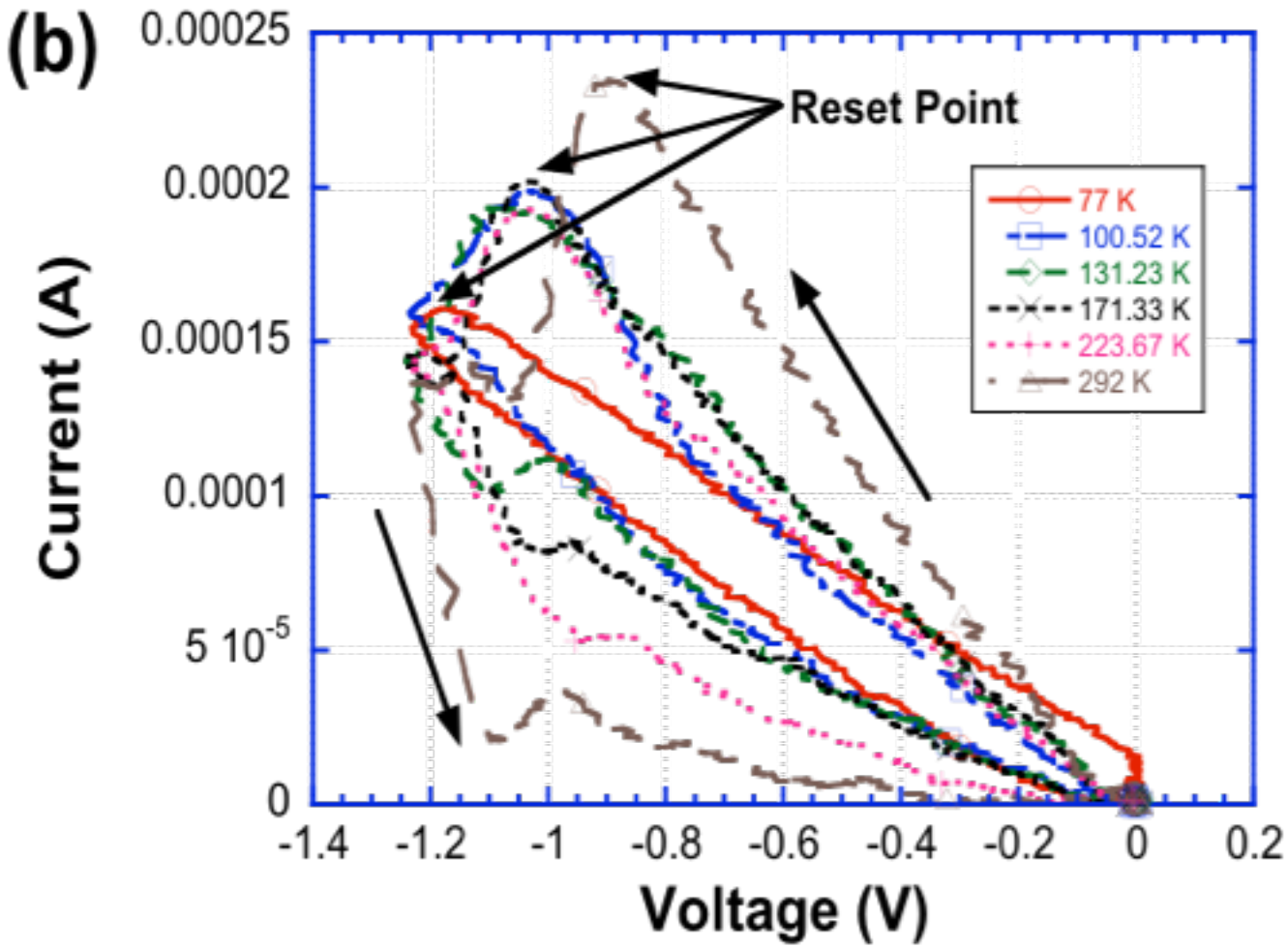
Temperature Dependent Reset Dynamics



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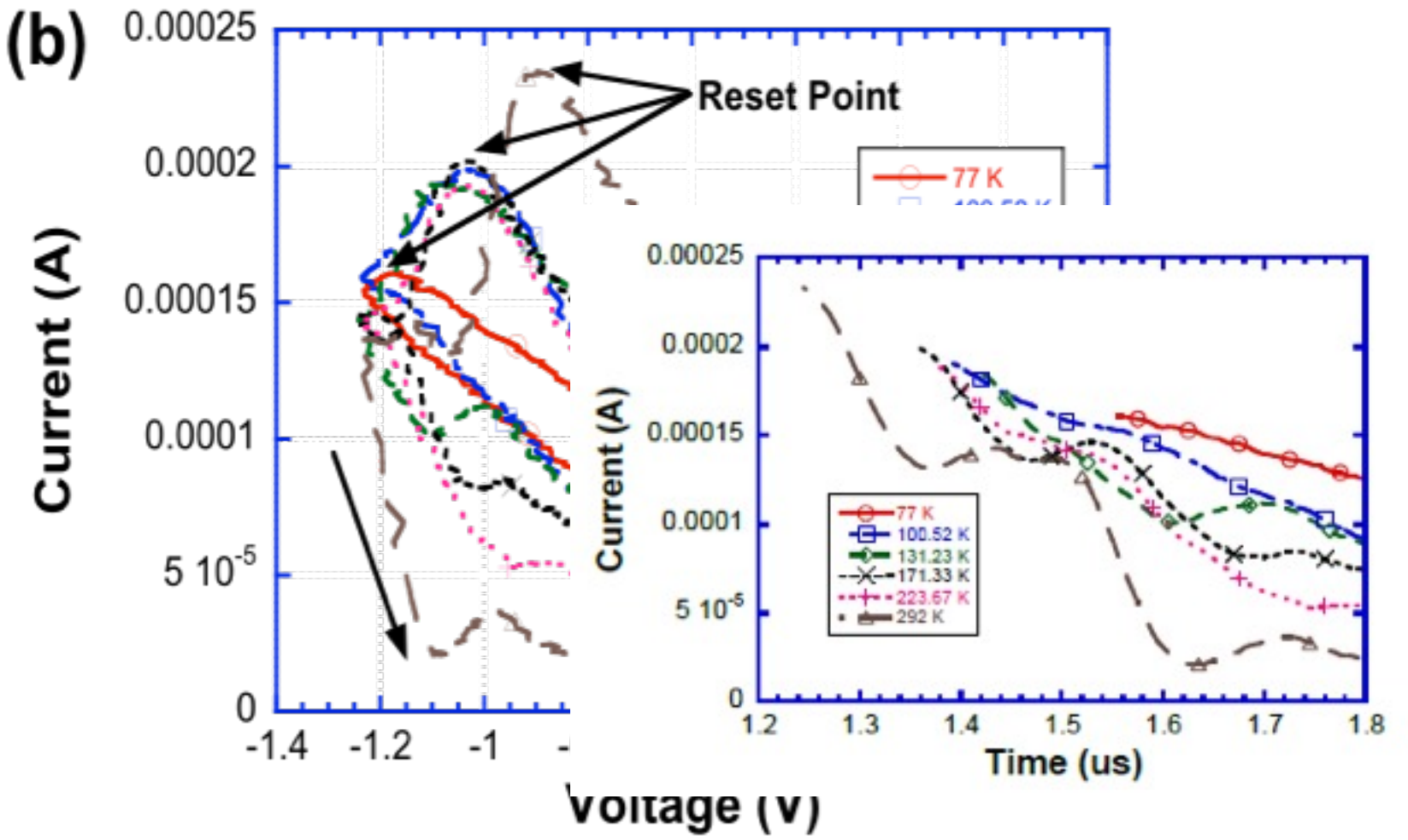
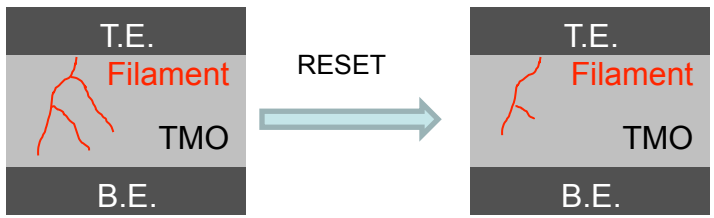
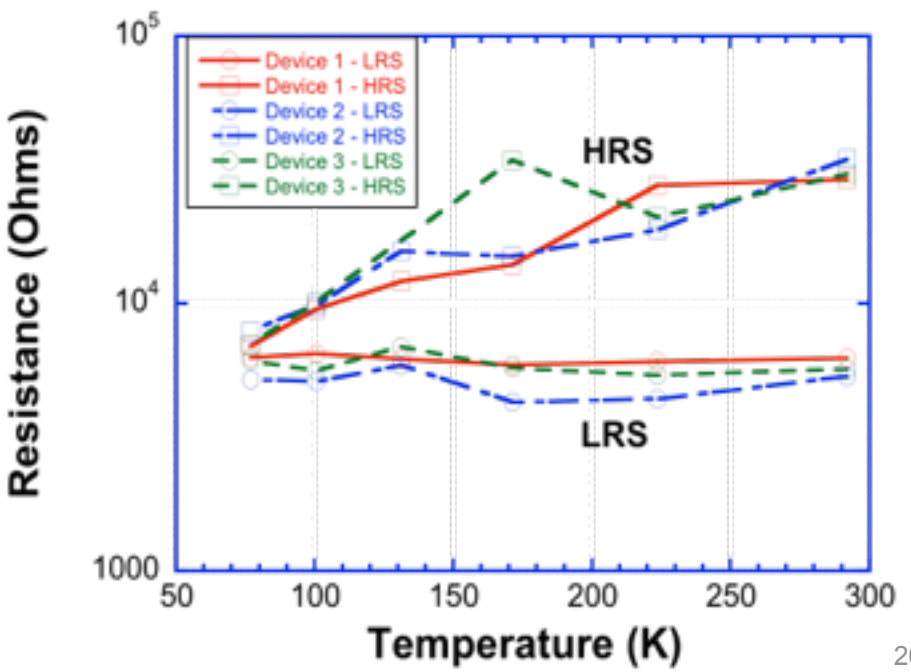


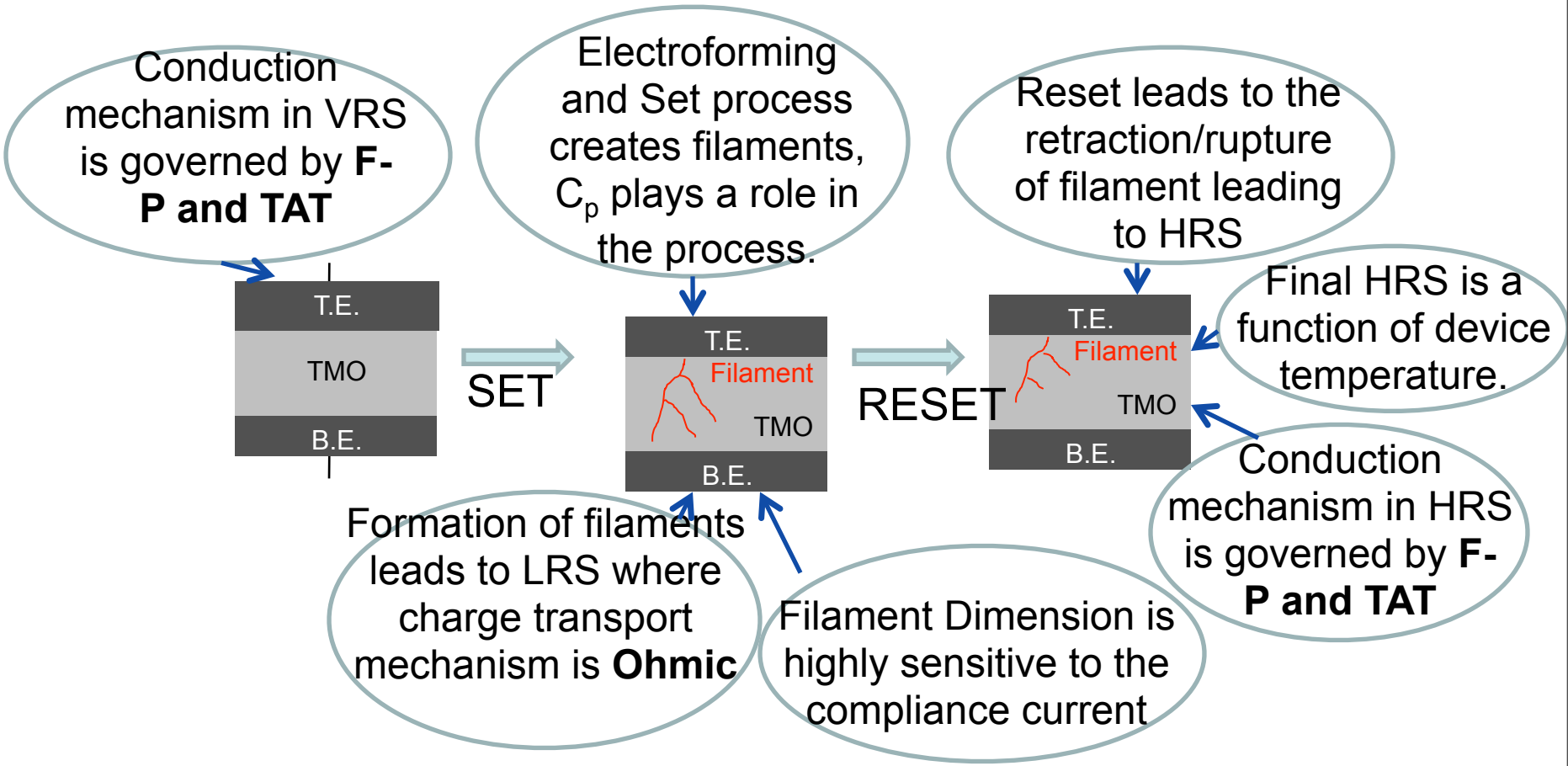
Final Reset vs. Temperature

- Mechanism of Reset is a multiple step process:
  - A critical power is needed to initiate the reset process
  - Continued reset results from subsequent re-oxidation of filament





Conclusions



Acknowledgements

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- Sematech Incorporation