Tackling Intracell Variability in TLC Flash Through Error Correction Coding

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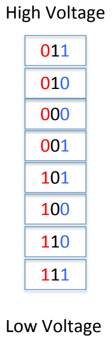
- Tensor product codes
  - P. Chaichanavong and P.H. Siegel, "A Tensor-Product Parity Code for Magnetic Recording," 2006.
  - J.K. Wolf, "On Codes Derivable from the Tensor Product of Check Matrices," 1965.

Voltage Levels for TLC

- Most Significant Bit MSB
- Center Significant Bit CSB
- Least Significant Bit LSB



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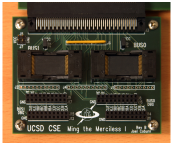

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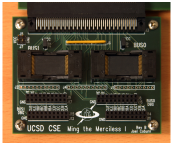

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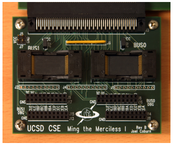

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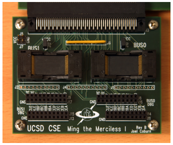

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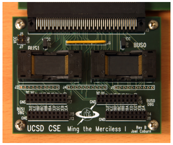

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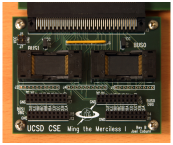

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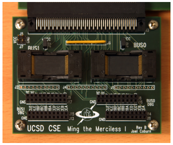
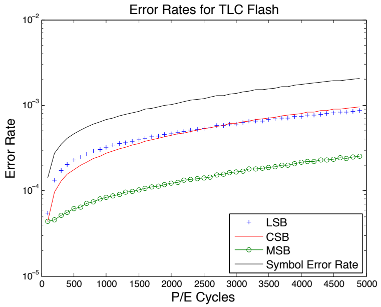
- On the other 99 cycles, the block was erased and all-zeros were written.



Raw Error Rate



Error Patterns Within a Symbol

Number of bits in symbol that err	Percentage of errors
1	0.9617
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$\boxed{\text{Idea: Design a code for observed intracell variability.}}$

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- A codeword is n binary length-m vectors so the result is a length-nm vector.
- Example over alphabet of size 8:
  $(45702) - > (100\ 101\ 111\ 000\ 010)$

Error Vectors

Definition (Bit-Error Vector)

The length-nm vector $\mathbf{e} = (\mathbf{e}_0, \mathbf{e}_1, \ldots, \mathbf{e}_{n-1})$, where each m-bit vector $\mathbf{e}_i$ represents a symbol of size 2^m, is a $[t; \ell]$-bit-error-vector if

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Definition (Graded Bit-Error Vector)

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Example of a $[5, 2; 1, 3]$-bit-error-vector:
(100 100 000 010 111 001 000 111 010).

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Goal is to construct a $[t_1, t_2; \ell_1, \ell_2]$-bit-error-correcting code and apply to Flash to mitigate the observed intracell variability.

Tensor Product Codes [1]

Theorem

- *Let* H_1 *be a parity check matrix for the* $[m, k_1, 2\ell + 1]_2$ *code* $\mathcal{C}^1$ *(standard* $[n, k, d]$ *notation).*

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- *Then,* $H_2 \otimes H_1$ *is a parity check matrix for a* $[t, \ell]$*-bit-error-correcting code.*

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- Suppose H_1 is an $r \times m$ parity check matrix of a $[m, k_1, \ell_2]_2$ code $\mathcal{C}_1$ where H_1 is $\begin{bmatrix} H_1' \\ H_1'' \end{bmatrix}$ such that the following holds:

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  2. $H_1^{''}$ is a r'' by m matrix for $r'' = r - r'$.

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Theorem (Construction 2)

Then H_B is the parity check matrix of a $[t_1, t_2; \ell_1, \ell_2]_{2^m}$-graded bit error correcting code, where

$$H_B = \begin{pmatrix} H_2 \otimes H_1' \\ H_3 \otimes H_1'' \end{pmatrix}.$$

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- Further simplifications are possible for special cases of the code parameters.

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  3. 'Scheme A' - Comprised of a non-binary $[256, 227, 5]_4$ code $\mathcal{C}^2$ applied to the LSB and the CSB for each Flash memory cell. An independent binary $[256, 240, 5]_2$ code $\mathcal{C}^3$ was applied to the MSB for each Flash memory cell. The overall rate is 0.904.

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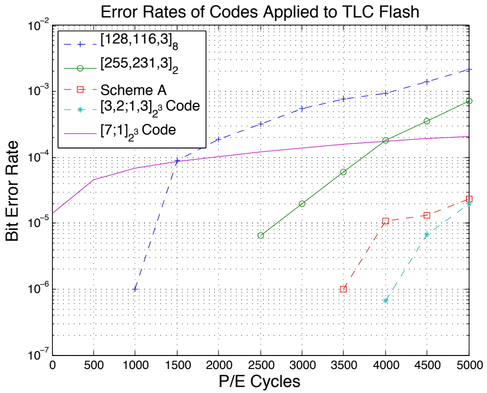
- Constituents of $\mathcal{C}$ are $\mathcal{C}^1$ as $[3, 0, 3]_2$ (with $\mathcal{C}'_1$ as repetition code), and $\mathcal{C}^2$ and $\mathcal{C}^3$ from Scheme A.

Results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Bit Error Rate
P/E Cycles
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Scheme A
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10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
0
500
1000
1500
2000
2500
3000
3500
4000
4500
5000

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- Codes based upon Tensor Product Codes offer an efficient alternative to binary and non-binary linear codes.