

# Abstracting the Flash Translation Layer for Enterprise-ready MLC

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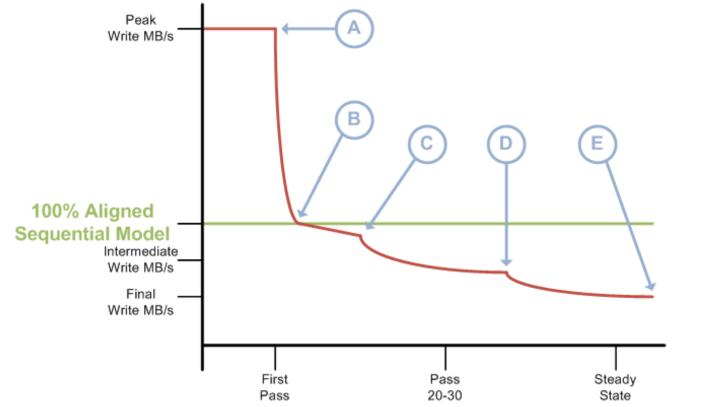
# Issues with SSDs in Arrays

- SSDs are not drop-in replacements for HDDs
- System optimizations for single SSD may not be portable to arrays
- Many complex issues (for 5 minutes)
  - Aligned Sequential Writing Trap
  - Wear Leveling Self-Destruct

### Consider FTL as a System / Device Abstraction



# Write Performance over the life of an SSD Device



Theory: Minimize write amplification and controller overhead by using aligned, sequential, fixed-blocksize writing

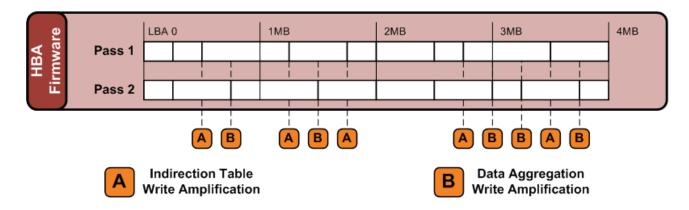


## 256KB Aligned Sequential Writes

#### Two passes over same LBA space

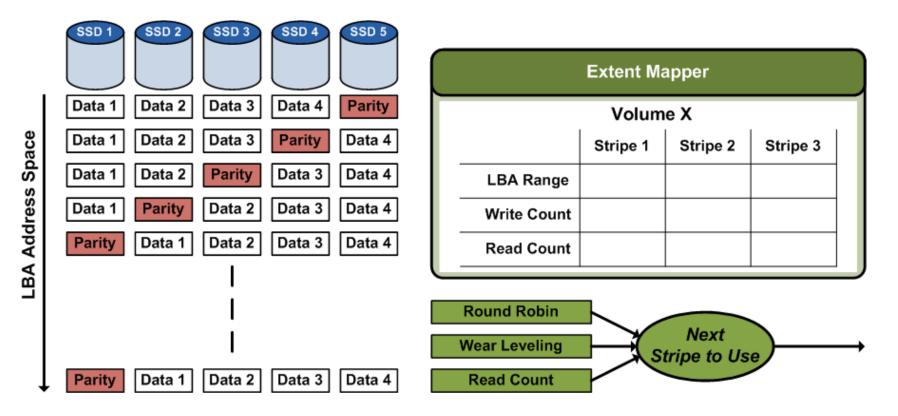


lel		LBA 0				1MB				2MB				3MB				4MB
Kerr	Pass 1																	
SO	Pass 2																	





#### Traditional Storage Array Volumes as Extents over Stripes



Theory: Global wear-leveling extends array life

#### Flash - Optimized Storage Array Memory Plan for wear and performance

	SSD 1 SSD 2 SSD 3 SSD 4 SSD 5	Extent Mapper									
LBA Address Space	Data 1 Data 2 Data 3 Data 4 Parity   Data 1 Data 2 Data 3 Data 4 Parity   Data 1 Data 2 Data 3 Data 4 Parity   I I I I I   Data 1 Data 2 Data 3 Data 4 Parity   I I I I I   I I <td< td=""><td>Volume X         Stripe 1       Stripe 2       Stripe 3         LBA Range            Write Range             Write Range              Write Range                Write Range</td><td></td></td<>	Volume X         Stripe 1       Stripe 2       Stripe 3         LBA Range            Write Range             Write Range              Write Range                Write Range									
	Data 1Data 2Data 3ParityData 4Data 1Data 2Data 3ParityData 4IIIIParityData 1Data 2Data 3Data 4ParityData 1Data 2Data 3Data 4	Rotation Countdown       Next         Stripe Activity       Next         Performance Model       Stripe and Range to Use         Wear Plan       Use         Read Count       Use									

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# Final Thoughts / Questions?

- Creating all-flash arrays is easy
- Maintaining performance and reliability over time requires new system architecture
- For performance and reliability, split FTL functions between array controllers and SSD devices
  - Block management and write buffering in SSDs
  - Global wear profiling in array controller
  - Lock down Kernel and HBA behavior