PCIe Testing for Quality and Reliability

Michael Bellon
Vice President of Engineering,
Flexstar Technology

Flash Memory SUMMIT

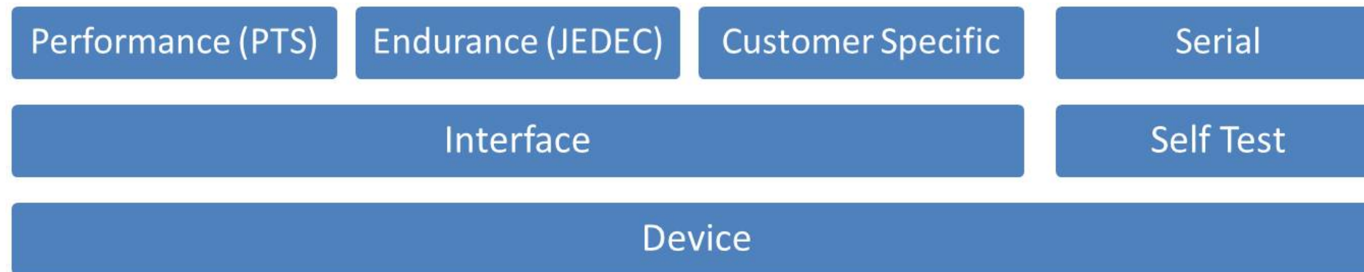
Why Test?

PCIe is just another form of SSD, after all

- ***Most of the tests apply since the requirements for performance and functionality remain the same***

- PCIe devices have different characteristics that separate them from standard SSDs:
  - the interface to the system motherboard is through a different technology
  - they tend to consume more power than SSDs
  - different airflow requirements

Software Environment



- Most software challenges are on the test system side
  - Current interface standards ATA / SCSI are employed
  - OS-aware hot-swap
  - Controller integration

- Industry standard tests are defined
  - JEDEC: JESD218A and JESD219 for reliability and endurance
  - SNIA: Solid State Storage Performance Test Specification

- Testing is tailored to the specific product lifecycle phase

JEDEC Certification

The JEDEC Solid State Technology Association sets requirements for Client and Enterprise application classes based on endurance ratings.

The following are the conditions that need to be satisfied:

- SSDs maintain capacity
- SSDs maintain the required Uncorrectable Bit Error Rate (UBER)
- SSDs meet the required Functional Failure Requirement (FFR)
- SSDs maintain data due to loss of power for time requirements for its respective application class

Table C.1 — Expected retention (weeks) at different use temperatures

Client

Power Off Temperature	Active Temperature 25	30	35	40	45	50	55
55							8
50						9	15
45					10	17	27
40				14	20	31	52
35			20	26	38	61	101
30		32	39	52	76	120	199
25	58	65	79	105	155	244	404

Enterprise

Power Off Temperature	Active Temperature 25	30	35	40	45	50	55
55							2
50						2	4
45					2	4	7
40				3	4	7	13
35			3	5	8	14	25
30		4	6	10	16	28	50
25	7	9	12	20	33	58	101

SNIA Certification

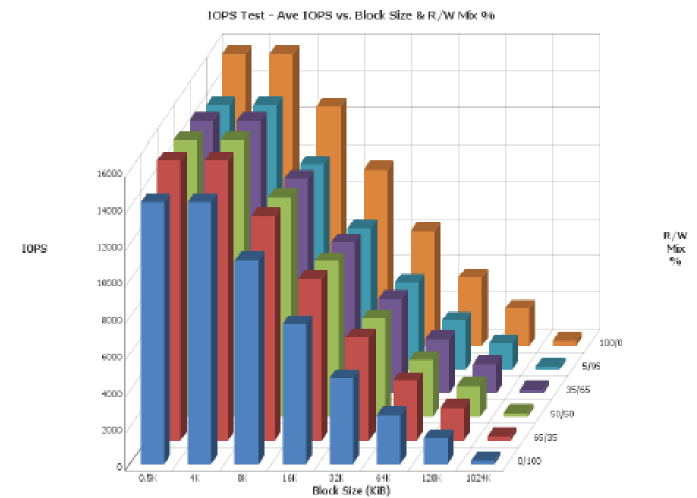
The Storage Networking Industry Association (SNIA) test process is highly dependent on:

- its prior usage
- the pretest state of the device
- the testing parameters

The SNIA testing procedure includes the following:

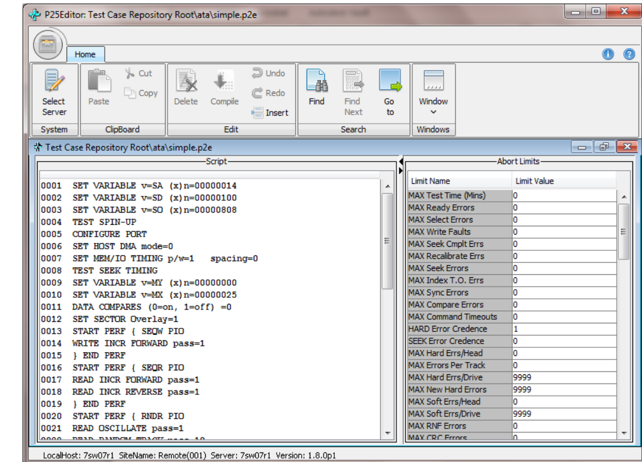
- IOPs Test
- Throughput Test
- Latency Test

PTS-C	IOPS Table - R/W Mix x BS						
ST9640322AS							
Test Run Date:	07/25/2012 11:38:46			Report Run Date:	08/20/2012 14:59:49		
IOPS Test - Ave IOPS vs. Block Size & R/W Mix %							
SNIA SSS TWG: SolidState Storage Performance Test Specification (PTS)						Rev.	0.0.1
						Page.	4 of 16
Device Under Test (DUT)		VENDOR: Company	DUT Model NO: ST9640322AS		SPONSOR: DeskTop	Flexstar	
Serial No.	[illegible]	DUT Preparation		Test Loop Parameters		Steady State	
Firmware Rev	[illegible]	Purge	UNKNOWN	REQUIRED:		Convergence	Yes
Capacity	640 GB	Pre-Conditioning		Data Pattern	Random	Rounds	1 - 5
NAND Type	Nand	Workload Independent	UNKNOWN	Tester's Choice:		PC AR	100%
Device I/F	SATA 1.5 Gb/Sec			OIO/Thread (QD)	UNKNOWN	AR AMOUNT	16 GiB
Test Platform	Peg2	Workload Dep.	UNKNOWN	Thread Count (TC)	3	AR Segments	2048



Functional / User Defined

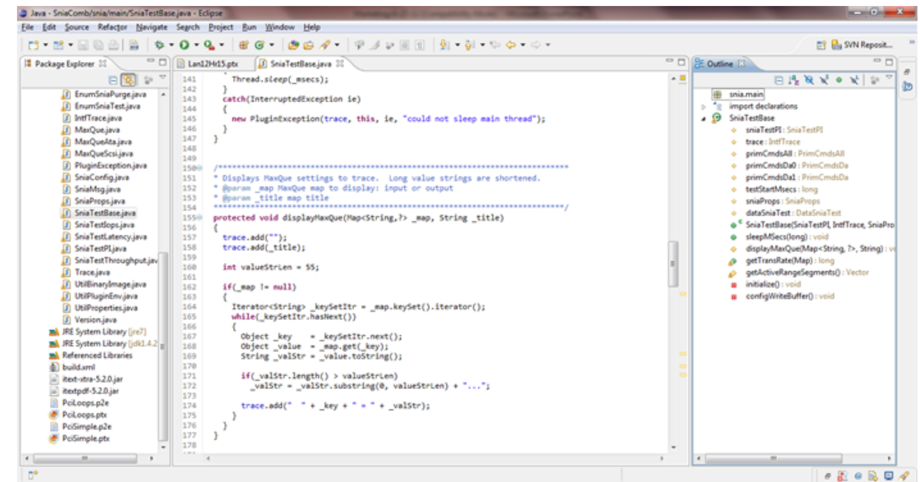
- What can be done with Interface testing
  - Ensure compliance to interfaces
  - Monitor failure modes
    - Power margining
    - Power cycling
  - FTL functionality to LBA write to LBA read
    - Correctness of garbage collection, wear leveling
    - Tailored to expected use case



- What cannot be done with Interface testing
  - Algorithm efficiency
  - No access to Meta data (SMART typical though)

- What can be done through self test
  - Handled by the FTL
  - Algorithm correctness

- Current limitation due to emulation of SCSI / ATA interface



The Challenges of PCIe Testing

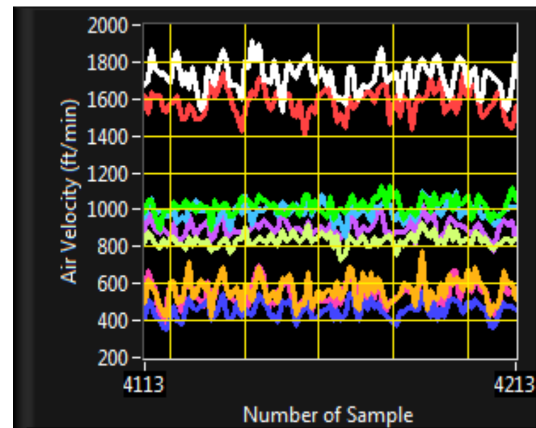
- Challenges exist in the areas of mechanical, electrical and software
- Typical SSD constraints still apply:
  - Environmental and Burn-in test systems are employed to accelerate device wear
  - Isolation of the support electronics is required
  - Independent device removal without interrupting other DUT
- Maintaining a set airflow around a PCIe device in the test environment is difficult due to turbulence caused by differing form factors
- Electrically challenging due to ultra long traces for signal integrity

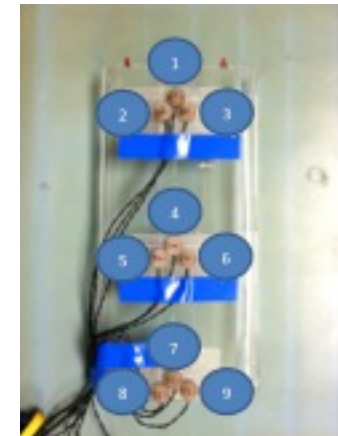
Airflow Across PCIe Devices

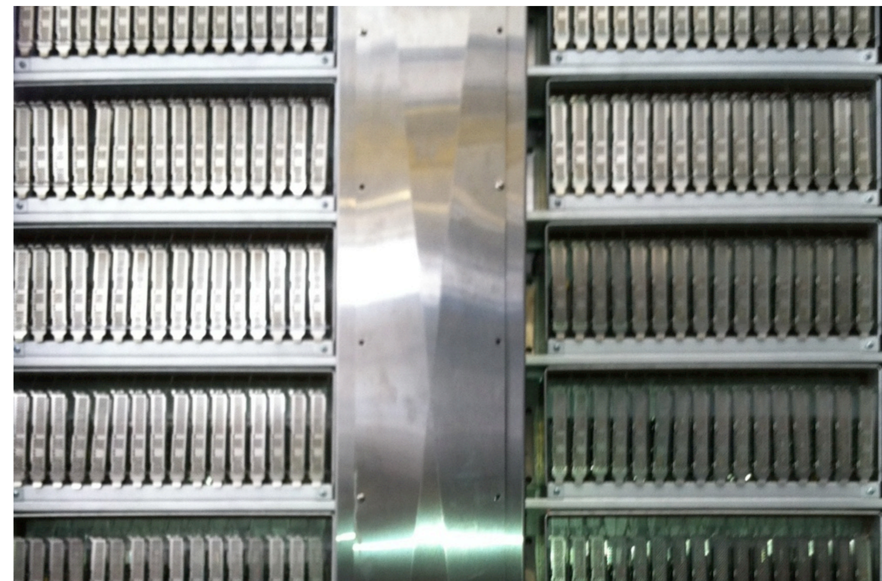
- Demonstrated airflow is across a single DUT
  – Air column from the back
  – Return airflow from the front
  – Two redirection points

- Large variance across the DUT length:
  – 400 LFM at trailing edge
  – 1800 LFM at leading edge

- Takeaway
  – Plan for airflow optimization with respect to device geometry







Future Predictions

- PCIe 3.0 will push electrical integrity harder
- Software should become easier as standards are set for communication and interface
  - NVMe / SOP adoption
- Mechanical challenges will continue until a 2.5” or 3.5” form factor is universally accepted
- The need for devices to be easily hot swappable will continue
- Increased LFM to eliminate cumulative heat

Feedback

- Questions
- Feedback
- Discussion