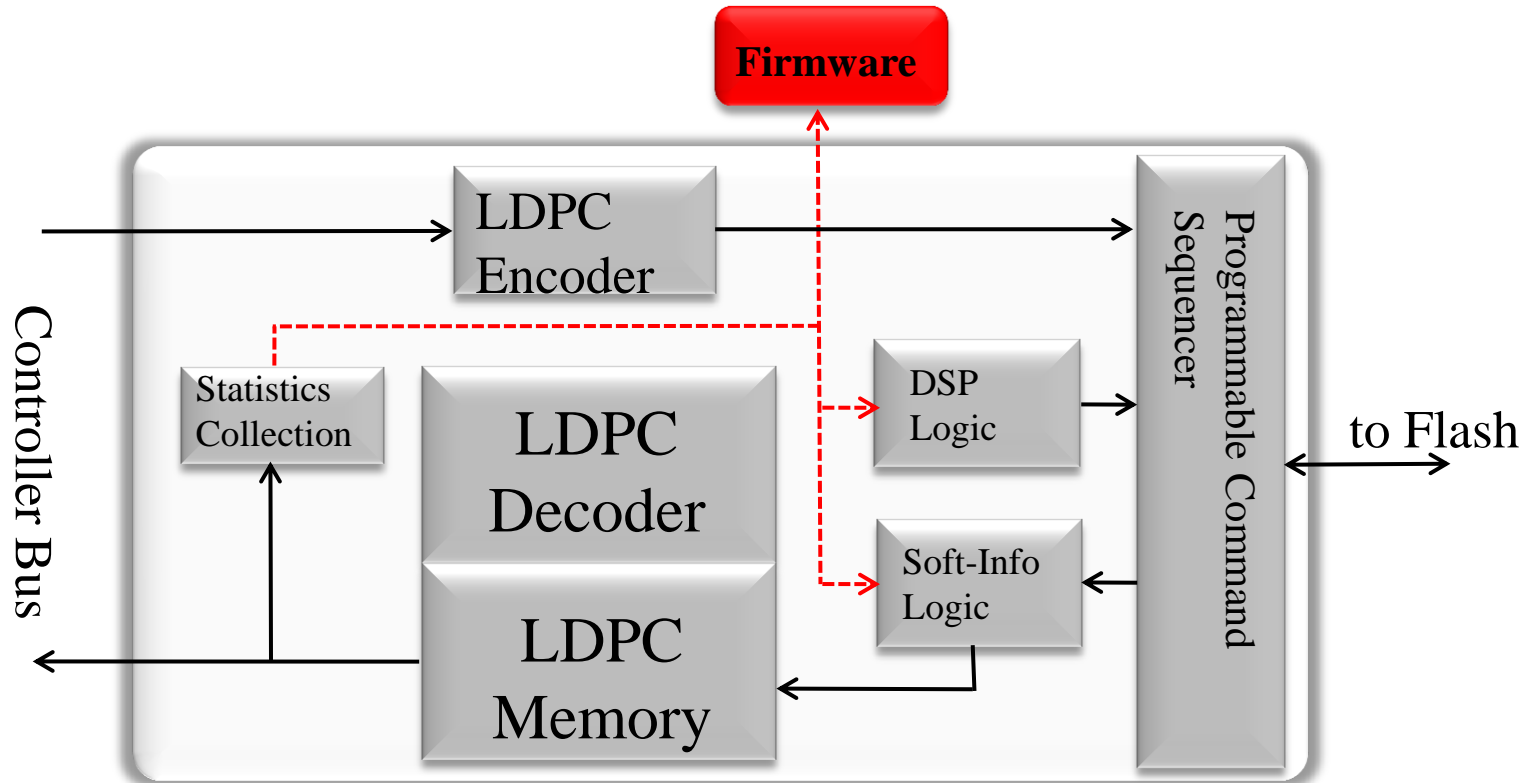


LDPC Compiler For NAND Flash and SSD Controllers

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Proton Read Channel

- LDPC-Based Read Channel provides significant (10x-20x) improvement in NAND Flash longevity.



LDPC Compiler

- LDPC Compiler supporting a wide range of data-rates
 - 50MB/s to 3.5GB/s for a single LDPC instance (in 40nm process)
- List of parameters selected prior to instantiation:
 - Codeword size (Macro-level: 1KB vs. 0.5KB vs. 2KB, etc.)
 - Several parameters for degree of parallelism and memory access options
- After compilation, each instance is supporting:
 - Simultaneous support for different amounts of parity/code rate
 - Simultaneous support for several LDPC codes
 - On-the-fly switching from one LDPC code to another
 - Each matrix can be an arbitrary LDPC matrix subject to certain constraints

LDPC Decoder Core Examples

- Codeword size is 1KB
- Total power is measured for TT, 0.9V, 25C
- TSMC 40G process

Decoder Throughput	Clock Frequency	LDPC Compiler Options	Gate Count (KG)	Memory Size	Total Power (Gates+Memory+leakage)	
					Beginning-of-Life	End-of-Life
800 MB/s	450 MHZ	Option set 4 CW=1KB	158.6	17.9KB	46mW	138mW
111 MB/s	250 MHZ	Option set 2 CW=1KB	36.6	17.9KB	5mW	14mW

More LDPC Examples

- LDPC Decoder cores (compiler output) examples for ASIC implementation under various conditions.

LDPC Compiler Options	Technology Library TSMC 40nm G HVT ONLY	Frequency (MHz)	Throughput (MByte/s)	Gate Count (KG)	Memory (KByte)
	Track				
Option set 1, CW=1KB	9T	250	111	36.6*	17.9
Option set 2, CW=1KB	9T	400	222	46.2*	17.9
Option set 3, CW=1KB	9T	600	534	70.4*	20.5
Option set 4, CW=1KB	9T	500	895	158.6*	17.9
Option set 5, CW=1KB	9T	500	1780	301.4*	20.5
Option set 5 ,CW=1KB	12T	1000	3560	391.8*	20.5

* Gate count is measured based on two input NAND gate

Design Implementation

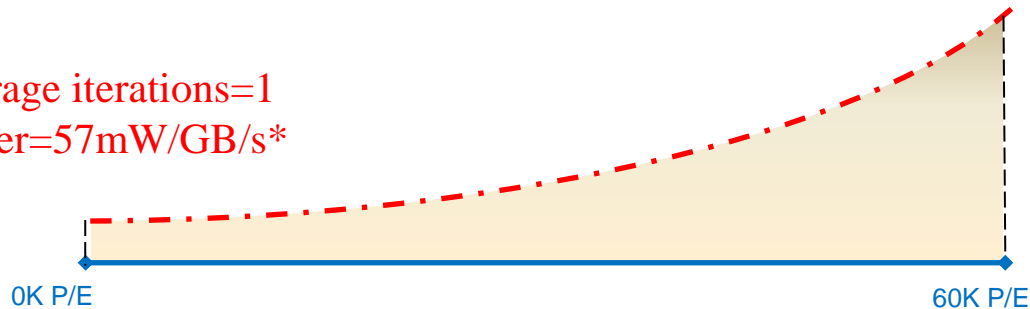
- ASIC, eASIC and FPGA implementation and integration are supported
- ASIC implementation
 - Cadence Design Flow
 - TSMC libraries
 - Trial place and route at IP/Block level
- eASIC implementation
 - LDPC Compiler is run with a custom option set for eASIC
 - Full integration with eASIC design flow, design implemented with clock frequency up to 500MHz.
- FPGA implementation
 - LDPC Compiler is run with a custom option set for FPGA

Sufficient Iterations for End-of-Life

- LDPC Decoder computational load and power consumption increase towards the End-of-Life of SSD:

Average iterations=3.5
Power=172mW/GB/s*

Average iterations=1
Power=57mW/GB/s*



- LDPC Compiler guarantees sufficient iterations for End-of-Life
 - Guaranteed sustained 3.5 LDPC iterations for quoted data-rates
 - Maximum iteration limit is programmable and is typically much higher (e.g. 8-128)

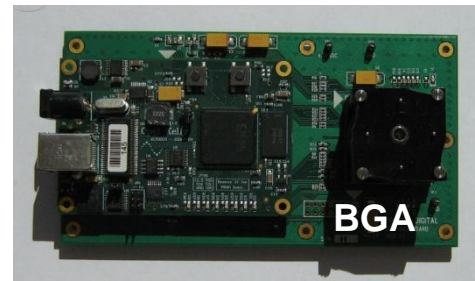
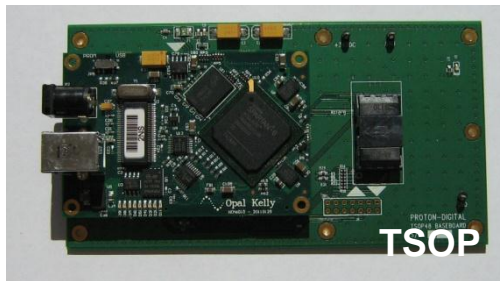
LDPC For Conventional Read

- Full-power LDPC decoder is used for conventional read ("hard-decision decoding")
- This reduces the occurrence rate of soft-information read
- Example of LDPC Correction Capability:

Method	User Bytes	Parity Bytes	Average bit errors corrected
BCH, T=70	1KB	123	70
LDPC Hard-Input Decoding	1KB	123	73
LDPC Soft-Input Decoding	1KB	123	>186 (=ER @ optimal Vth) >490 (=ER @ nominal Vth)

From LDPC to Flash Read Channel

- Significant testing and system optimization required for full Flash Read Channel Solution – LDPC is only a component
- Read Channel testing on various Flash Geometries: 2X/2Ynm, 1Xnm
 - “Special Commands” from different Flash manufacturers



- Testing on full manufacturing yield distribution
 - Flash samples from production line
 - “Bad Samples” from production line

