

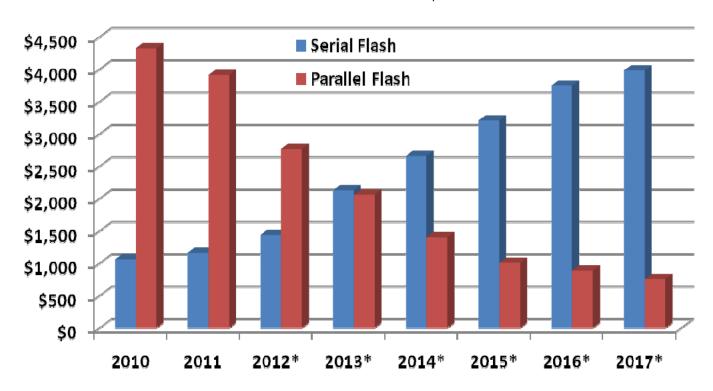
Serial NOR Flash Applications Drive Growth

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NOR Flash Market by Revenue

Revenue in Millions of \$†



NOR Flash market is migrating from Parallel to Serial

- Serial revenue will grow from \$1B in 2010 to ~\$4B in 2017, while Parallel declines
- Revenue crossover in 2013, Units crossover in 2009 (2011 6B units ~2/3 Serial)
- Serial Flash replacing Parallel due to cost, space & pin-count advantages



Why SPI?





	Parallel NOR Flash	Serial NOR Flash	SPI Advantage	
Interface Pins	28 to 44	4 to 6	Lower system cost	
Packaging	48-56 pin TSOP 48-64 ball BGA	8-pin SOP, WSON, USON, WLBGA	Smaller, Lower cost	
Performance	8/16/32-bit bus, Best Random Access	Quad SPI Speed Comparable to PF for Fast Boot & XIP	Comparable performance with fewer pins	
Architecture	128KB Sector erase	4KB Sector erase	PC Requirement, Efficient memory usage	
Density	4Mb to 2Gb	512Kb to 2Gb	Serial Flash has caught up	
Technology	110nm, 90nm 75nm, 65nm, 45nm	110nm,90nm, 75nm, 65nm, 58nm	Advanced technologies for Serial Flash = Smaller Packages	



Flash Memory Applications

PC-Related

Desktop, Notebook, Server Optical Disk Drives Hard Disk Drives LCD Monitors Printers







Communications

DSL and Cable Modems
Router & Switches
Wireless LAN, M2M
Bluetooth, GPS, Mobile
Phones

















Consumer

LCD & Digital TV, Tablets
DVD Player & Recorders
Set Top Box, Cordless Phone
Electronic Toys/Games
Digital Cameras, Appliances







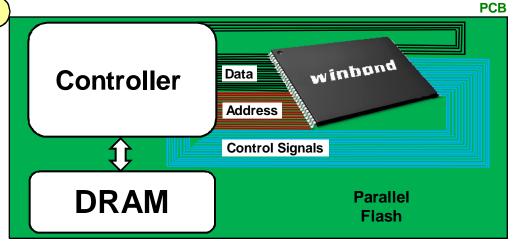


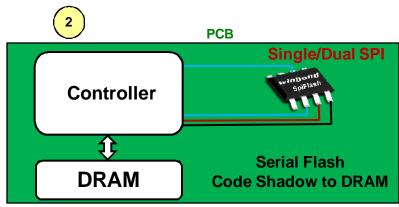
Automotive/Industrial

Infotainment, Driver Assist Instrument Cluster, Camera, Telematics, Digital Radio, Smart Meters, Smart Grid

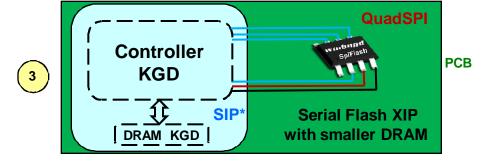


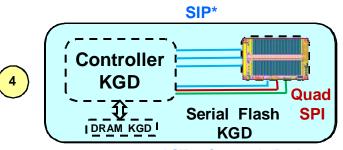
Application Trends for Serial Flash





PCB = Printed Circuit Board





* SIP = System In Package

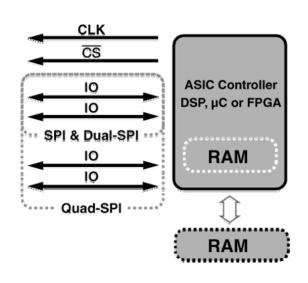
Optical Disk Drive (ODD) Serial Flash Evolution Example:

- Early designs used Controller + Parallel Flash + DRAM on a PCB
- To reduce cost and space, designs moved to Serial and eventually to System In Package (SIP) 2-Chip or 3-Chip solutions with Known Good Die (KGD)
- This trend is very similar for other applications like Mobile Phones



Quad SPI & QPI Performance

SPI Protocol		Number of Clocks			Command Overhead
Туре	Fast Read Instruction	Instr.	Add.	Dummy	# Clocks
SPI	Single I/O	8	24	8	40
Dual SPI	Dual Output	8	24	8	40
	Dual I/O	8	16		24
Quad SPI	Quad Output	8	24	8	40
	Quad I/O	8	8	4	20
	Quad I/O Continuous Read	8	4		12
QPI	QPI Read	2	6	2	10–16*



- Number of clock cycles reducing, and performance increasing
 - QuadSPI and QPI (Quad Peripheral Interface) offer XIP (eXecute In Place) = Direct code execution – No need for DRAM or buffer memory

^{*} QPI allows programmable dummy clocks to adjust to performance required



Space Efficient Packaging











BGA24 8x6mm (TB)=5x5



WSON8 8x6mm* (ZE)



WSON8 6x5mm* (ZP)



USON8 2x3mm* (UX)





WLBGA8 1.4x2.4mm* 8Mb (BY) **:**

WLBGA8 1.8x2.7mm* 16Mb (BY)



TSSOP8 173mil (SD)



SOP8 150mil (SN)



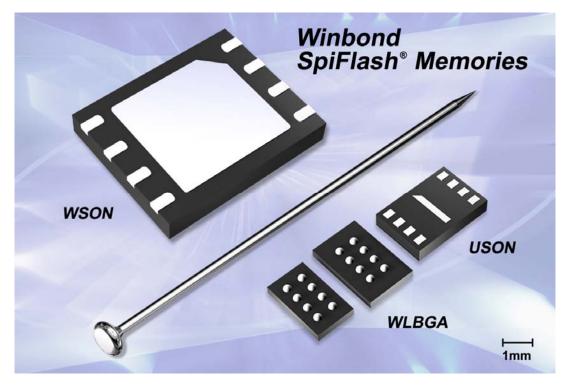
SOP8 208mil (SS)



SOP16 300mil (SF)



Ultra-Small Form Factor Packages

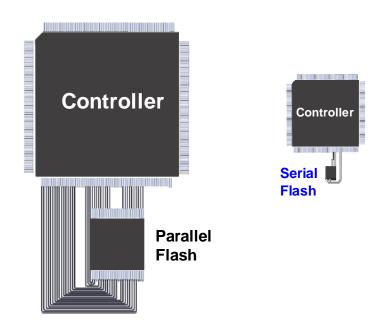


- New USON & WLBGA (CSP) packages
 - <20% the size of popular Serial Flash packages like 8-pin SOIC and WSON
- Ideal for space constrained applications including
 - Mobile Phones, Tablets, GPS, M2M, WLAN, HDD, Bluetooth, MP3 & more



Summary

- Serial Flash has become a popular alternative to Parallel Flash as well as the solution of choice for emerging applications due to:
 - Pin-count
 - Space Efficiency
 - System cost
 - Chip cost
 - Performance



Thank You