Design Considerations for UFS & *e*MMC Controllers

Andrew Haines

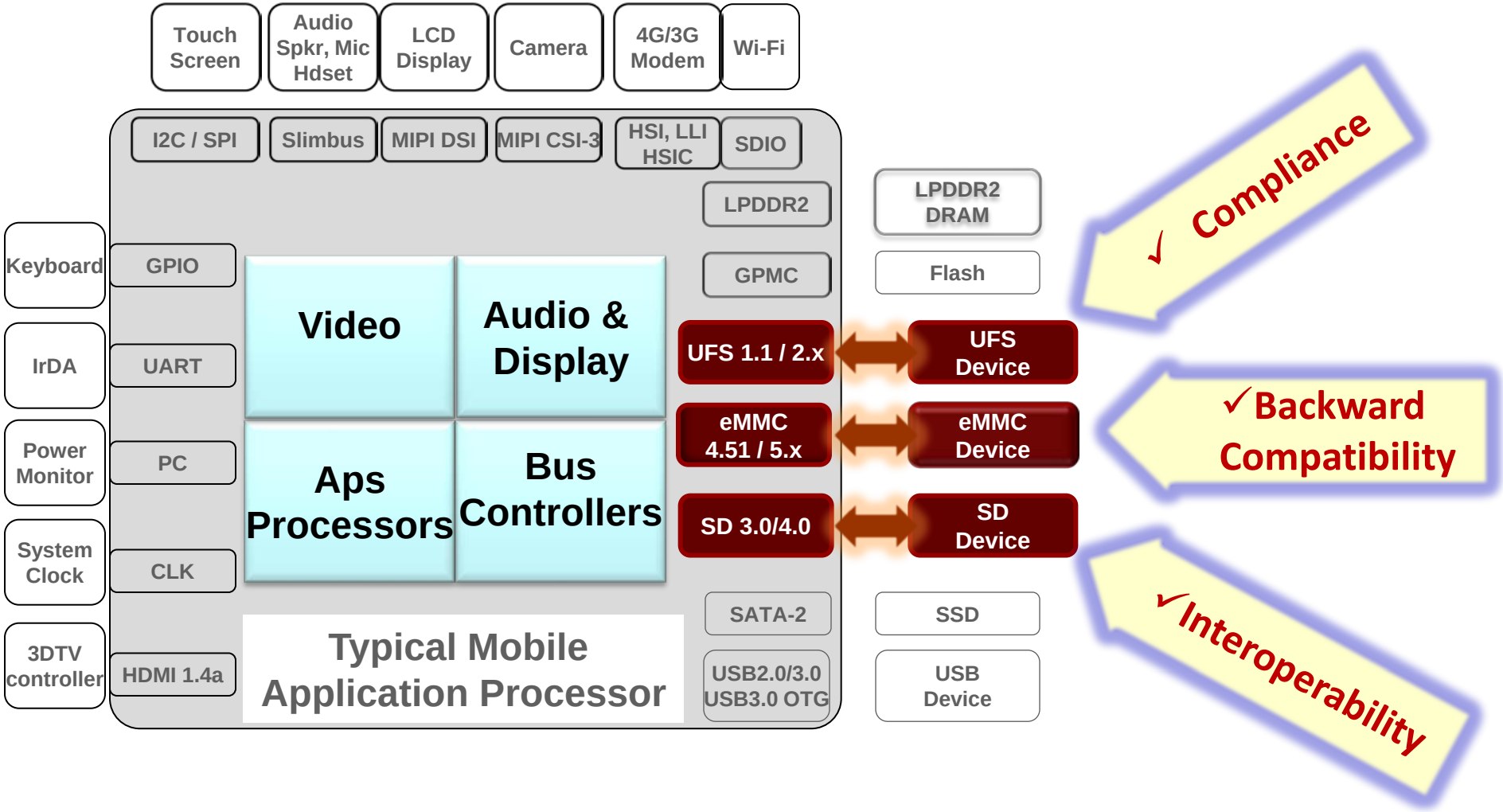
VP Marketing

Arasan Chip Systems, Inc.

Agenda

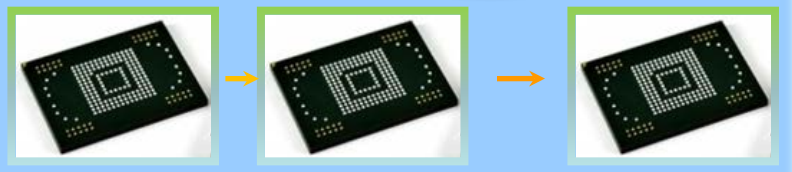
- Mobile Storage in SoC
- Challenges in Mobile Storage Controller Designs
- Enabling Mobile Storage Design Ecosystem
- Summary

Multiple Mobile Storage Interfaces in Application Processor

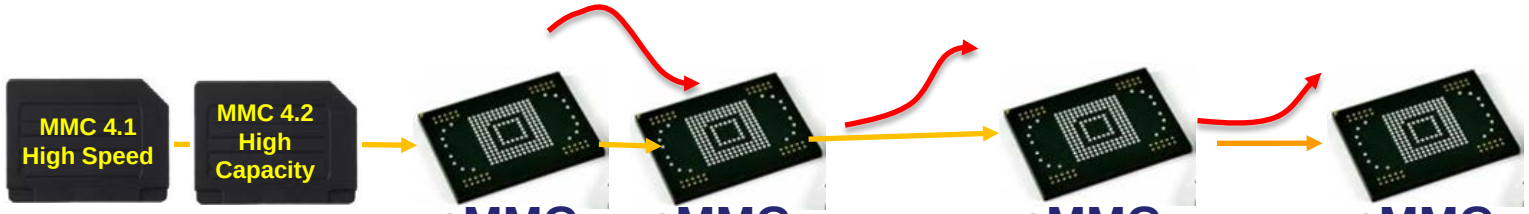


Mobile Storage Evolution Faster Than Ever

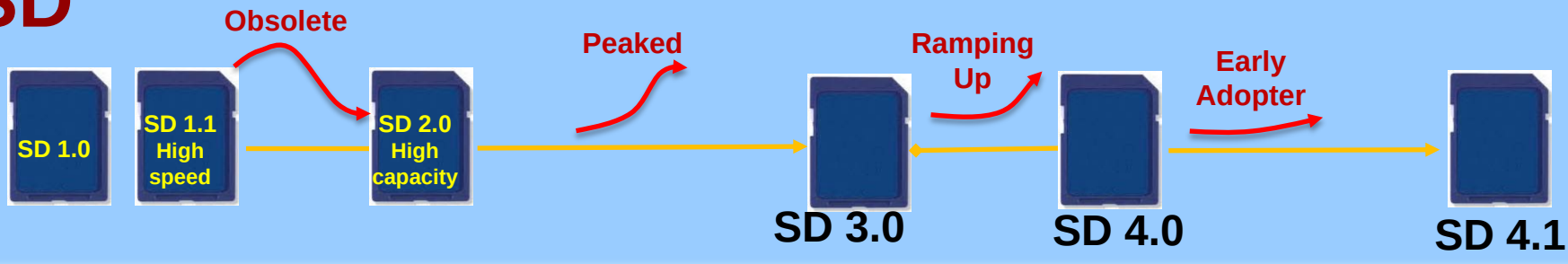
UFS



eMMC



SD



2003 2006 2009 2011 2012 2013

Challenges of Backward Compatibility eMMC

	eMMC 4.41	eMMC 4.51	eMMC 5.0
Max Throughput	High Speed 832 Mbps	HS200 1.6 Gbps	HS400 3.2 Gbps
Data Lines	4 or 8-bit		8-bit
Signal Count	10 Pins		11 Pins (Data Strobe)
IO Voltages	1.2 V / 1.8 V 3 V		1.2 V / 1.8 V
Interface	DDR-52	HS200	HS400
Data Strobe	No		Yes
Tuning (Read)	No	Yes	
Clock (MHz)	0 – 52 MHz	0 – 200 MHz	

eMMC Compliance

- eMMC Device spec published by JEDEC
- Compliance can be done through 3rd party Compliance Testers
  - No formal compliance guidelines

Challenges of Backward Compatibility UFS

		UFS 1.0	UFS 1.1	UFS 2.0
Transaction Layer	Host Interface	HCI 1.0	HCI 1.1	HCI 2.0
Link Layer	UniPro™	v1.40	v1.41	v1.60
	# of Lanes	Single Lane	Single Lane	2-Lane
Physical Layer	M-PHY	v1.0	v2.0	v3.0
	Data Rate	1.5 Gbps	2.9 Gbps	5.8 Gbps
	# of Lanes	1		2
	Interface	Tx +/-, Rx +/-		
	Diff $V_{peak-peak}$	500 mV Max (non-terminated) 250 mV Max (terminated)		

Source: JEDEC

UFS 1.1 Compliance

	Protocol	Rev.	Test Spec	Certification
Transaction Layer	UFS	1.1	UFS Test Spec v1.0	UFSA
Link Layer	UniPro	1.41	UniPro CTS_v1.0_r01	MIPI / UNH-iOL
PHY Layer	M-PHY	2.0	M-PHY CTS_v0.99	

Design Challenges

Can I have all these validated before starting my SoC design?

2. Backward Compatibility

eMMC 4.3 ➔ 4.4 ➔ 4.5 ➔ 4.51 ➔ 5.x

UFS 1.0 ➔ 1.1 ➔ 2.x

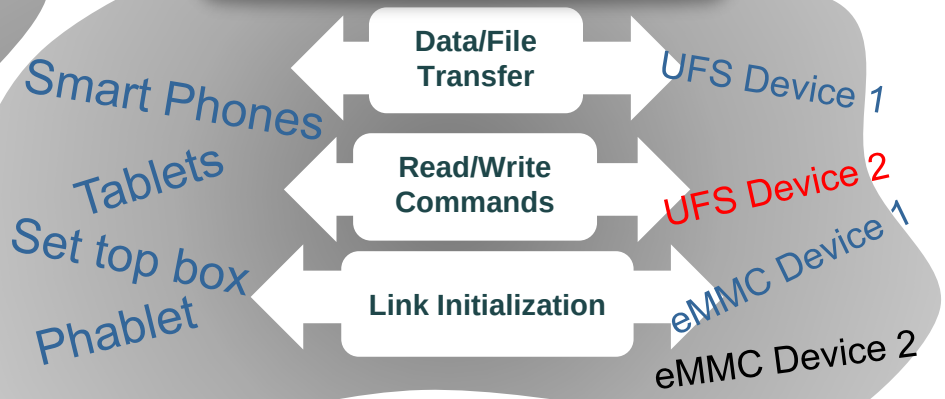
UniPro 1.40 ➔ 1.41 ➔ 1.6x

M-PHY 1.0 ➔ 2.0 ➔ 3.x

SD 2.0 ➔ 3.0 ➔ 4.0 ➔ 4.x

UHS-II ➔ UHS-?

3. Inter-Operability



JEDEC

eMMC

UFS

UFSA

SDA

SD

SDIO

Physical Layer

Link Layer

Application Layer

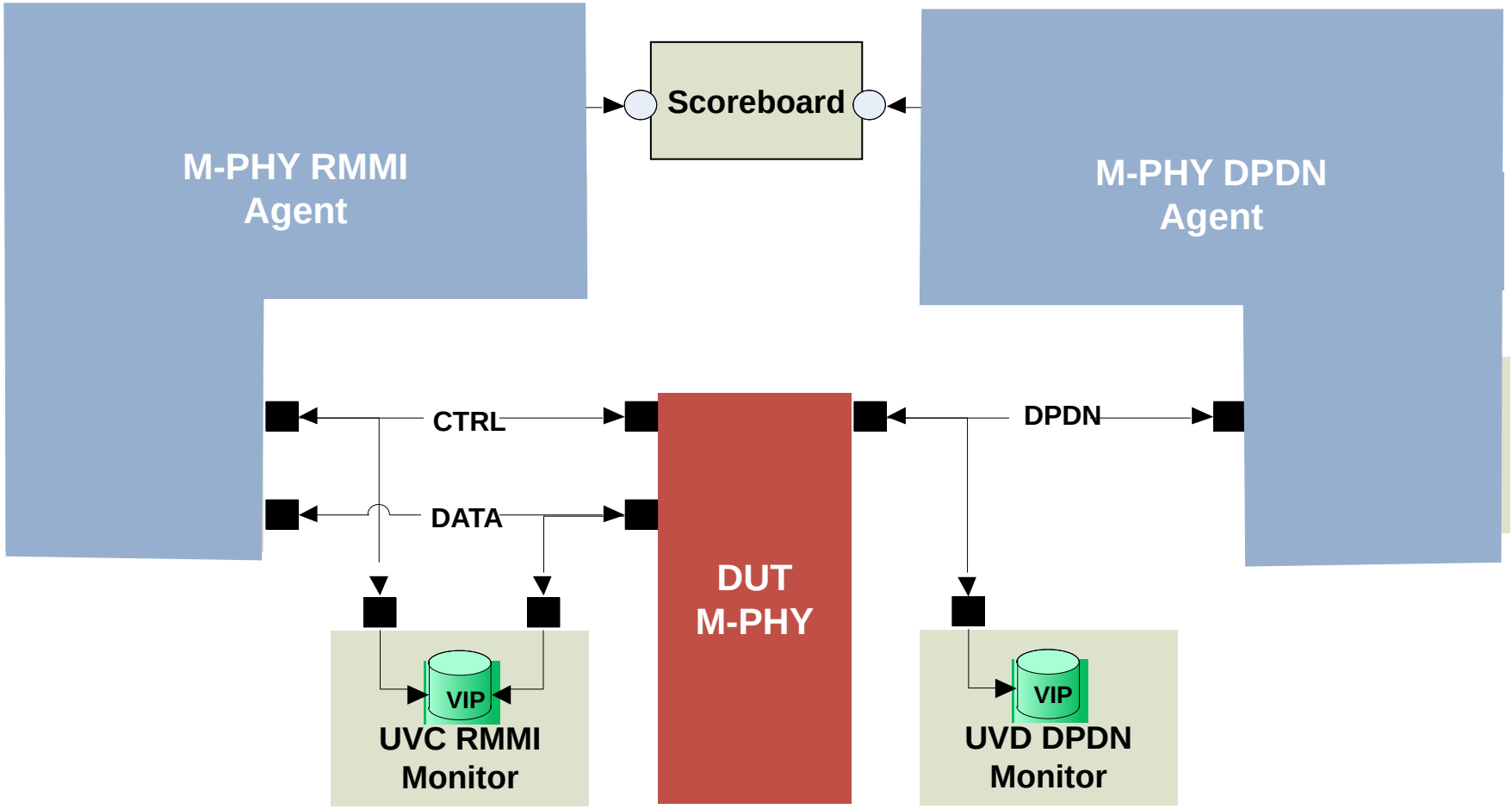
MIPI® Alliance

M-PHY ®

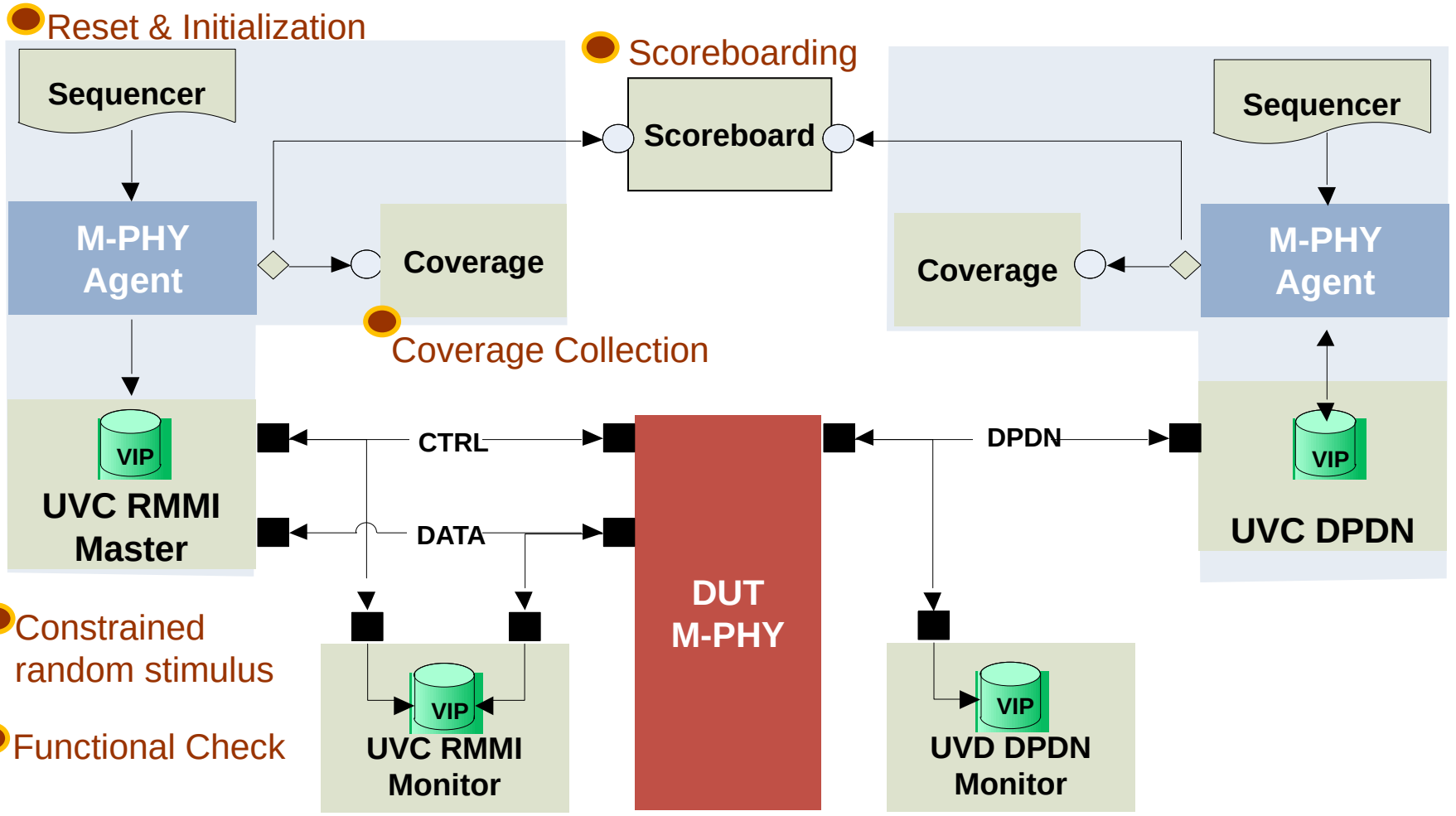
UniPro℠

1. Compliance to Industry Standard(s)

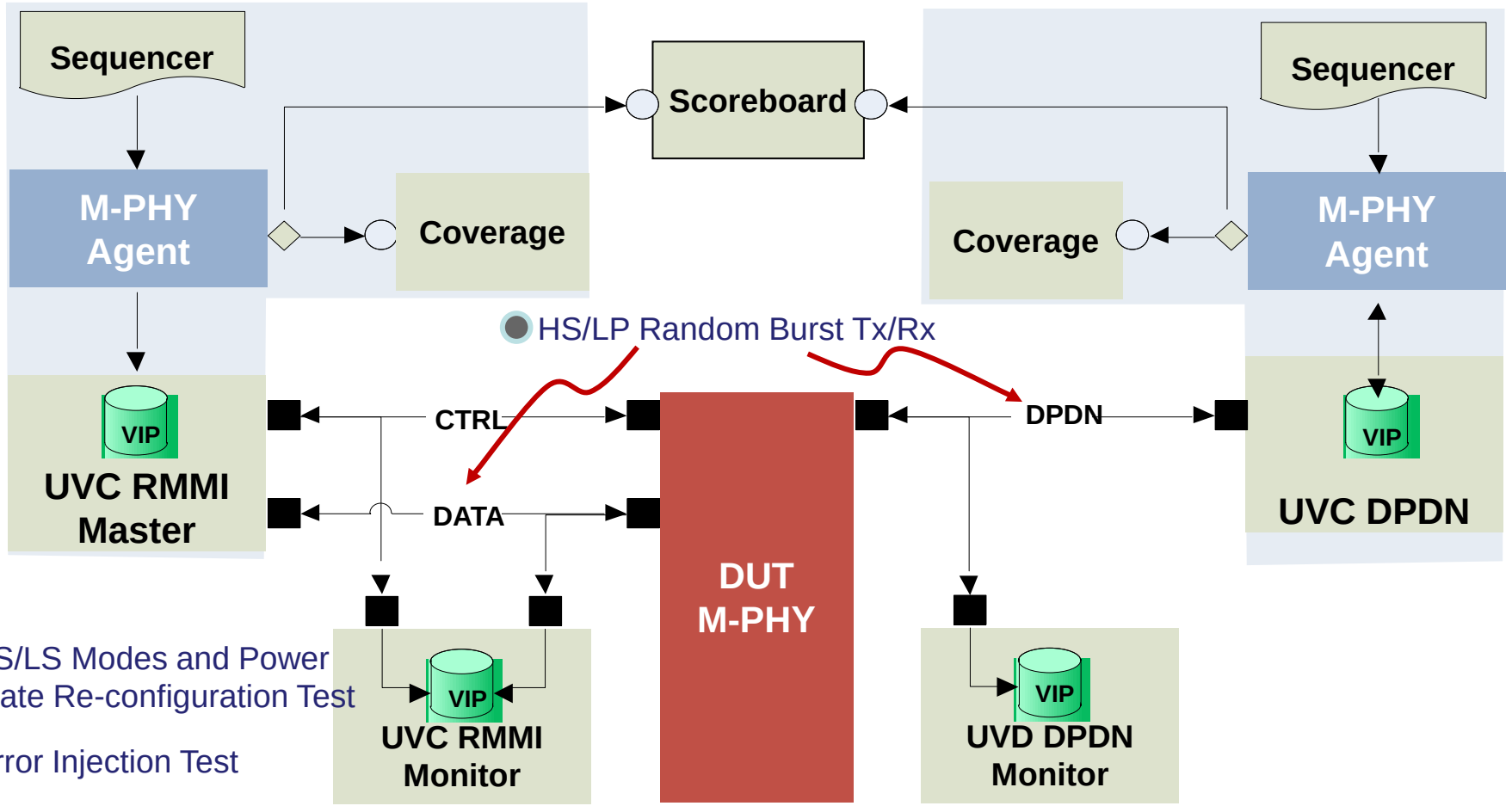
M-PHY ® Verification Before Silicon



M-PHY Verification Before Silicon

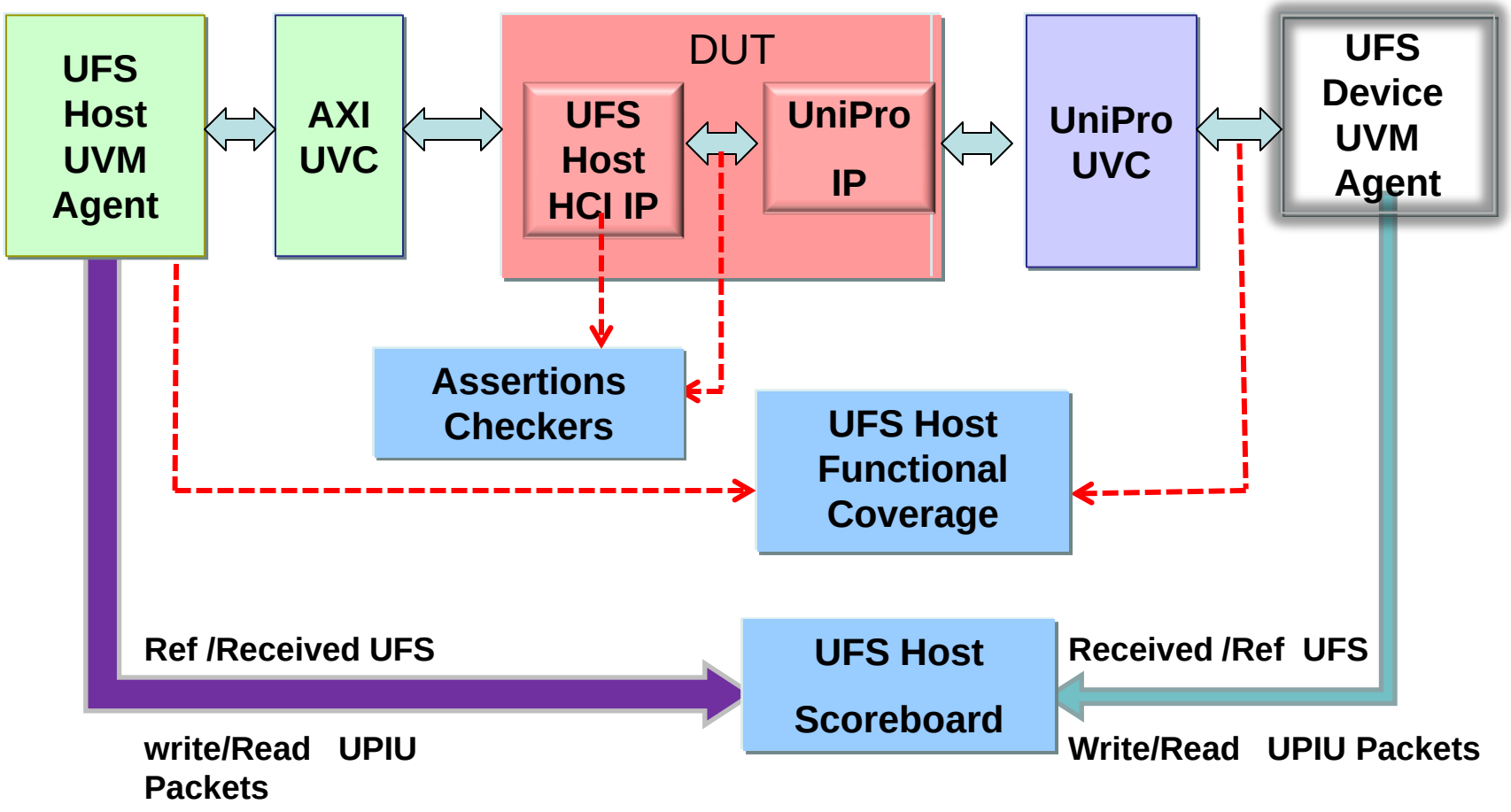


M-PHY Verification Cases



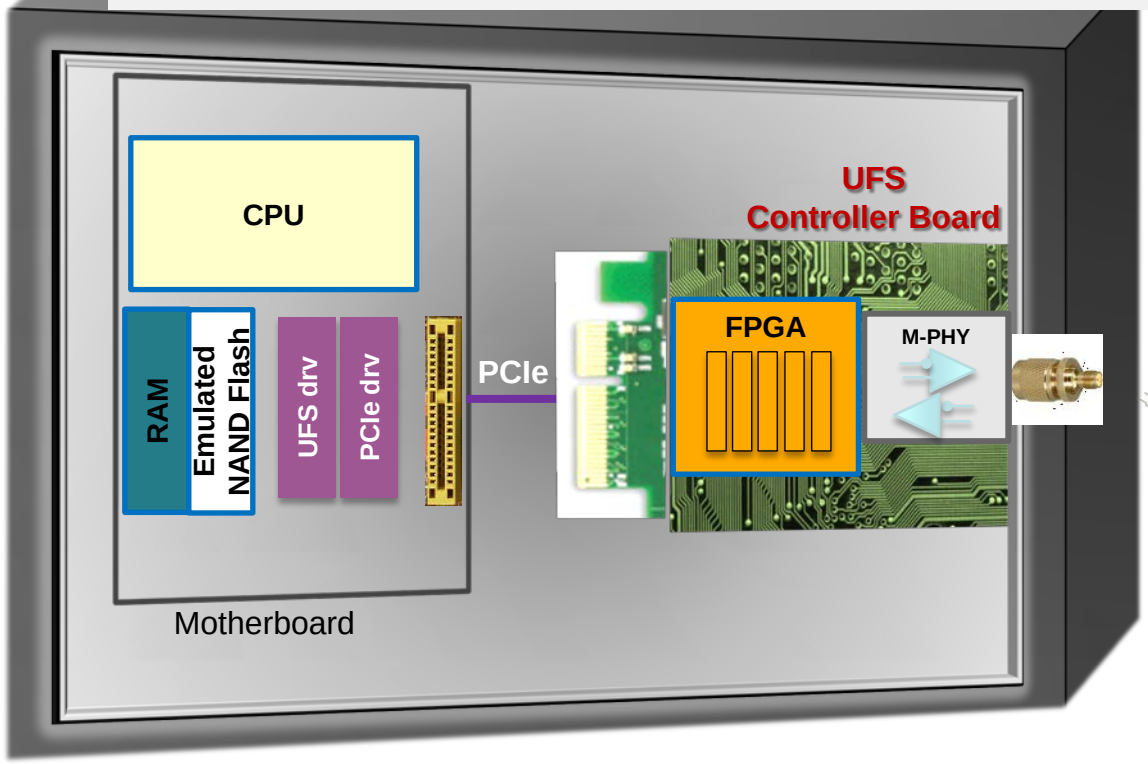
- HS/LS Modes and Power State Re-configuration Test
- Error Injection Test
- Timing – Gate Level Simulation
- HW Reset test
- Attribute read/write test

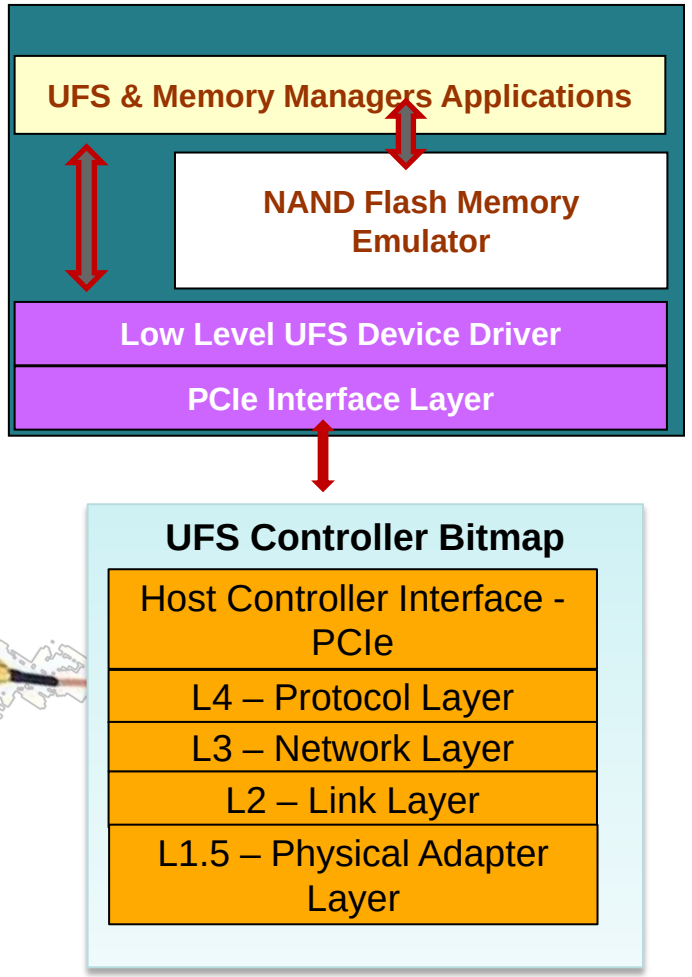
UFS Controller Verification Before Silicon (UFS-HCI + UniPro)



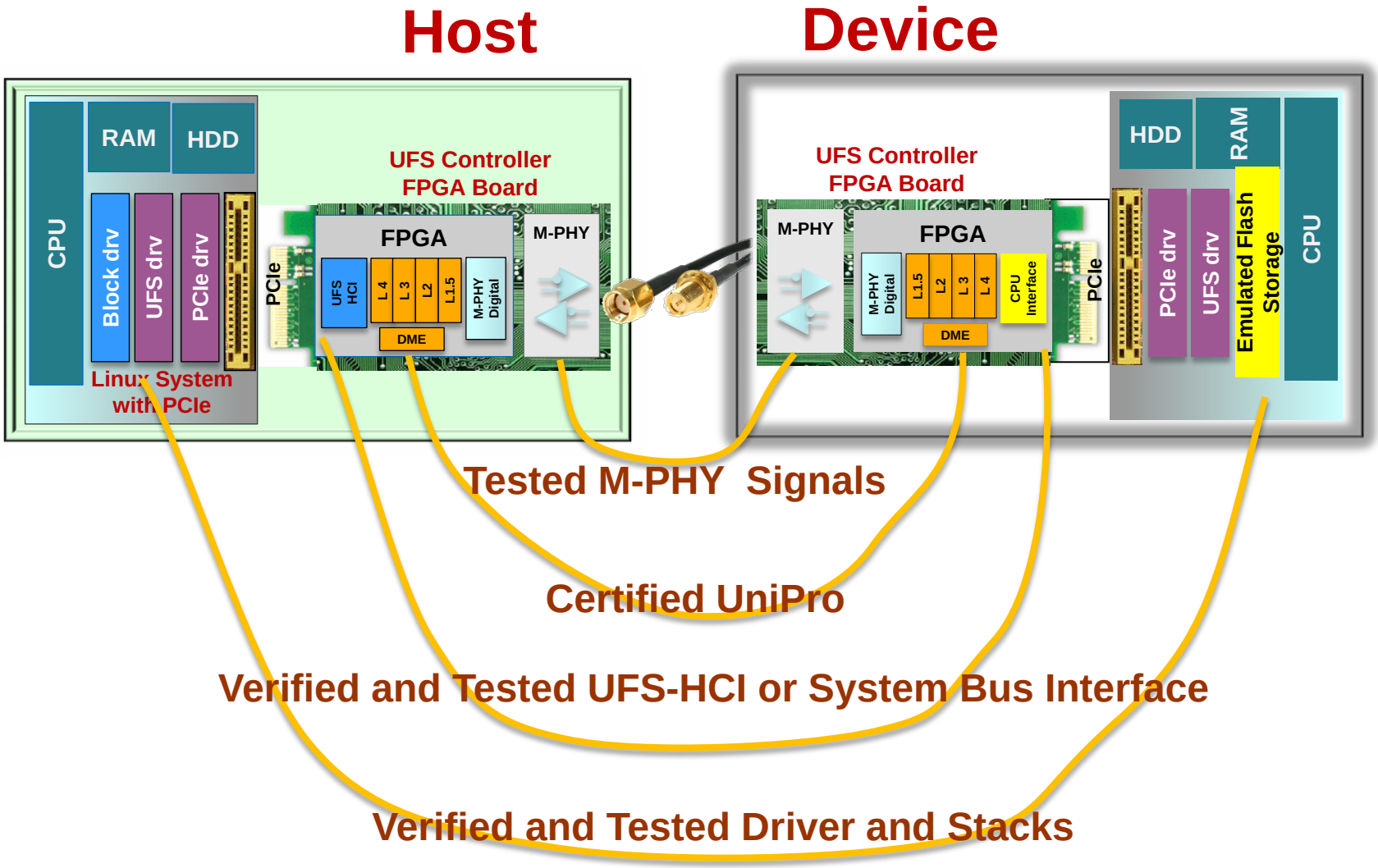
Migrate to FPGA based System

- A black-box approach enables quick access to a validation platform
- FPGA with Verified UFS IP





FPGA System for Device Validation & Software Development



Enabling UFS/eMMC Design Ecosystem

- FPGA based Development Platform productized into **Validation Platform**
  - IP, software stacks and PHY come together
- Used **by IP vendor** (e.g.. Arasan) for Interoperability testing with other pioneers
- Used **by Test & Measurement vendors** as target platforms
  - For validation of protocol generators and analyzers
- Ultimately used **by SoC/Device vendors** as target or reference platforms for silicon validation
  - Assured of IP interoperability, compliance, and backward compatibility

Summary

- **New JEDEC storage standards** continue to evolve for new markets
  - **Early IP/SoC validation** enables compliance and compatibility for fast time-to-market
- Different SoC vendors at **different stages of spec adoption**
  - Different spec revisions from different OEM's
  - **Backward compatibility** and **Interoperability** a must among vendors
- **IP vendors** continue to
  - **Lead the pack** in transforming specs to RTL and GDSII
  - Keeping **backward compatibility** with older standards in new designs
  - Enabling **ecosystem-wide Inter-Op** and **compliance** through
    - Software stacks
    - Hardware Validation Platforms

All items available before starting your SoC/Device designs !!

THANK YOU