3D Vertical RRAM

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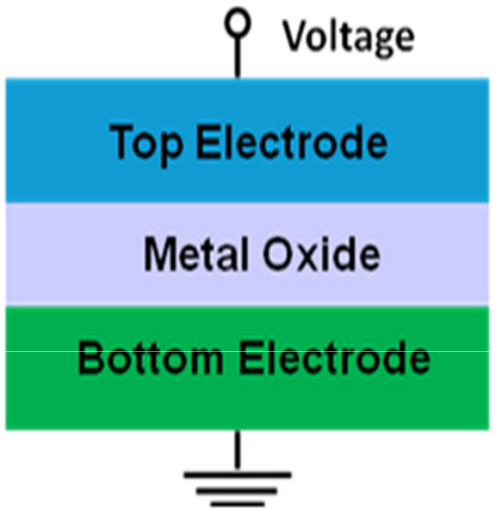
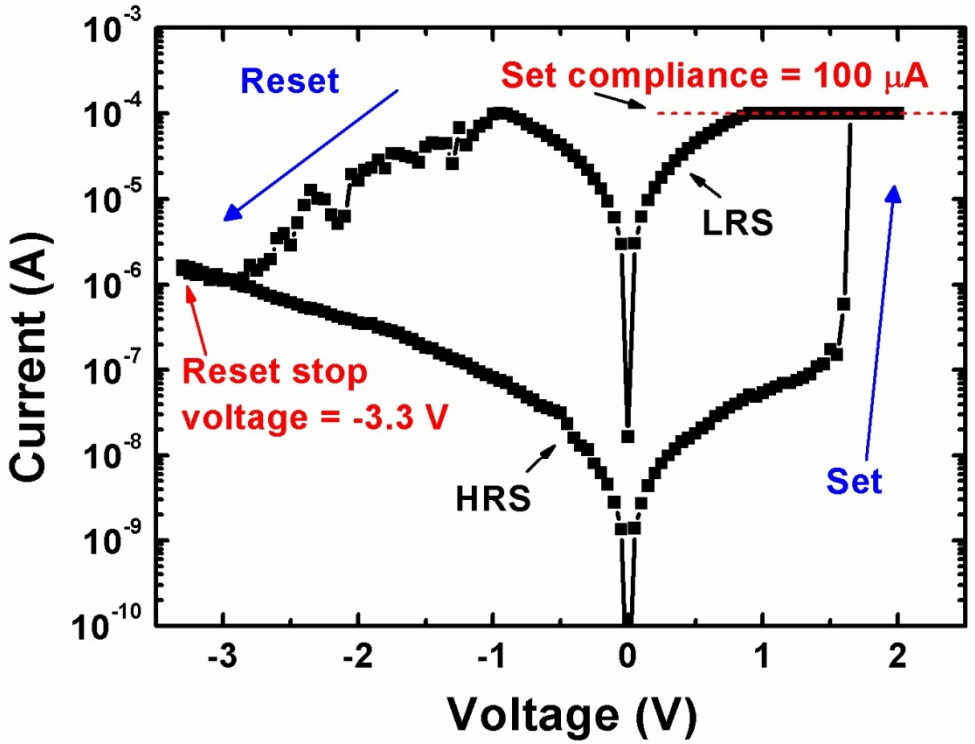
Collaborator: Peking University, China

What is RRAM?





- "0" : High Resistance State (HRS)
- "1" : Low Resistance State (LRS)
- HRS→LRS: SET
- LRS→HRS: RESET

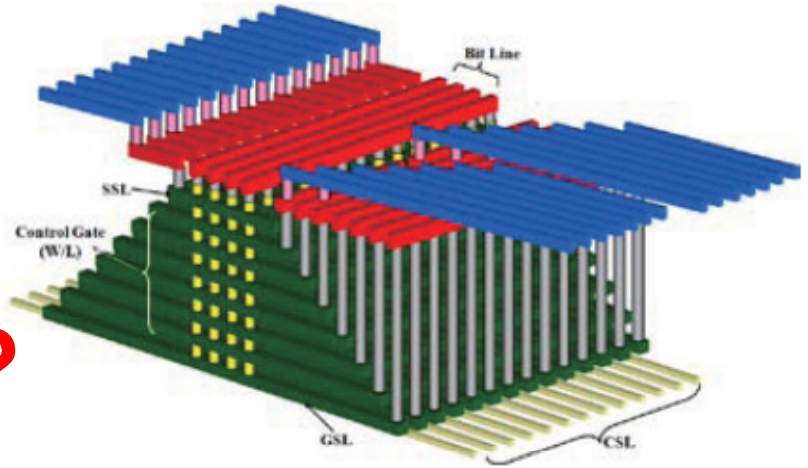
Why 3D Architecture in RRAM?

RRAM has showed excellent single-cell performance.

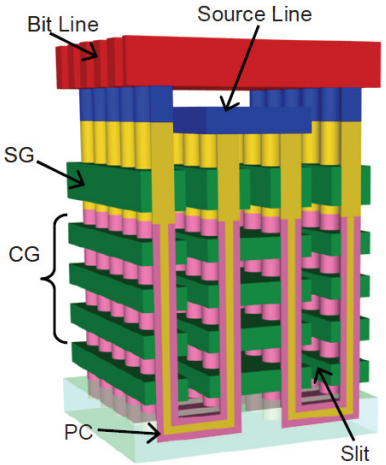
	FLASH	RRAM
cell area (F^2)	<4 if 3D	<4 if 3D
multi-bit	3	3
scalability	<20nm	<10nm
voltage	>20V	<3V
speed	~10µs	<10ns
energy/bit	~100pJ	~0.1pJ
endurance	<1E5	1E6-1E12
retention	>10years	>10years

??

A technology path toward 3D integration is needed in RRAM.



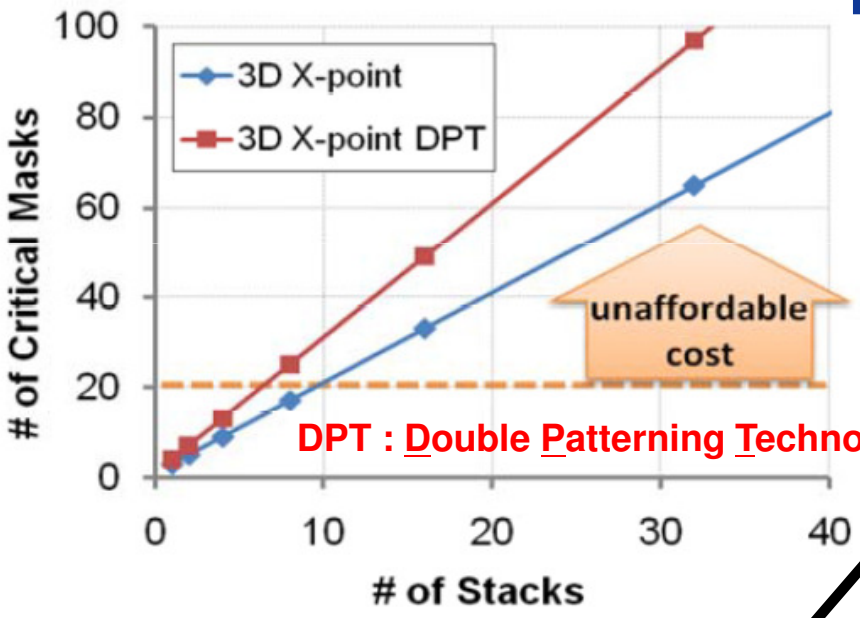
3D NAND by Samsung, VLSIT, 2009



3D NAND by Toshiba , VLSIT, 2009

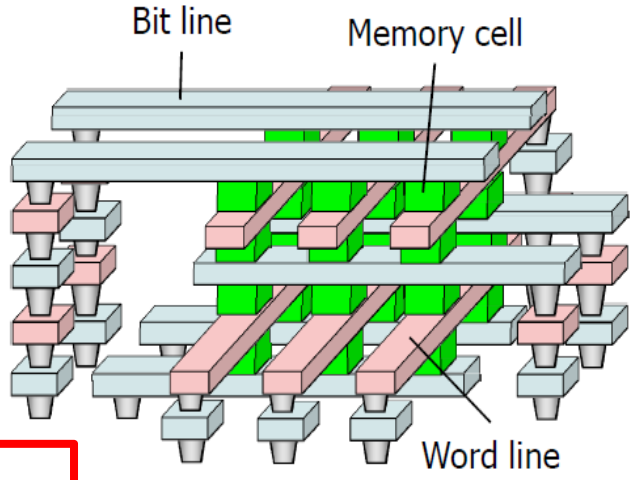
Bit-Cost Effective 3D Integration

Horizontal RRAM Estimated Cost



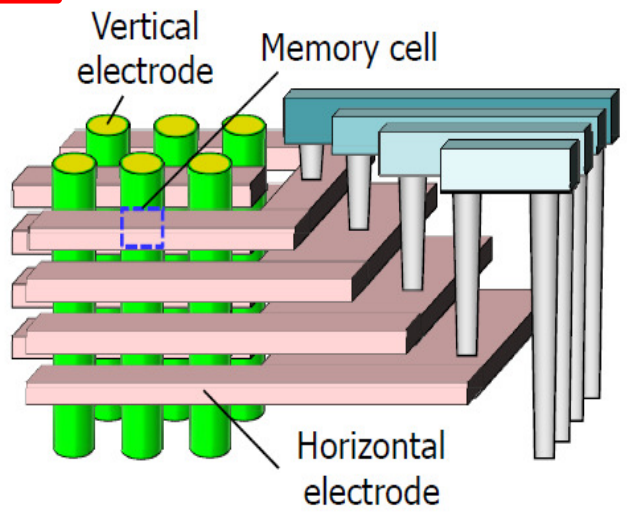
DPT : Double Patterning Technology

Horizontal RRAM



V.S.

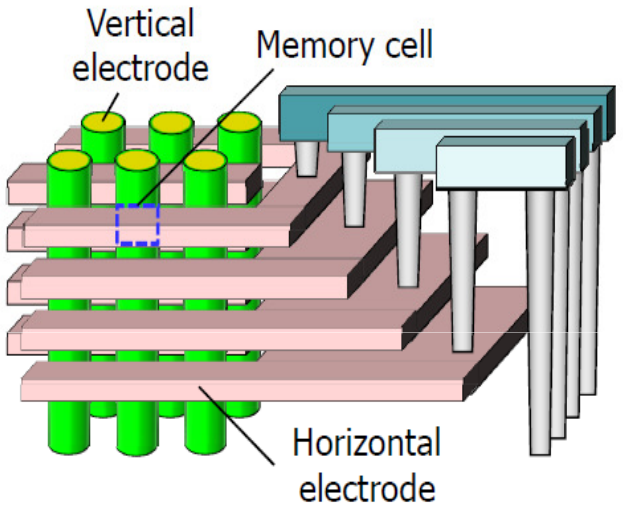
Vertical RRAM

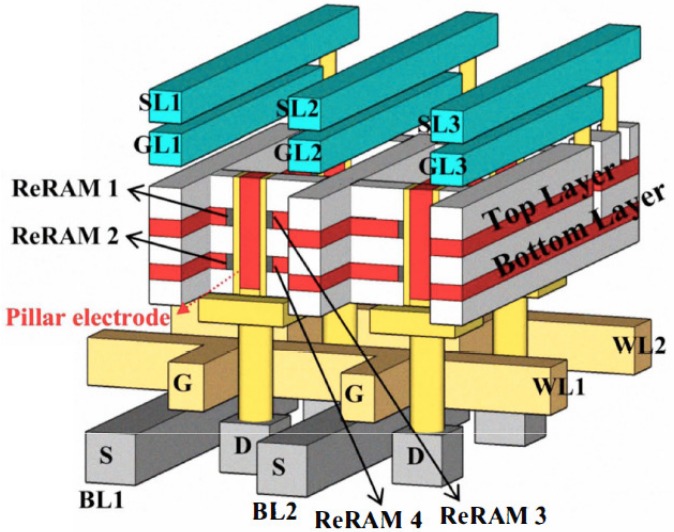


I. G. Baek, *et al.*, IEDM, 2011 (Samsung)

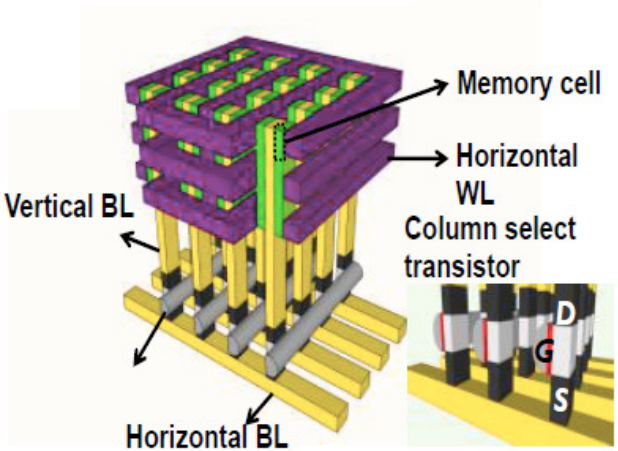
Various 3D VRRAM Architectures

I. G. Baek, *et al.*, IEDM, 2009 & 2011(Samsung)





W.-C. Chien , *et al.*, VLSI, 2012(Macronix)

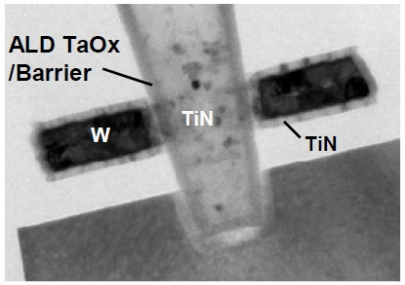


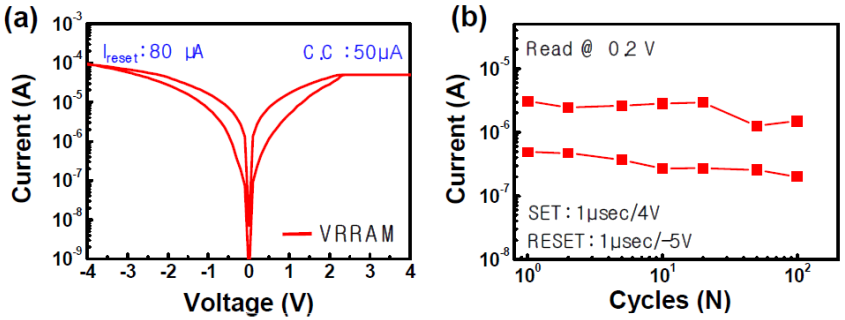
L. Zhang, *et al.*, IMW, 2013(IMEC)

Recent Advances in Demonstration

1. Samsung [I. G. Baek, *et al.*, IEDM, 2011]

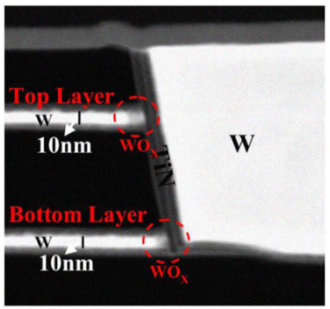
TiN/TaOx/barrier/TiN
Size: 30nm in width
Switching Voltage:~3/-4V
Reset Current: ~80 μA
Endurance: 100 Cycles

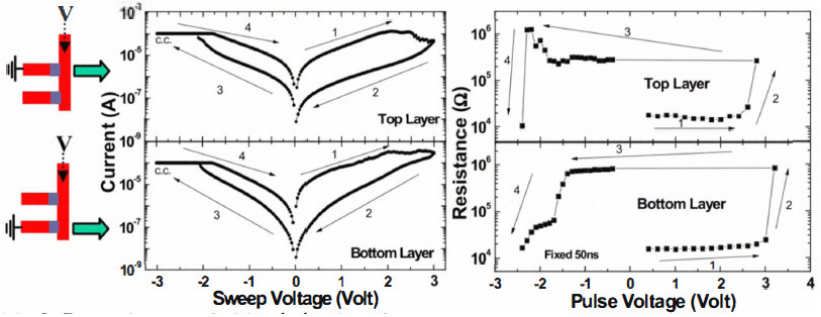




2. Macronix [W.-C. Chien , *et al.*, VLSI, 2012]

W/WOx/SP-TiN/TiN
Size: 10nmx100nm
Speed: ~50ns
Reset Current: ~200 μA
Switching Voltage:~3/-2.5V
Good read immunity
Endurance: 600 Cycles(T)
Endurance: 300 Cycles(B)





Outline

- 3D Vertical RRAM Demonstration
- Key Issues for 3D Memory Array
- Summary

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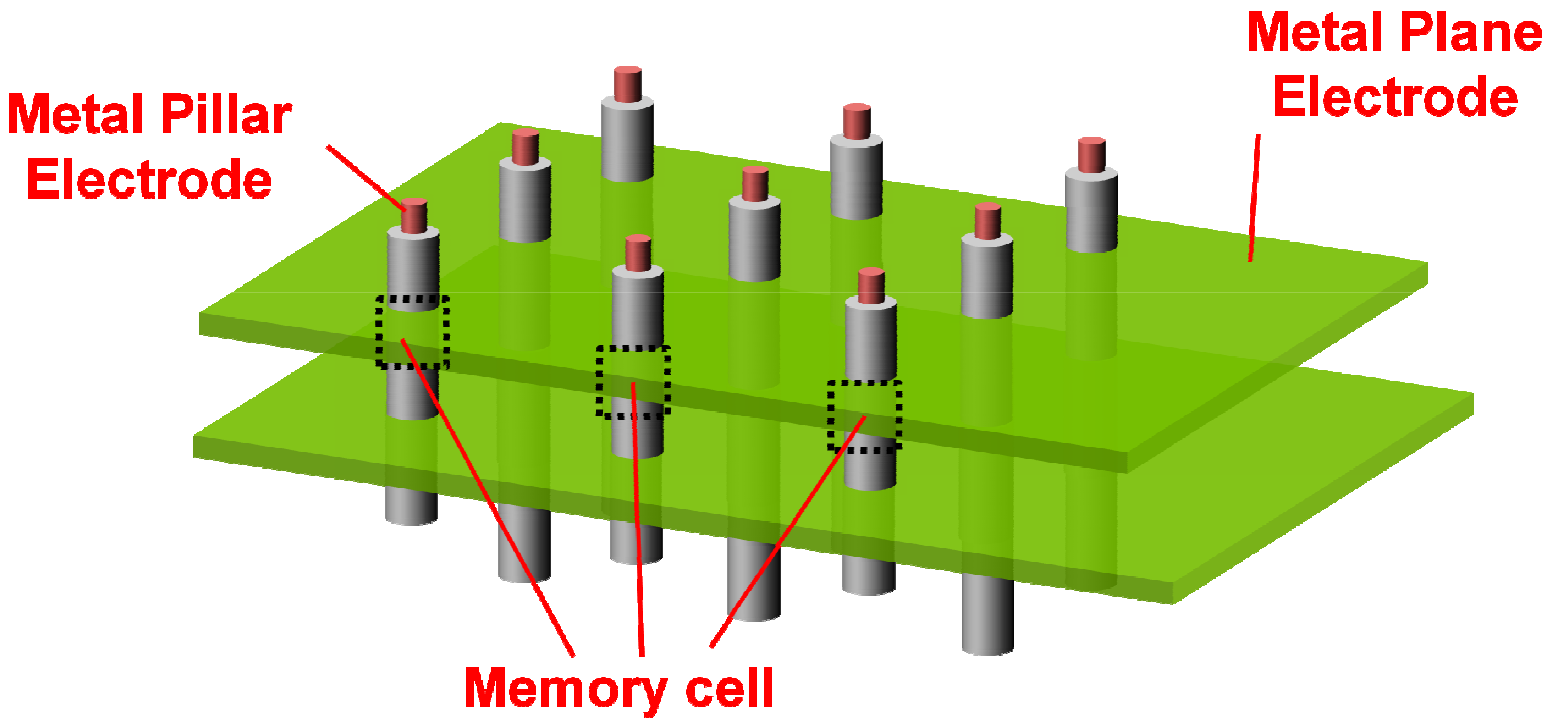
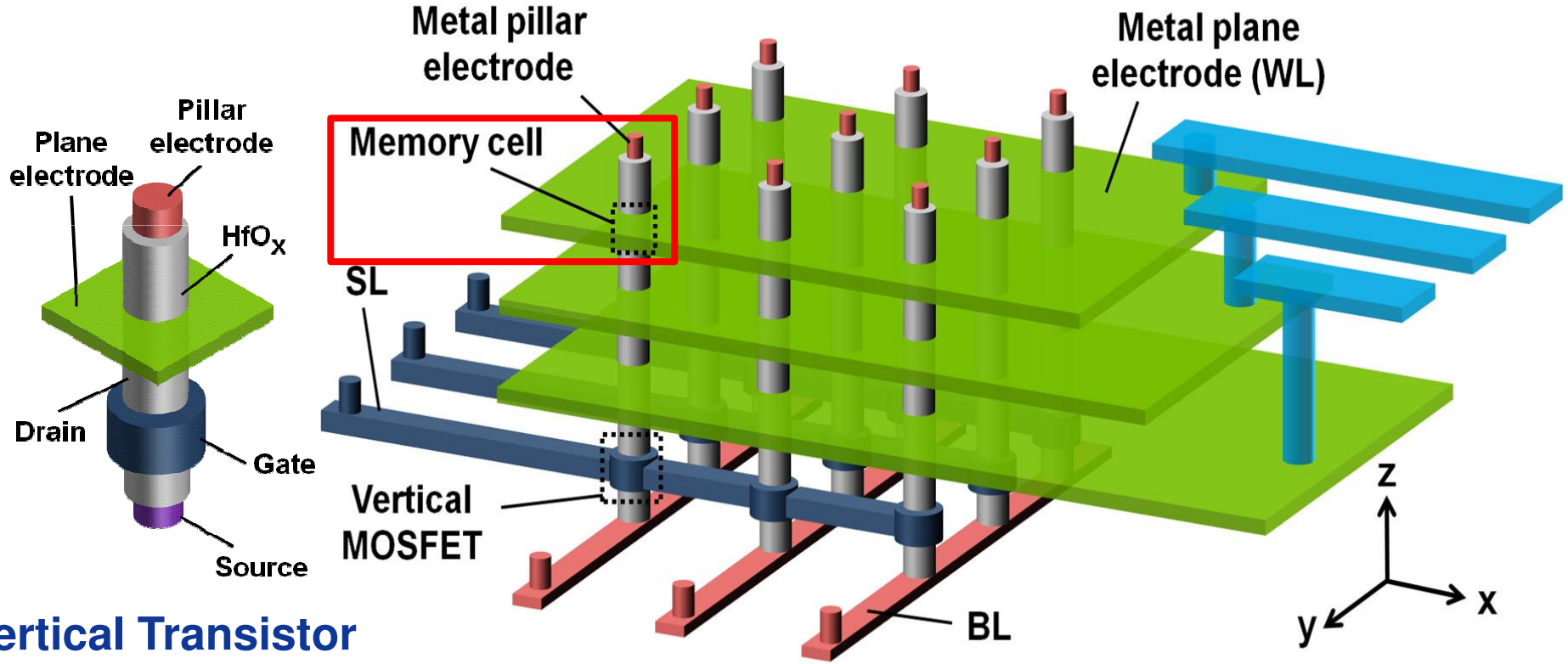
3D Cross-Point Using Metal Planes



H.-Y. Chen, *et al.*, IEDM, 2012 (Stanford)

3D Cross-Point Using Metal Planes

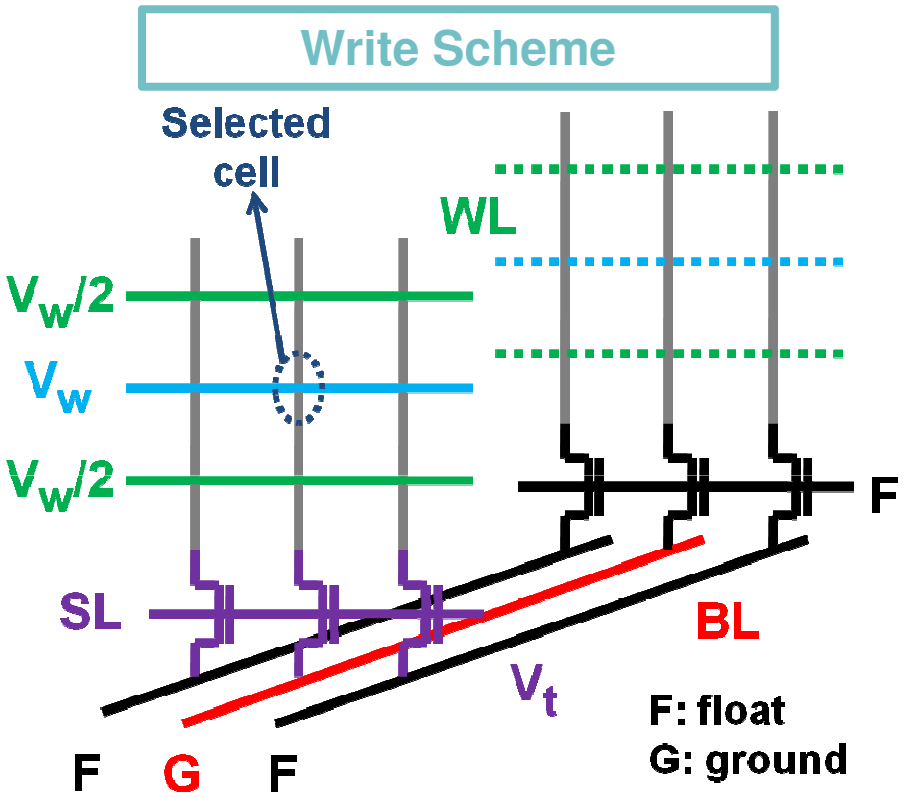
Each Vertical RRAM Cell is randomly accessible in the array!

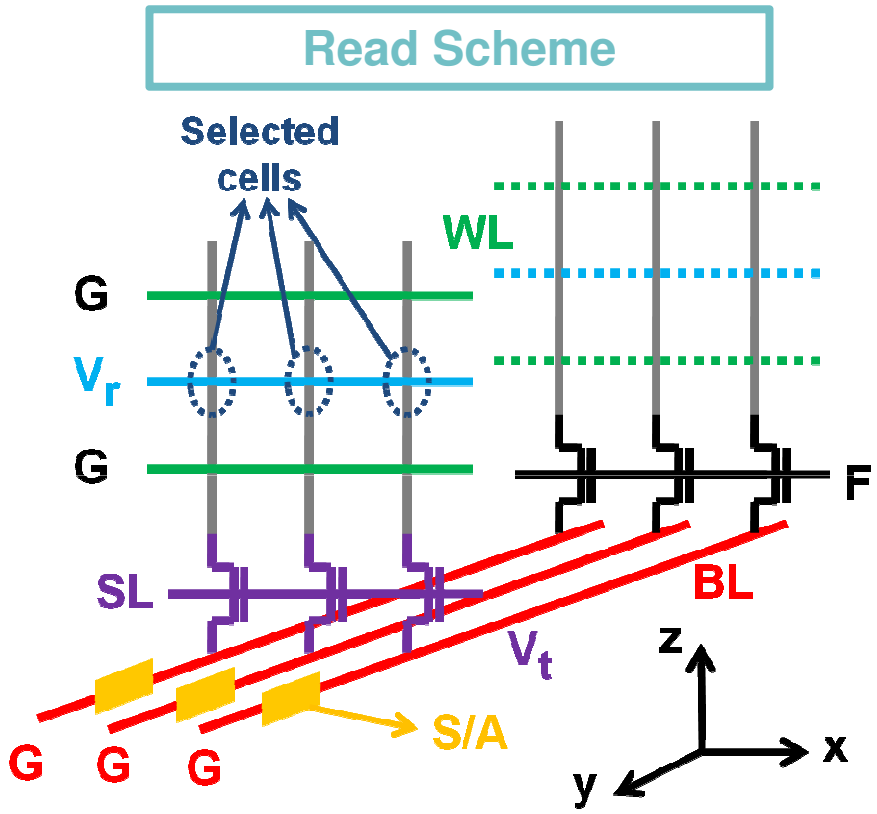


Vertical Transistor

H.-Y. Chen, *et al.*, IEDM, 2012 (Stanford)

3D VRRAM: Write/Read Scheme



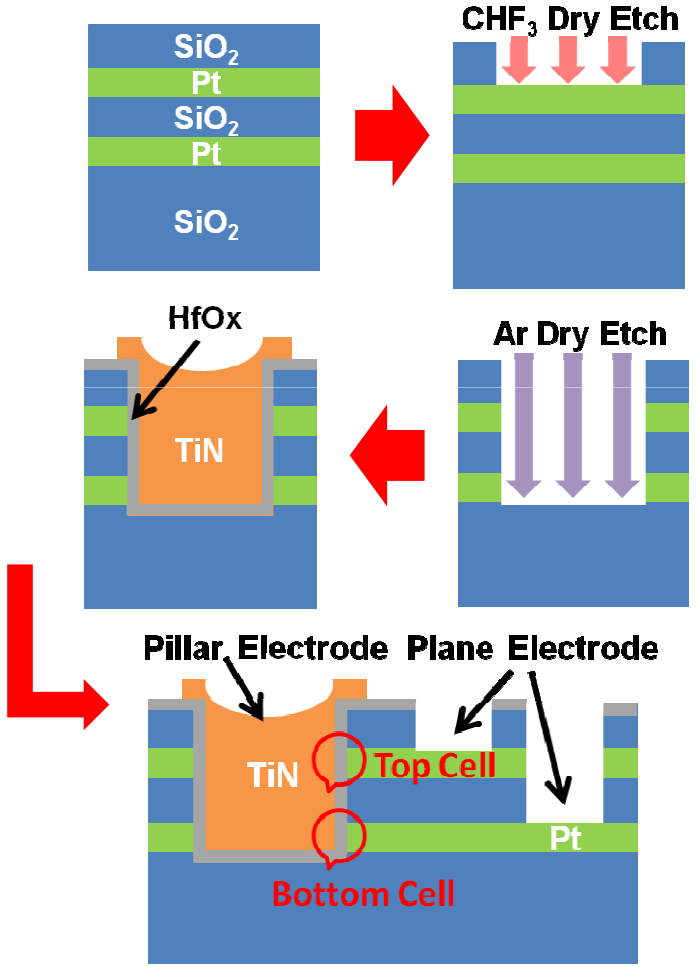


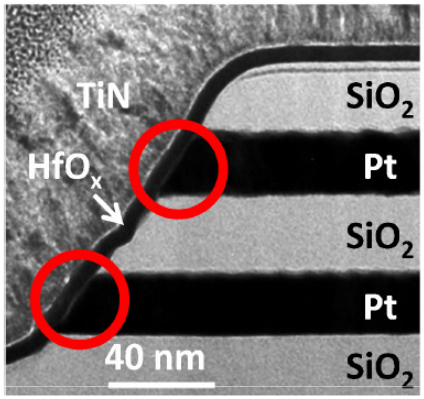
1. Vw applied to the selected cell's WL
2. Vw/2 applied to unselected cells' WL (to avoid unintentional writing)
3. SL of the selected cell's pillar turned on
4. BL of the selected cell's pillar ground

1. Vr applied to the selected cells' WL
2. SL that controls the selected cells turned on
3. The data of a row of cells read out by the sense amplifier (S/A)

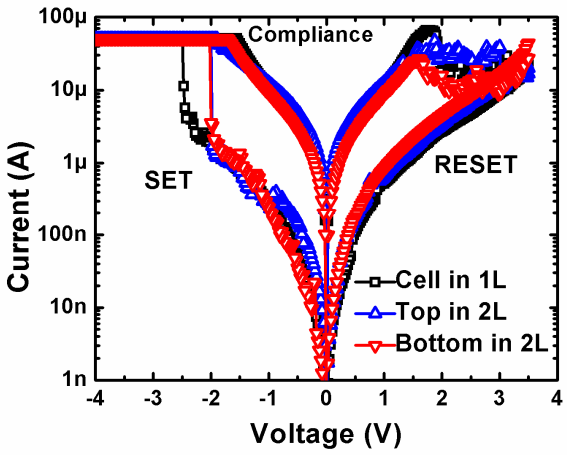
H.-Y. Chen, *et al.*, IEDM, 2012 (Stanford)

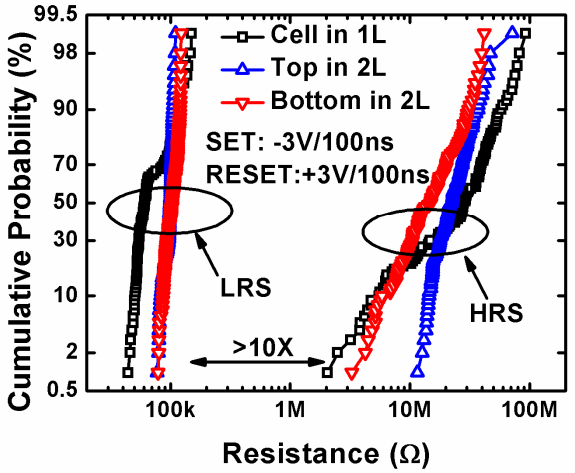
Device Fabrication and Performance





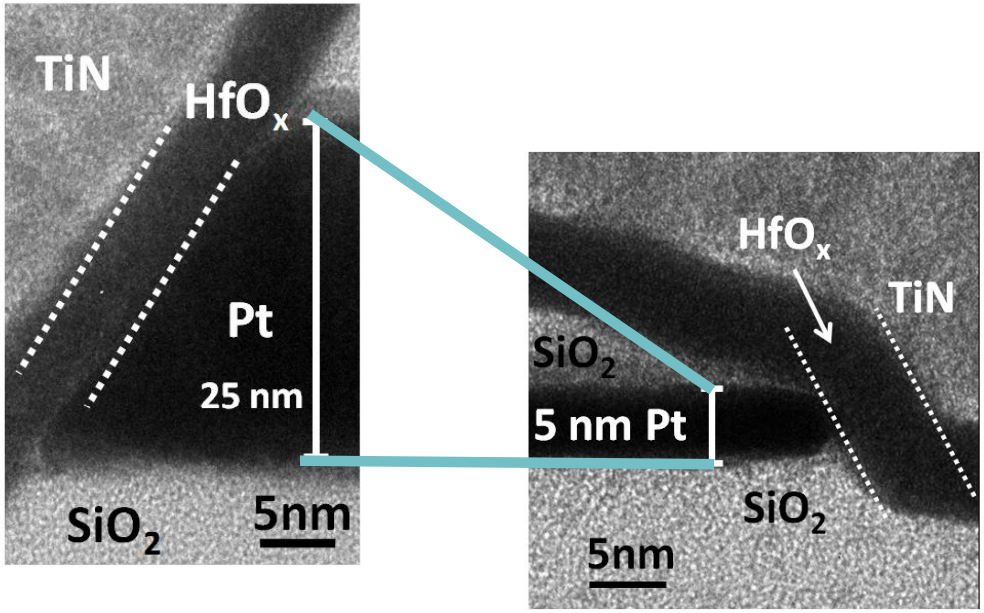
voltage	<3.5V
current	~50 μA
speed	~100 ns
R_{on}/R_{off}	100kΩ/10MΩ
endurance	>1E8
retention	>28h@125C



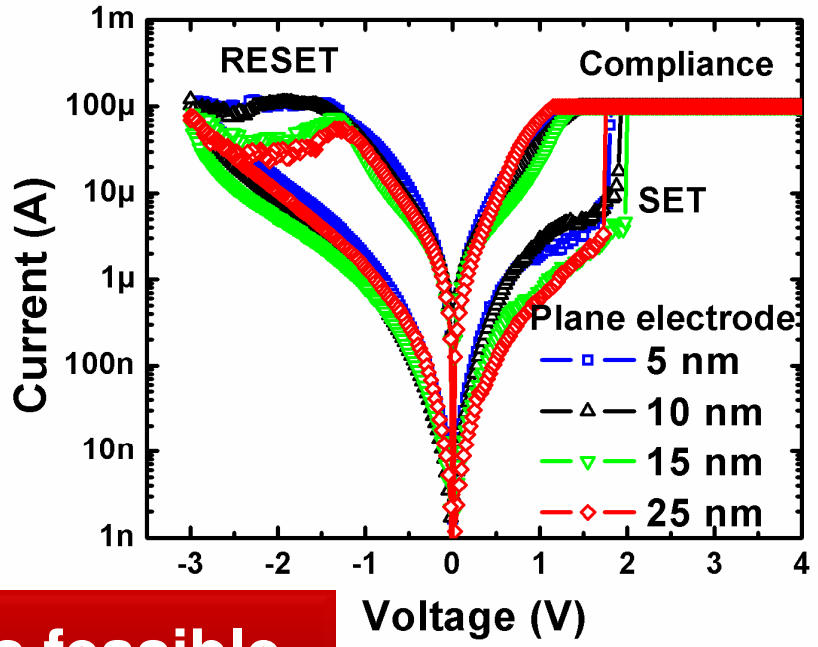


H.-Y. Chen, *et al.*, IEDM, 2012 (Stanford)
S. Yu, H.-Y. Chen, *et al.*, VLSIT, 2013 (Stanford)

Metal Electrode Scaling

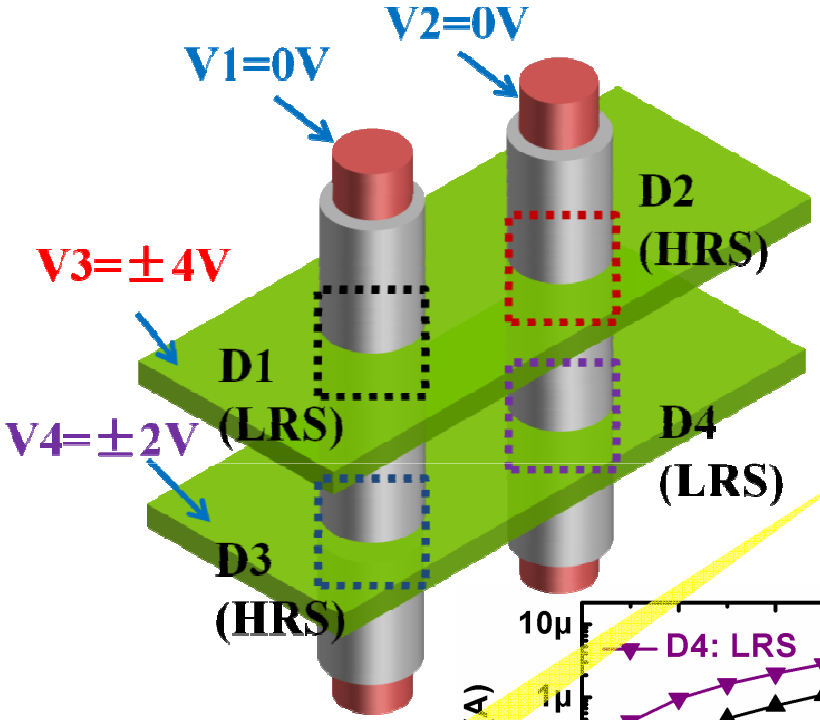


H.-Y. Chen, *et al.*, under review (Stanford)
S. Yu, H.-Y. Chen, *et al.*, VLSIT, 2013 (Stanford)



Metal electrode scaled to 5 nm is feasible.
=> Improve integration density

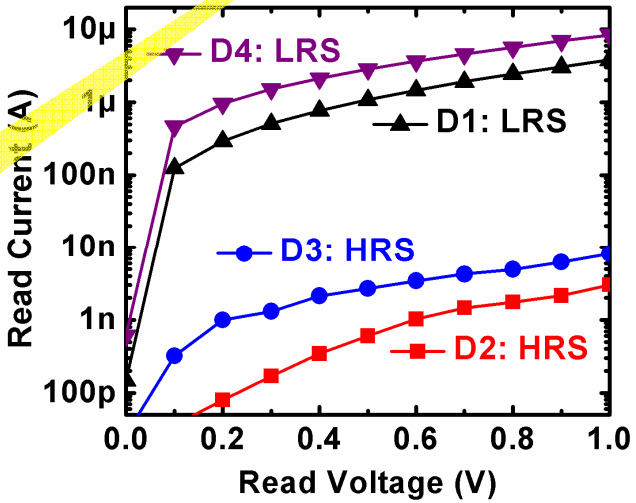
Demonstration of Array Operation

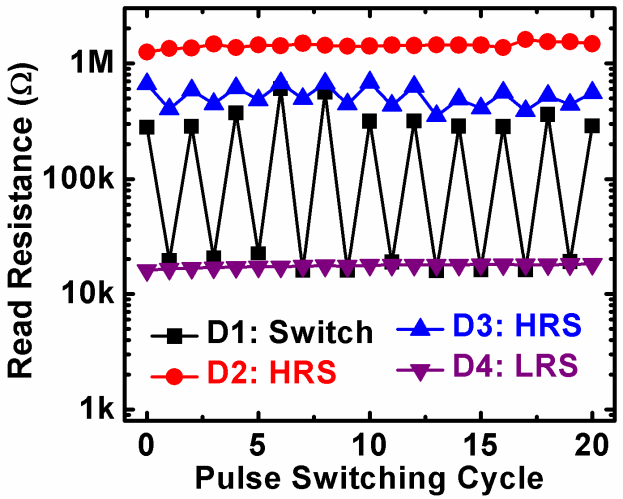


	V1	V2	V3	V4
Read D1&D2	0	0	0~1V	0
Read D3&D4	0	0	0	0~1V
SET D1	0	Float	-4V	-2V
RESET D1	0	Float	+4V	+2V

V/2 write scheme

S. Yu, H.-Y. Chen, *et al.*, VLSIT, 2013 (Stanford)





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- 3D Vertical RRAM Demonstration
- **Key Issues for 3D Memory Array**
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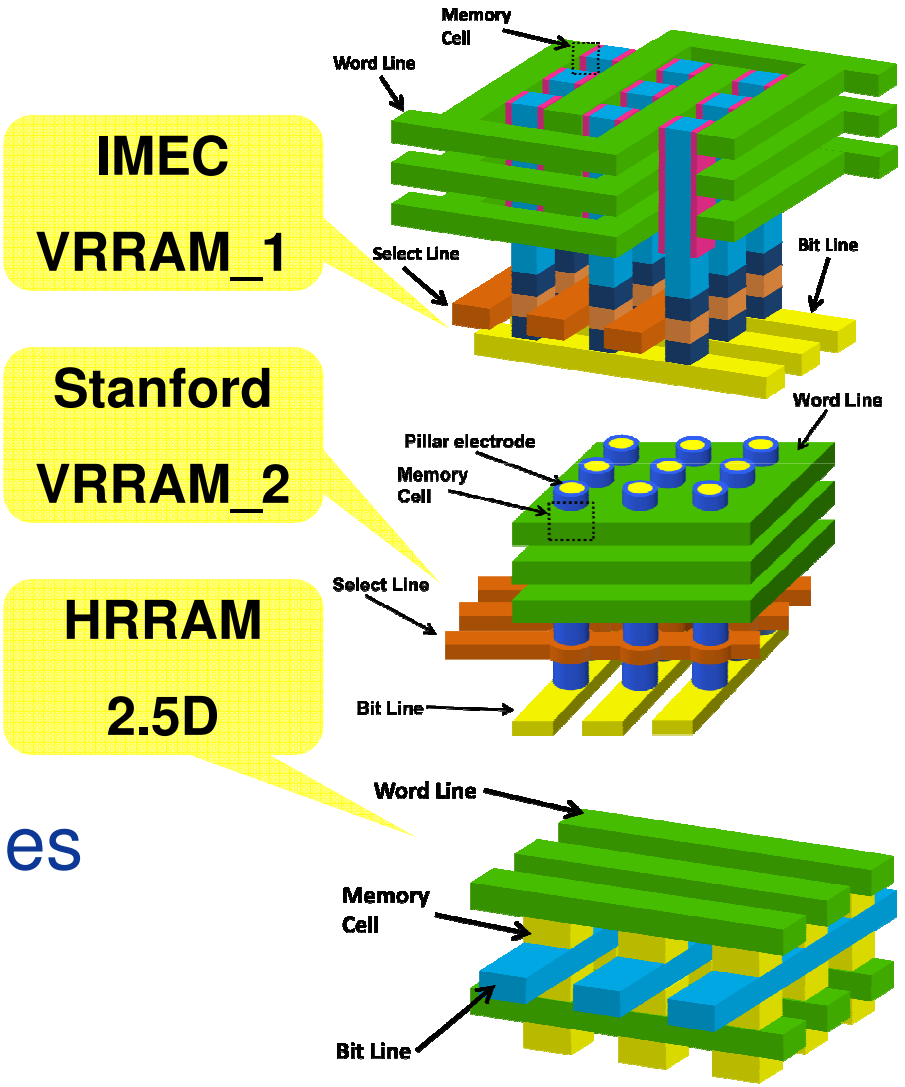
Challenges for 3D Memory Array

- Sneak path leakage
- Selection Device
- Parasitic capacitance
- Line resistance
- Plane resistance
- Interconnection
- Fabrication technologies



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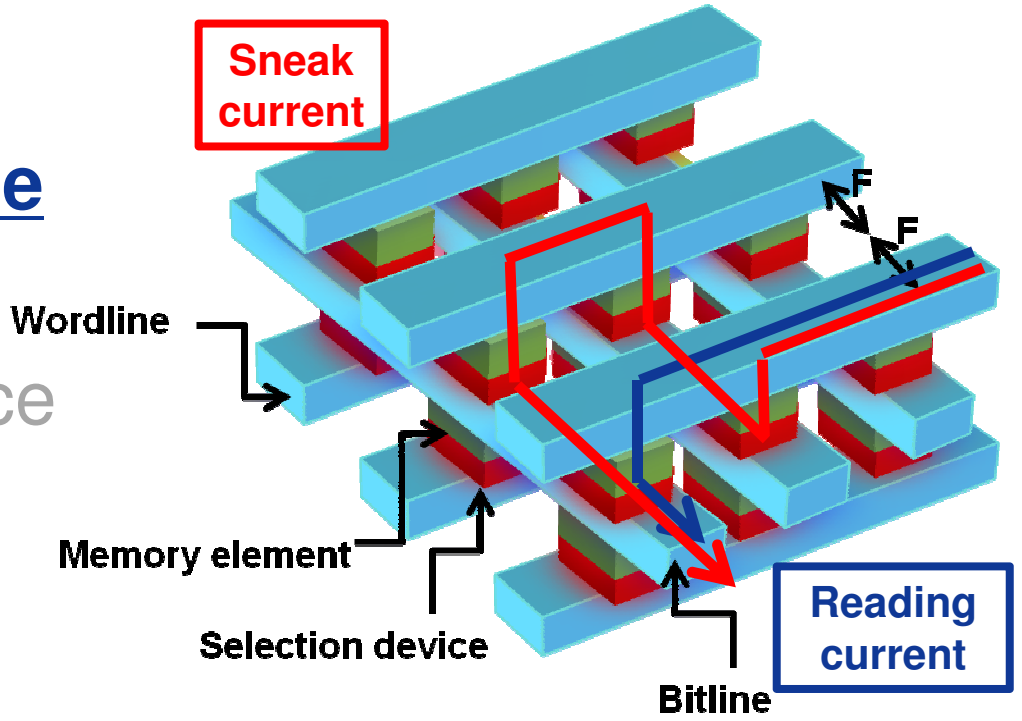

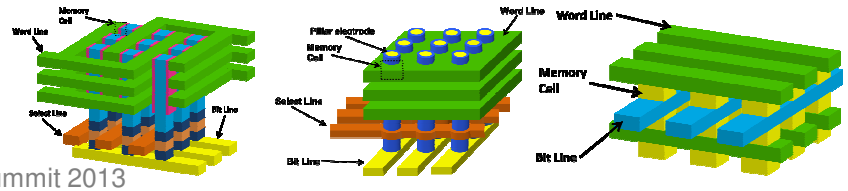

Sneak path causes read disturbance problem and increases the power consumption.

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Sufficient on/off ratio requirement

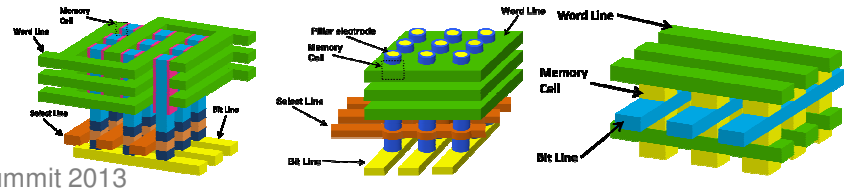
High current density requirement
Ex. (>10MA/cm^2)

Polarity requirement

High endurance requirement

Scalability requirement

3D low temperature fabrication requirement…



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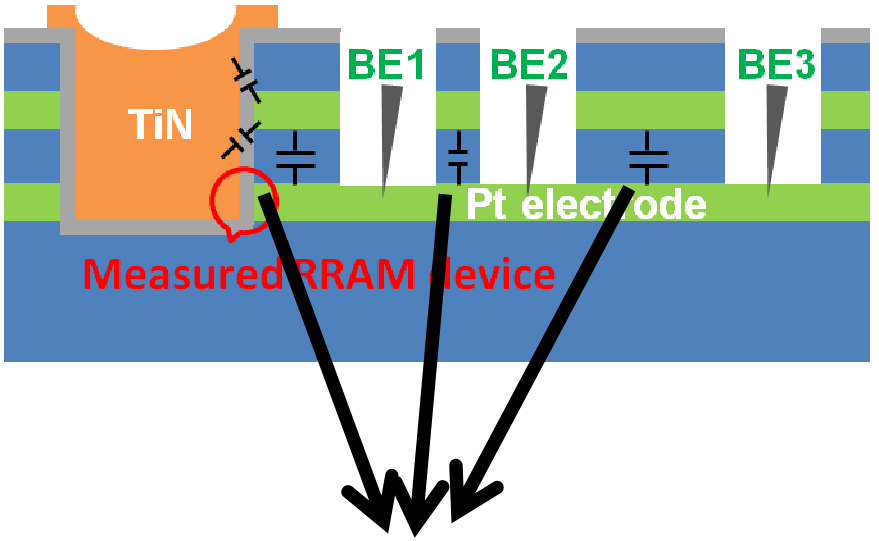
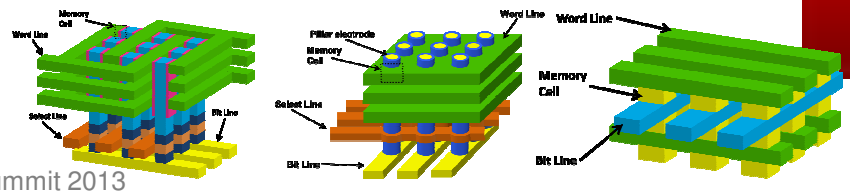


Parasitic capacitance causes RC delay.



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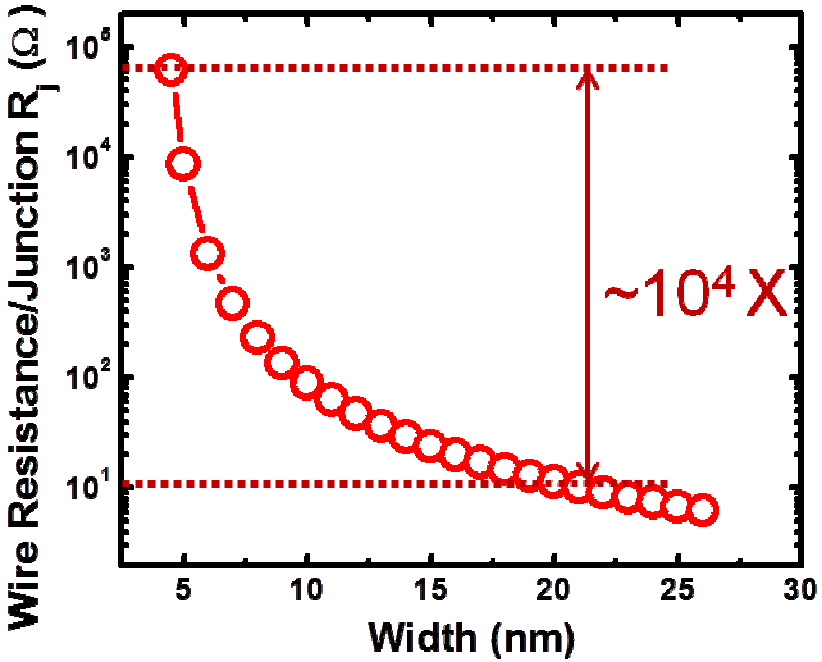
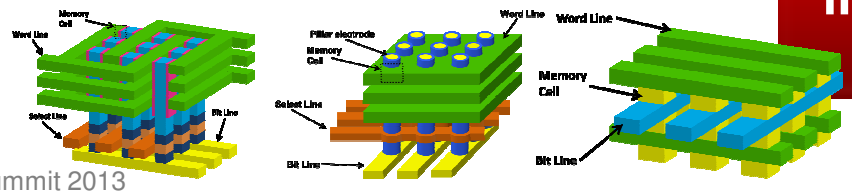


~ 4 orders of magnitudes' increase in R_j at scaled wire dimensions.



J. Liang, et al. IMW 2012, p. 61.

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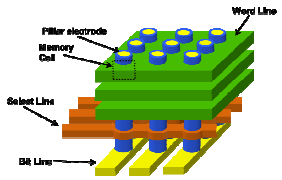

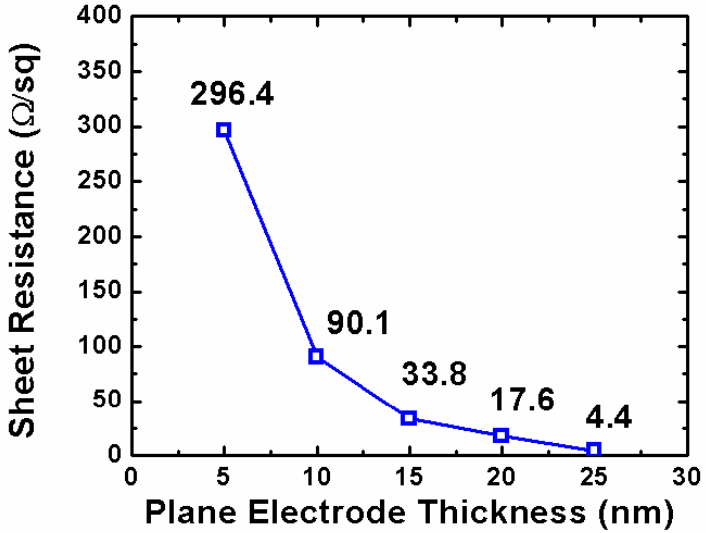

The thinner the electrode, the more resistive plane electrode =>Higher switching voltages

H.-Y. Chen, *et al.*, under review (Stanford)

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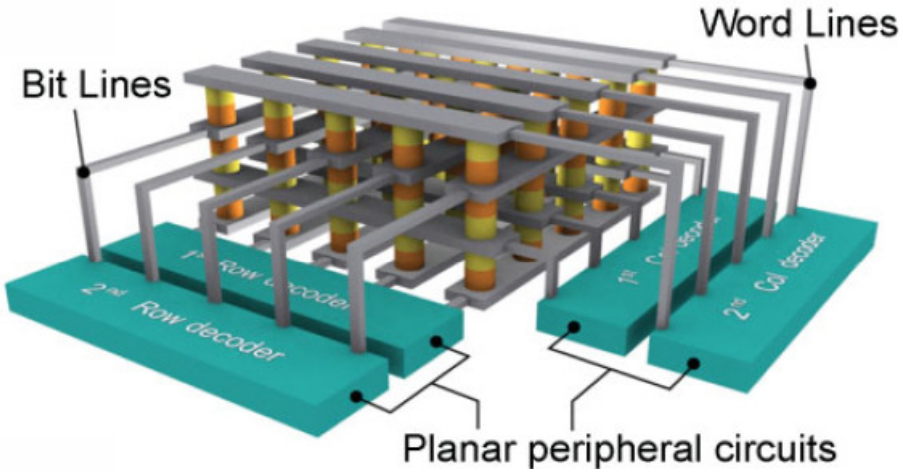
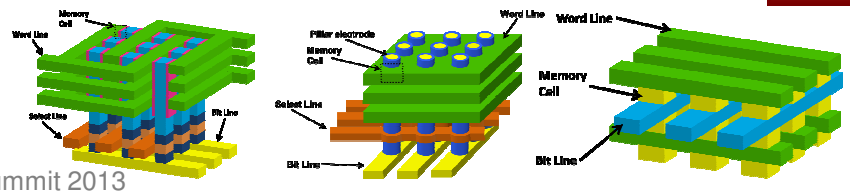


Complicated wire routing
Increased circuit overhead



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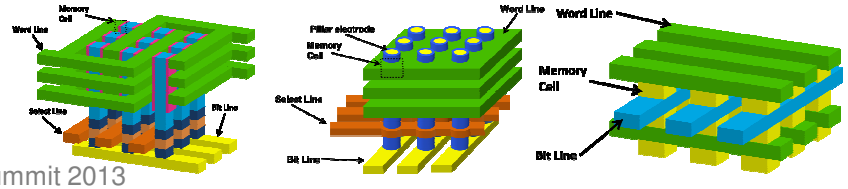

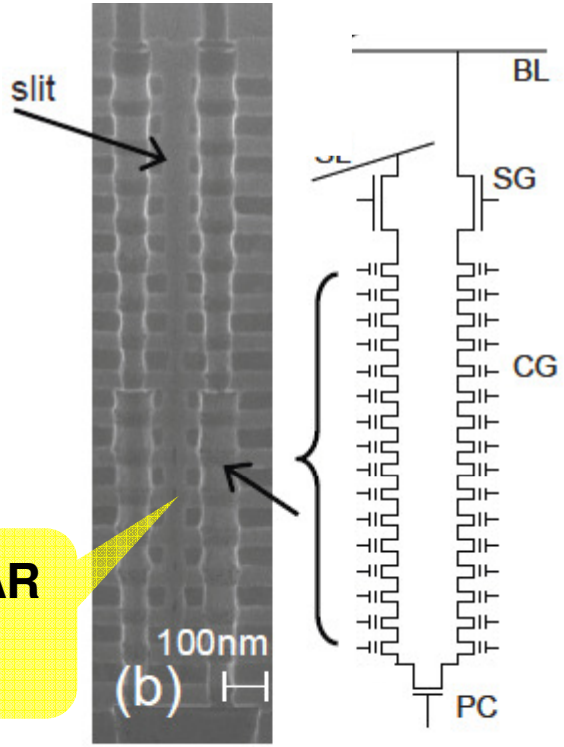

Etching AR ~ 30

R. Katsumata, et al. ***VLSI 2009, p. 136.***

Etching capability
CMOS-friendly material

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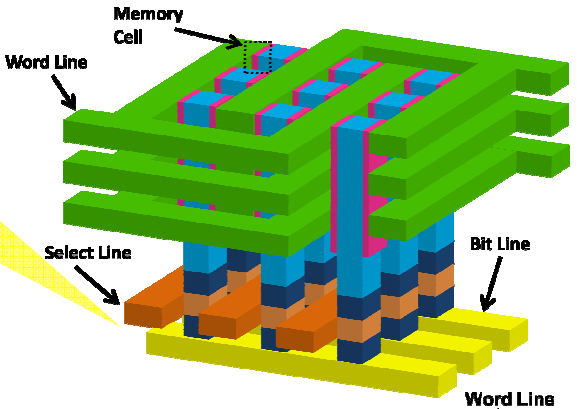
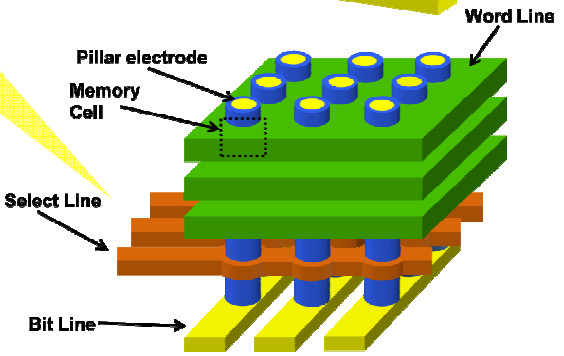
All the 3D array designs face the similar challenges with the different degree of influence.

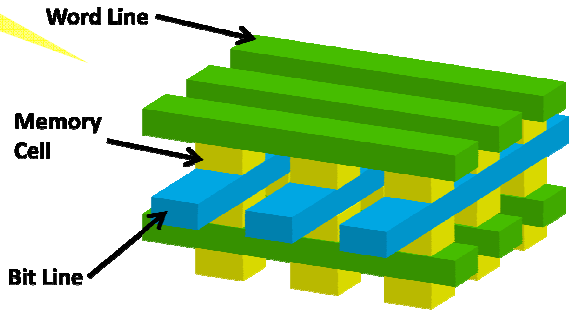
IMEC VRRAM_1



Stanford VRRAM_2



HRRAM 2.5D



Summary

- **3D vertical RRAM cross-point array is promising for next generation mass storage due to the effective bit cost.**
- **A comprehensive understanding for the particular VRRAM array is reported in this talk:**
  - **(1) memory architecture design**
  - **(2) read/write schemes**
  - **(3) device fabrication, scaling, and characterization**
  - **(4) array operation demonstration**
- **Key issues for developing 3D memory array were discussed.**

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- 973 Program (2011CBA00602), China
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- H.-Y. Chen is additionally supported by
  - Intel Fellowship
  - Taiwanese Government Scholarships to Study Abroad
  - IEEE Electron Devices Society PhD Student Fellowship

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