New wafer level stacking technologies and their applications

WDoD™ a new 3D PLUS technology

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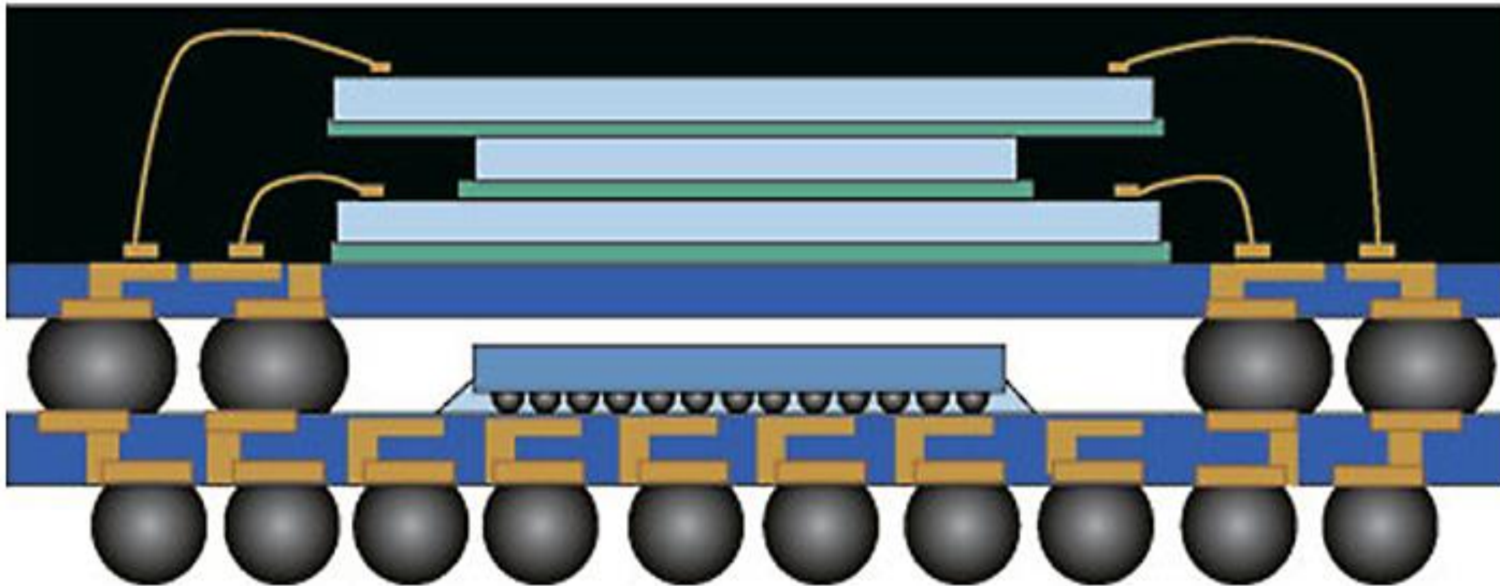
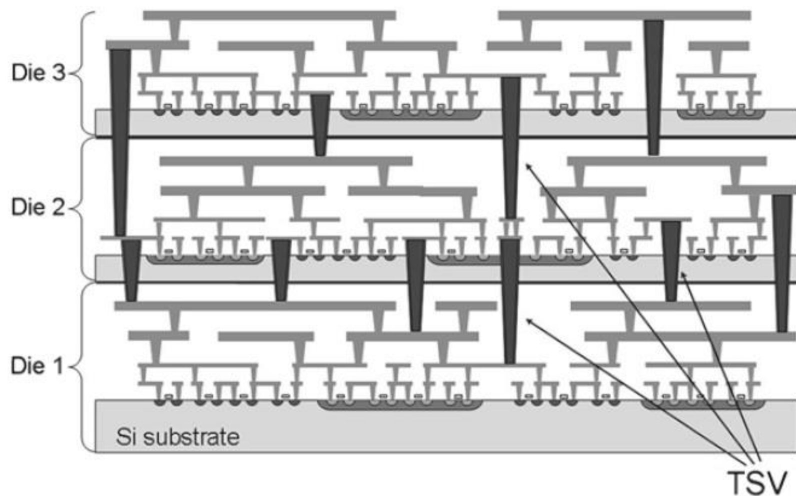
Existing wafer level assembly processes: die on die and PoP

- Today, using the PoP technology, the assembly houses can assemble die and BGA packages together:

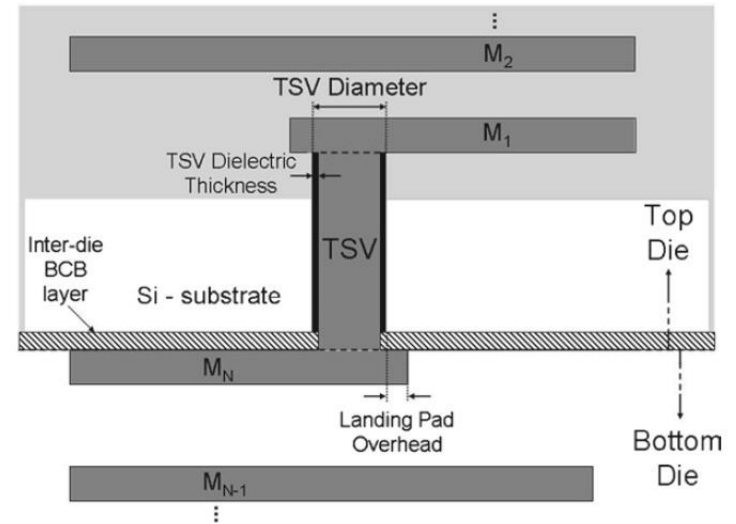


Existing wafer level assembly processes: Through Silicon Vias

- And using the TSV (Through Silicon Via), the assembly houses can assemble dice on top of each other at wafer level.



Through-silicon via providing electrical links among multiple vertically stacked die



Cross-section of a TSV

=> We are not today at production level but at prototyping level. The assembly yields are not controlled quite yet.

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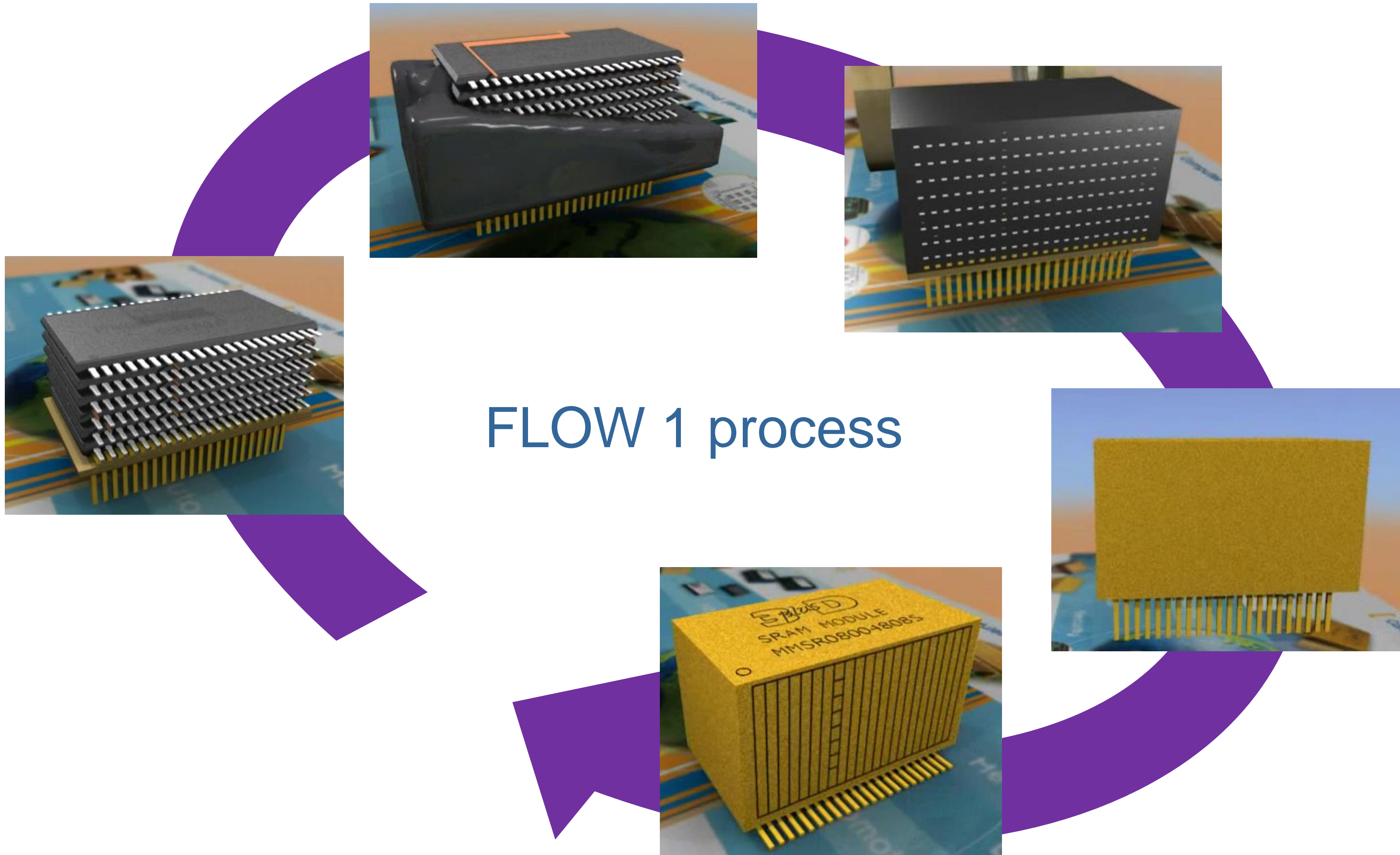
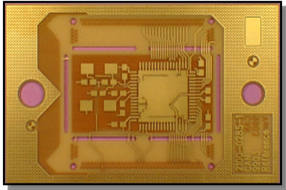
3D PLUS existing process: Flow 1



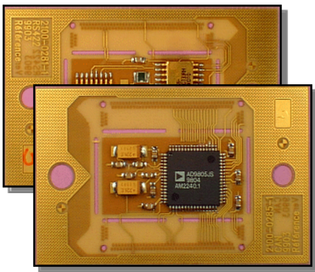
It was introduced 20 years ago for high reliability applications (military and space).

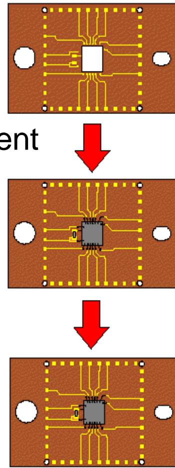
3D PLUS existing process: Flow 2

1) - Flex Design



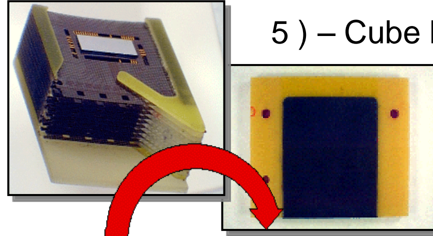
2) – Components attachment



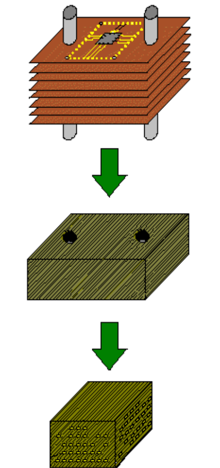


3) - Circuit Test & Screening

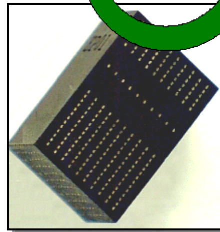
4) – Layers Stacking



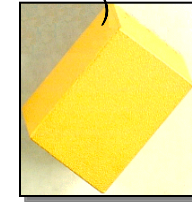
5) – Cube Molding

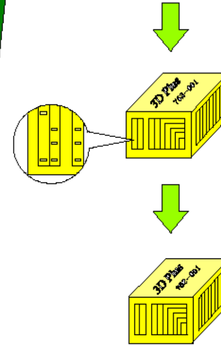


6) – Cube Sawing

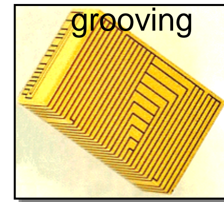


7) – Cube Plating (Ni + Au)

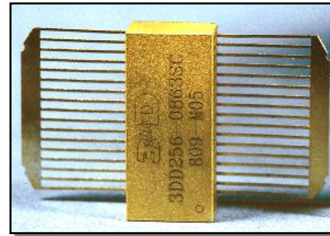




8) – Circuit interconnection by laser grooving



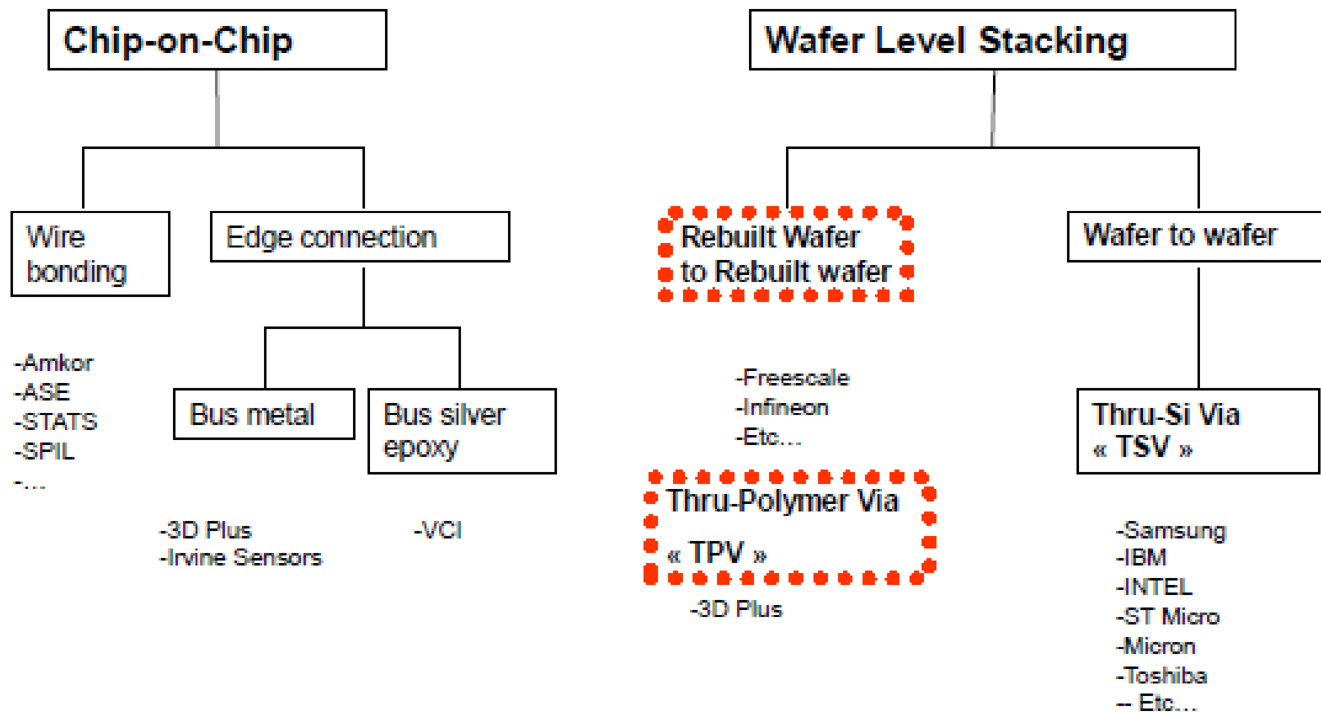
9) – Cube Test & Screening



Same "heritage" than flow 1!

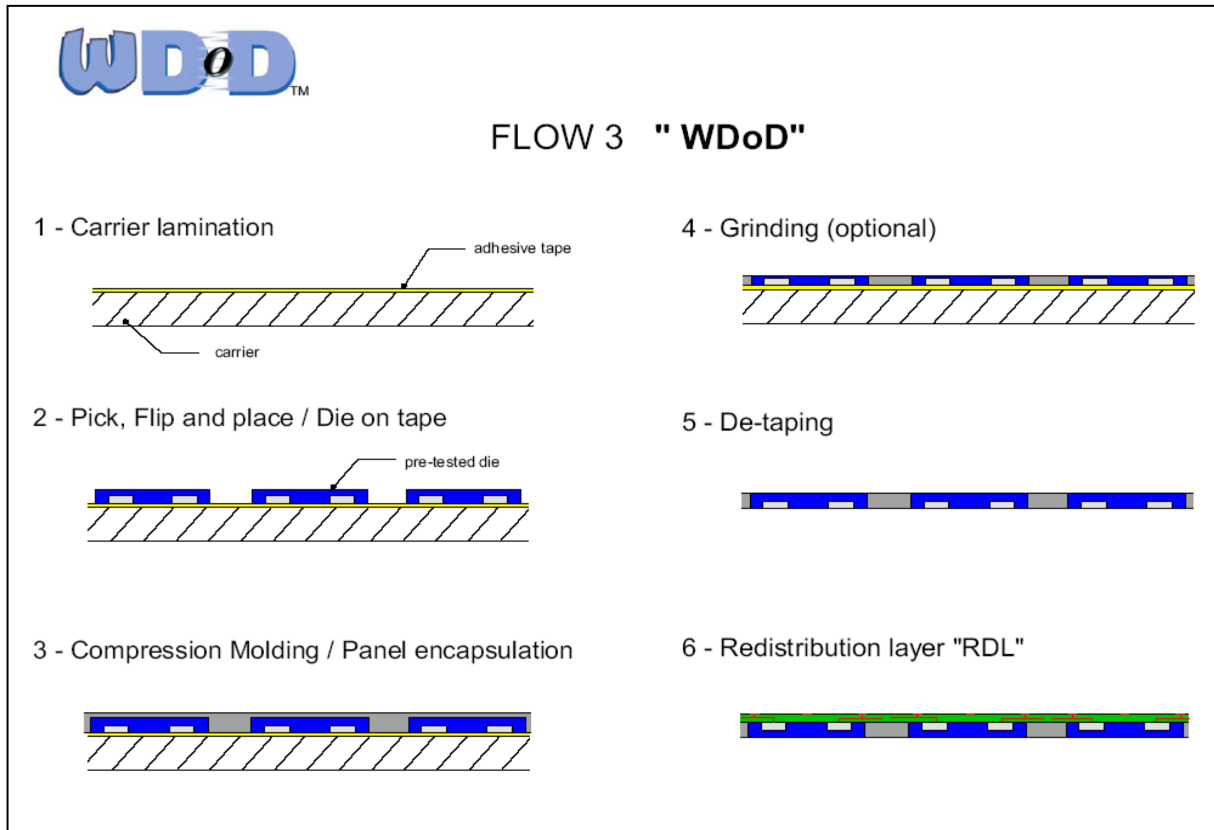
New WDoD™ process: Flow 3 (1/5)

- Based on its long history and strong background in 3 dimensions packaging, 3D PLUS developed a new wafer level assembly process: WDoD® or “wire free” die on die.



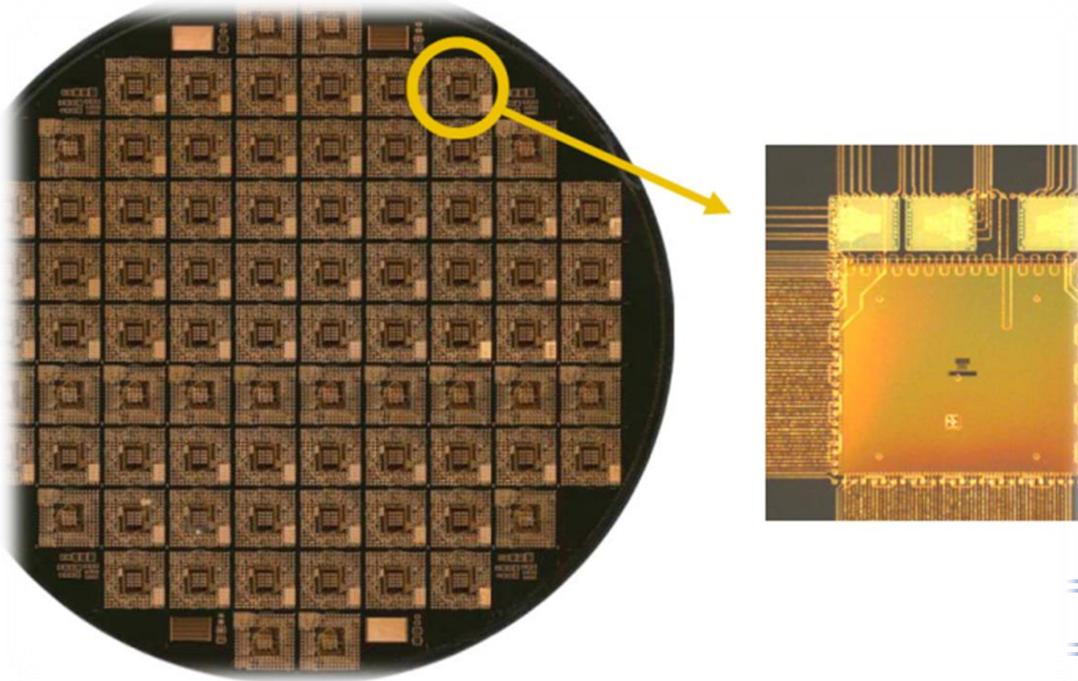
New WDoD™ process: Flow 3 (2/5)

- We are not starting from wafers but from "rebuilt" wafers:



New WDoD™ process: Flow 3 (3/5)

- We re-build a 100% good wafer based on tested "known good dice":



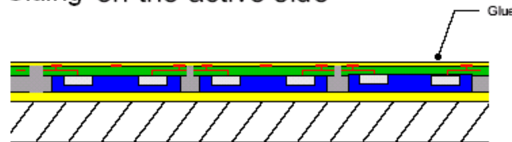
=> No wire bonds nor bumps
=> Single chip or multi chip
=> Passive, antennas, MEMs
=> Ultra low K compatible
=> No package substrate

New WDoD™ process: Flow 3 (4/5)

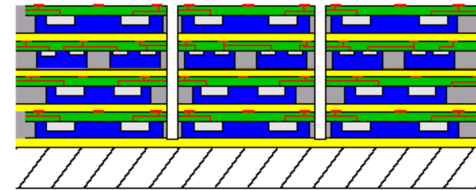
- Then we stack the re-built wafers and create TPVs (Through Polymer Vias) to connect the layers together.

FLOW 3 **" WDoD"**

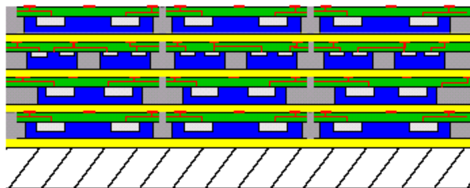
7 - Gluing on the active side



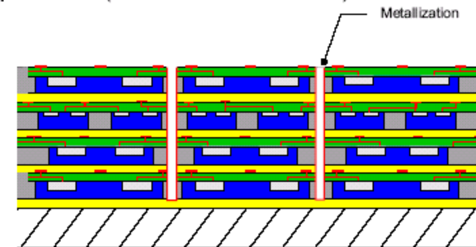
9 - Dicing of the rebuilt and stacked wafers



8 - Stacking of the "Known Good Rebuilt Wafer"

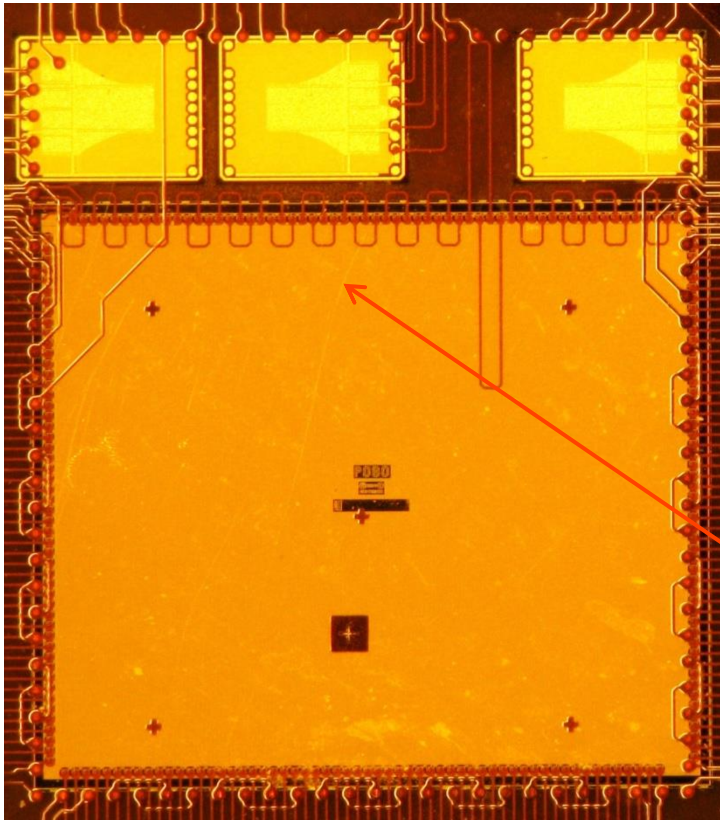


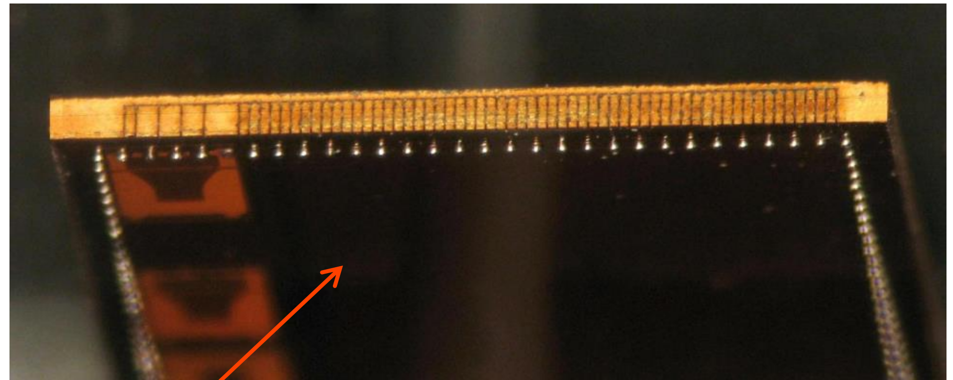
10 - Dicing street edges plating parallel process (electroless Ni + Au)

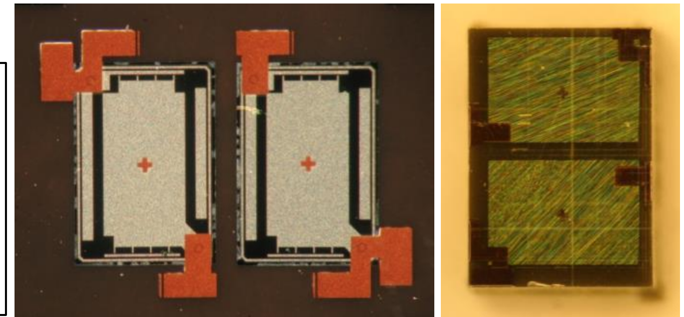


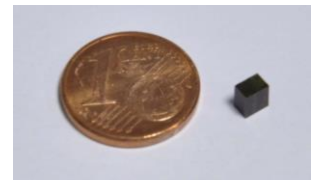
New WDoD™ process: Flow 3 (5/5)

- The process allows to stack up to 10 levels per millimeter. Examples:









Multi-dice stacks: a possibility for uSSDs.

Capacitors stacks

Comparison of processes

	PoP	WAFER LEVEL PACKAGE	
		Wafer to Wafer with TSV	Rebuilt Wafer to Rebuilt Wafer without TSV (WDoD™)
Stacking of different size of the die			
More than 1 Die/Level			
Sourcing flexibility			
Test and / or burned-in before stacking			
Package size			
Package height			
Cost			

Best

Good

OK

Poor

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Conclusion

With this new process offering an advanced level of integration 3D PLUS, targets the following markets:

- High end Industrial and Military,
- Medical (implantable devices).
- All higher volumes applications where RELIABILITY and high level of INTEGRATION are key.

=> We'll be happy to answer all your questions!

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Today's Technology for Tomorrow's Electronics

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