Bright Side Analytics

NAND-Flash
2D to 3D Transition

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3D Flash - Geometry

- Retrograde Geometry at Introduction
  - 2D X/Y geometry nearly constant below 19 nm
    - Concentration is on “Z” layering (cost effectiveness)
    - Implication: Limited number of 2D shrinks
  - Larger geometry required for:
    - Reliability
    - Durability
    - Yield
- Increasing the number of layers
  - The new shrink?
  - Price-per-bit slope change?

3D Flash - Process Technology

- Device physics well known
- Nearest neighbor disturb
  - Still a problem
- SiO3 Floating Gate to SiN Charge Trap
  - High Program/Erase voltage still required
  - Silicon Nitride lithography difficult under 20 nm
- Vender specific device characteristics
- 2D geometry to layer number optimization
- IP ownership arrangements
  - Remain a challenge

3D Flash - Economics

- Oligopolization effects
  - Stable pricing
  - Complacent competitive environment
  - Vendor specific device and services
- Business Cycle
- Fab Stall
  - 450 mm Wafer Fab push out [2018?]
  - EUV push out [2016?]
- Maintain 300 mm wafer and Flash process infrastructure
- Vertical integration of controller & firmware
- “Cost Effectiveness” situation

3D Flash - Roadmap Challenges

- Roadmap laundry list
  - “Cost Effectiveness” ?
  - SLC now, MLC, TLC later?
  - Redundancy requirements?
  - Flash subsystem cost escalation?
  - Voltage scaling?
  - Power?
- Marginal system level performance gain
- “Cost Effectiveness” situation
- Next generation technology ~~on the horizon~~ ready

Non-Volatile - Next Gen

- Only one type will reach commodity status
  - STT, MRAM, RRAM & PCM candidates
- Law of commodity memory:

  "Price is always the determining factor"

- Favored candidate: Resistive RAM [RRAM]
  - Adesto (discrete), Panasonic (SoC) in production
  - Altis Semiconductor sampling (Adesto SoC)
  - Crossbar (SoC) demonstrator
  - Micron, SK Hynix, SanDisk, Toshiba & Rambus in development

Resistive RAM - Roadmap Feature Set

- Standard CMOS fab process
- BEOL “bolt on/over” SoC
- Both voltage & geometry scaling below 10 nm
- 0.5X smaller cell than NAND
- 10X endurance over NAND
- Read/Write symmetry & Byte Write
- 20X greater write performance than NAND
- 20X lower power than NAND
- Radiation resistant
- Cost effective
- IP dates to ~1990
- long term roadmap

Summary

- 3D NAND will ramp through 2015
  - “Cost Effectiveness” requires market validation
  - No real performance deltas
- Resistive RAM introductions create a competitive market race for dominance
  - Incumbent producers set on 3D NAND production prior to resistive RAM launch
  - Defection of a single producer will change everything…,