Mixed Ionic Electronic Conduction (MIEC) based Access Devices for 3-D Crosspoint Memory

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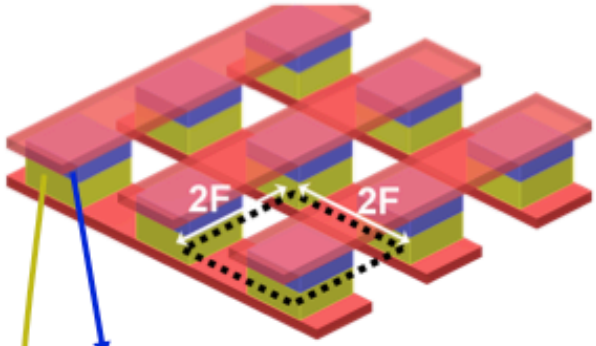
Outline

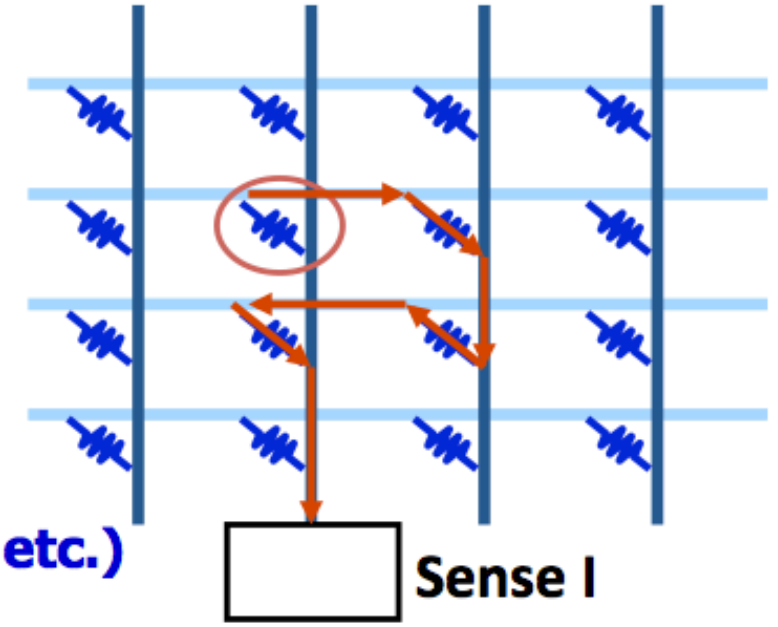
- Motivation
- MIEC access device characteristics
  - DC IVs and pulse currents
  - Large array yield and variability
  - Thickness and CD scaling
- Crosspoint roles of an access device (AD)
  - Long term leakage of un-selected and half-selected states
  - Write operations and recovery to low leakage
  - Read operations
- Conclusions

Need for an Access Device



Memory Element (PCM, RRAM etc.)

Access Device (Selector)

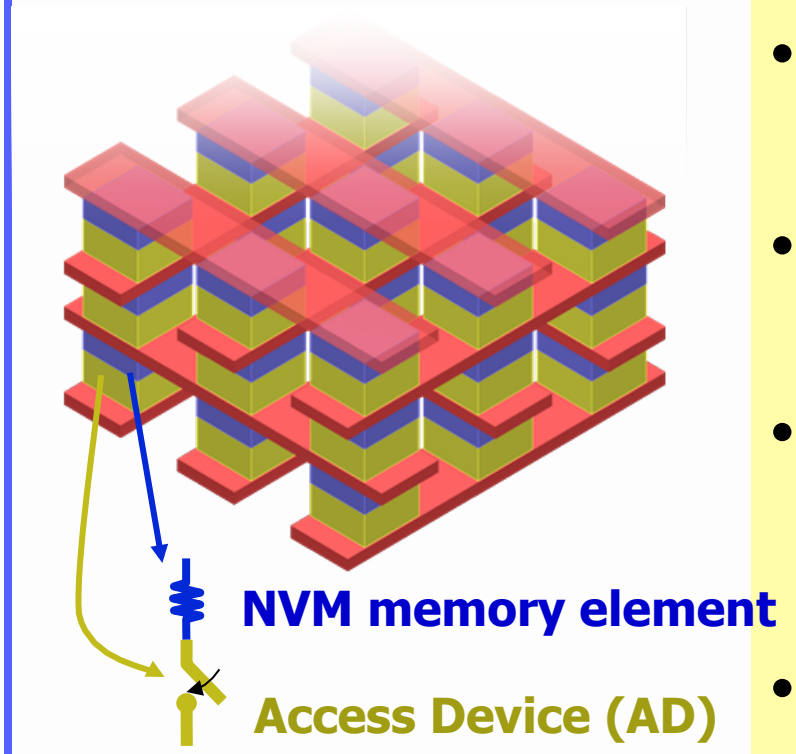


Current 'sneak path' problem

Access device needed in series with memory element

- Cut off current 'sneak paths'
  that lead to incorrect sensing and wasted power
- Typically diodes used as access devices
- Could also use devices with highly non-linear I-V curves

Access Device for 3D Crosspoint Memory



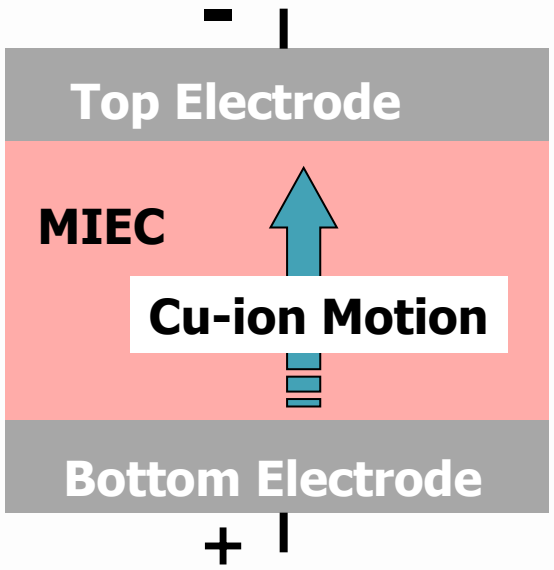
Basic Requirements

- **High ON-state current density**
  > 10 MA/cm² for PCM RESET
- **Low OFF-state leakage**
  ON/OFF ratio **> 10^7** for large arrays
- **BEOL-compatibility**
  < 400 ˚C processing for 3D memory with multi-layer stacking
- **Bipolar operation** (required for robust RRAM)
  → not possible with conventional diodes

MIEC-based Access Devices satisfy all 4 criteria

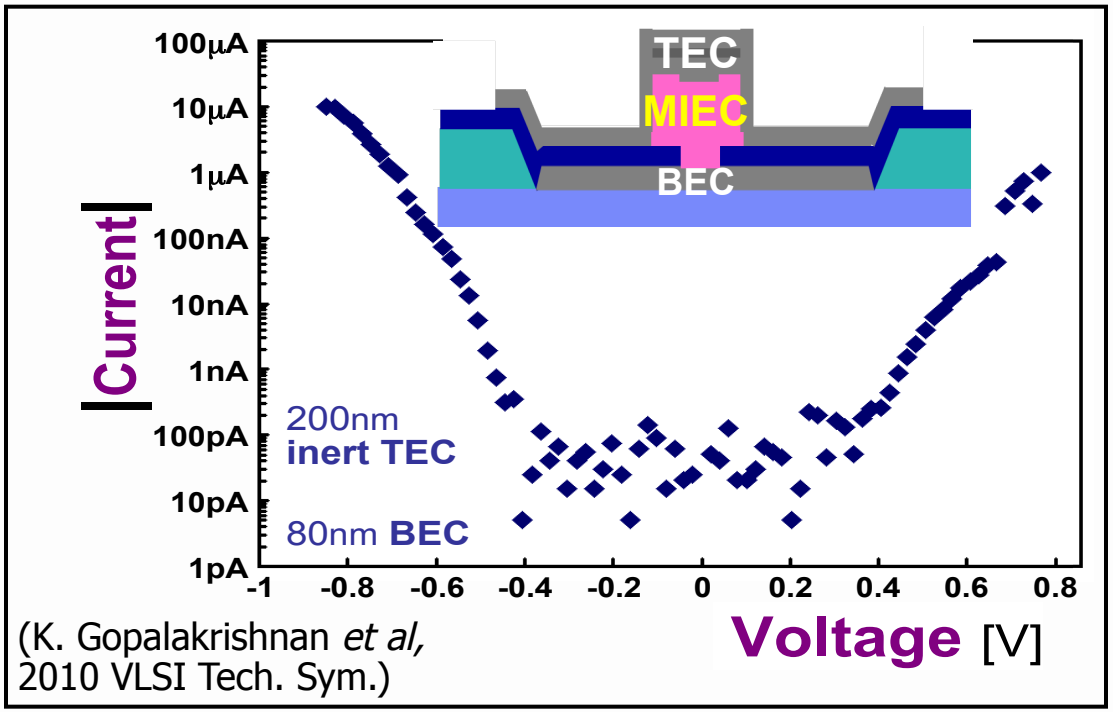
→ ADs that could enable 3D for any low voltage NVM

MIEC Device Operation



Cu-containing MIEC (Mixed-Ionic-Electronic-Conductor*)

- Mobile Cu-ions → transport in E-field
- Cu interstitials/vacancies can act as dopants and **modulate**
  - **local electron/hole concentration,**
  - **Schottky barriers at interfaces,** etc.



(K. Gopalakrishnan *et al*, 2010 VLSI Tech. Sym.)

Applied voltage leads to **Transient Cu-ion drift,** followed by Steady-state **electron/hole current**

(Gopalakrishnan *et al*, 2010 VLSI Tech. Sym.)

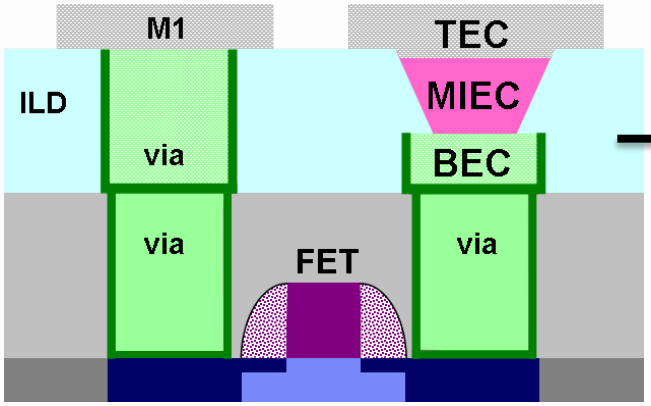
*See I. Riess, *Solid State Ionics*, 157, 1 (2003) for MIEC models.

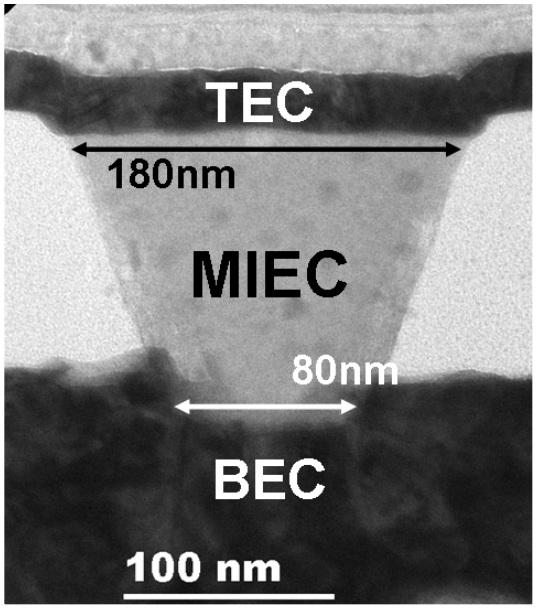
MIEC Access Device Fabrication

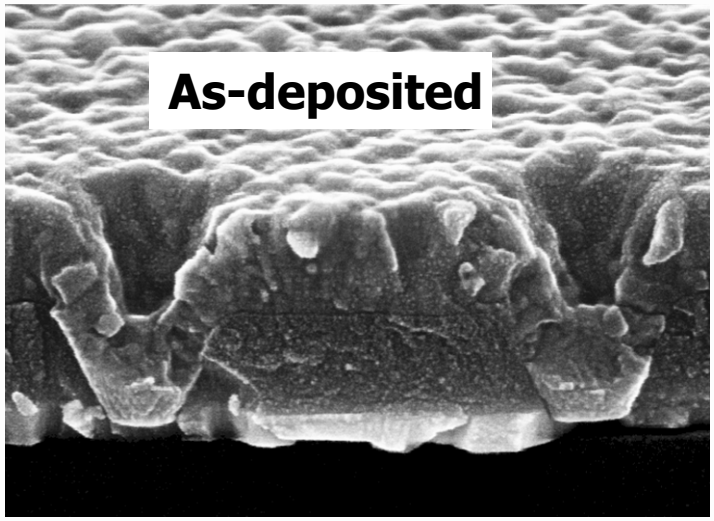
180 nm CMOS Front-End

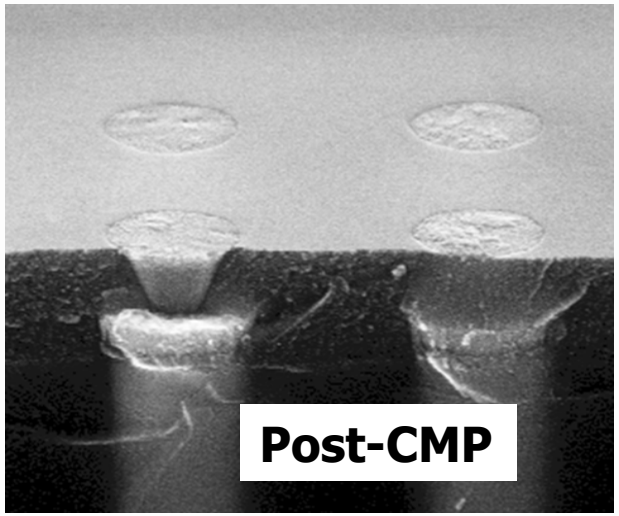
→ 1T1S

(1 transistor + 1 selector)







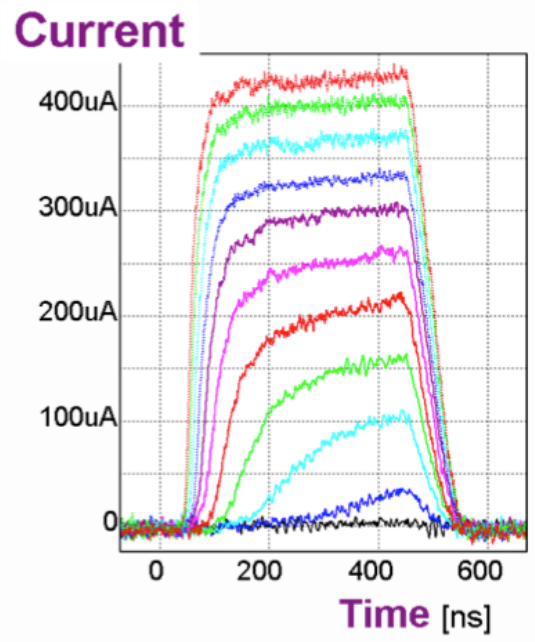


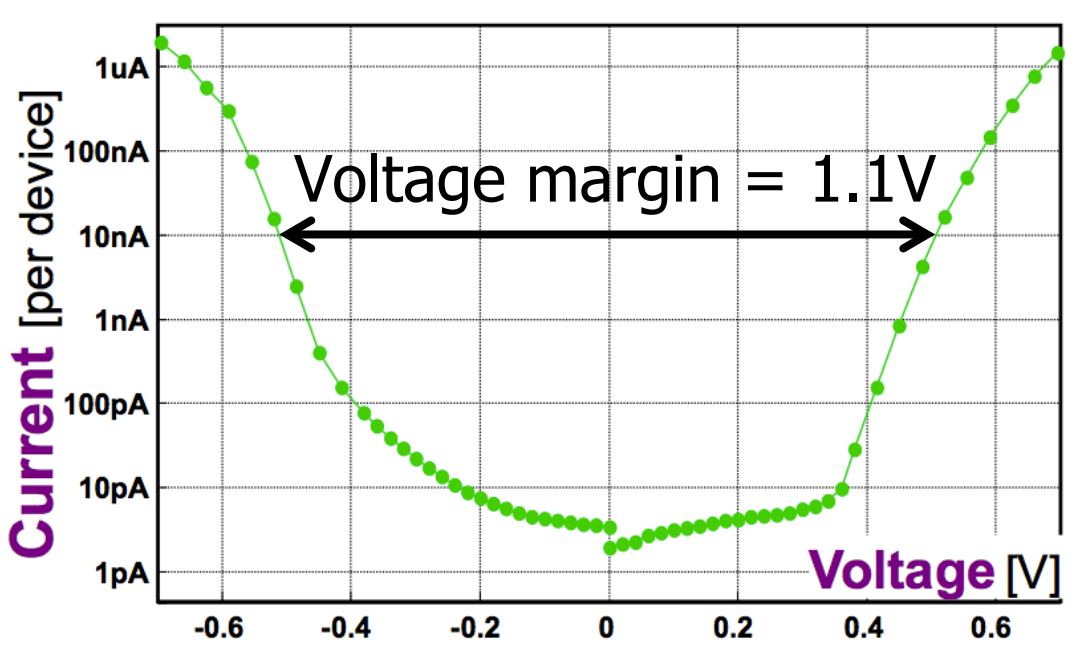
CMP process for MIEC material with modified commercial Cu slurry →

self-aligned MIEC diode-in-Via (DIV) in 200 mm wafer process

(Shenoy *et al*, 2011 VLSI Tech. Sym.)

MIEC Device Performance

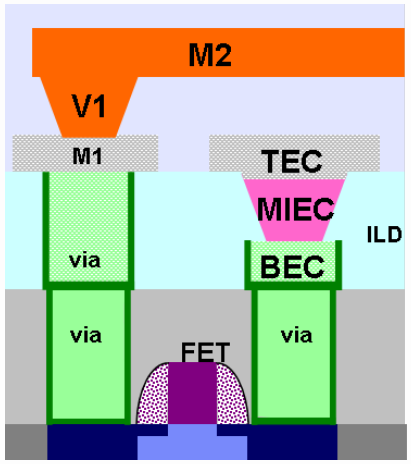


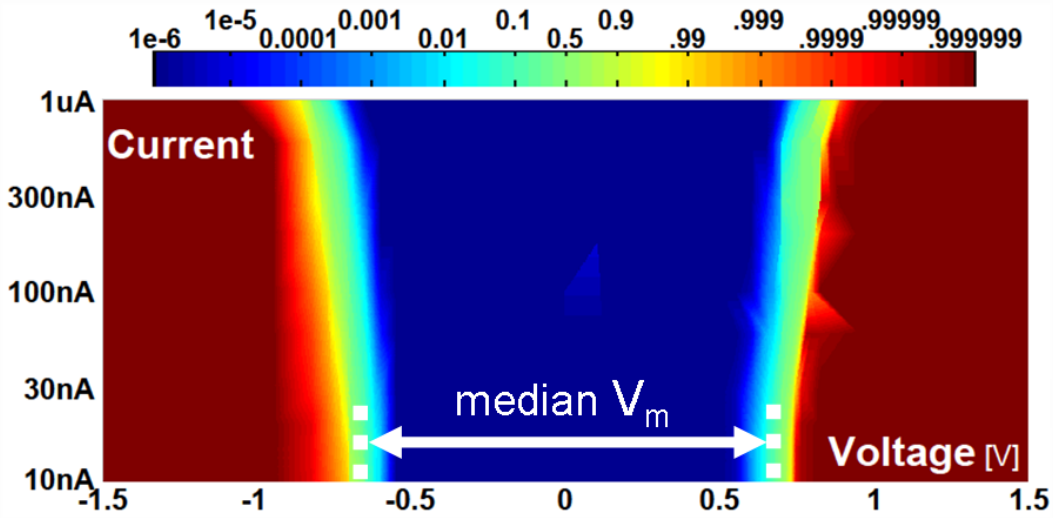


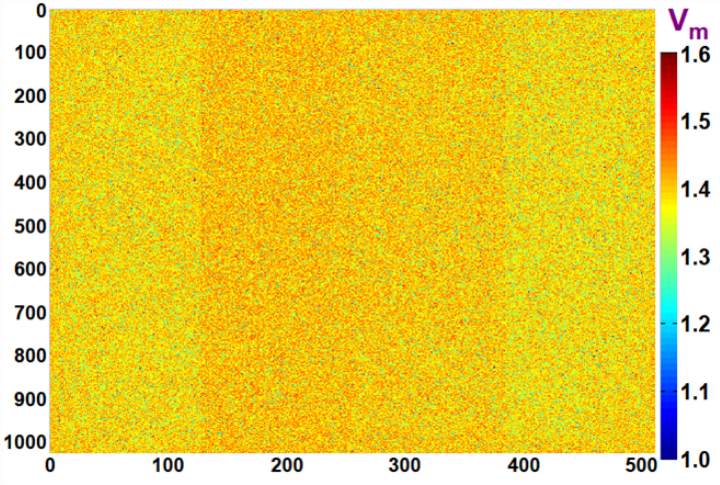
- Low **(< 10pA) OFF state leakage** currents near 0V bias
- High **(> 400µA) ON state currents** → current density > 15MA/cm^2
- **> 10^7 ON / OFF** ratio
- Wide (0.8V) window with low current (<100pA)
- **Endurance > 10^8 cycles** @ **~100µA** currents

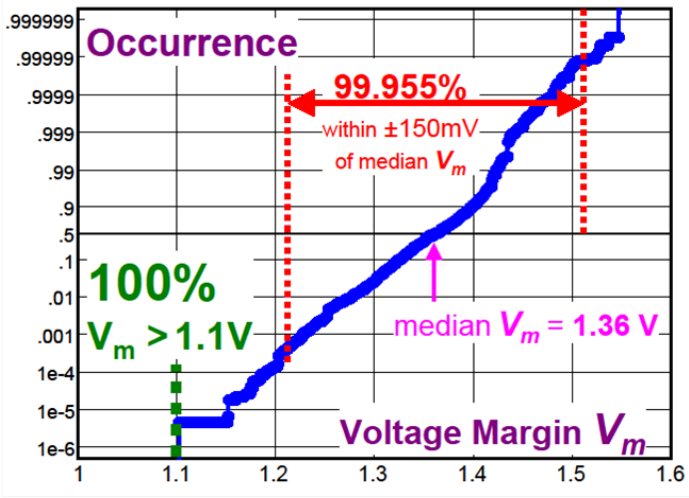
(Shenoy *et al*, 2011 VLSI Tech. Sym.)

MIEC Yield & Variability





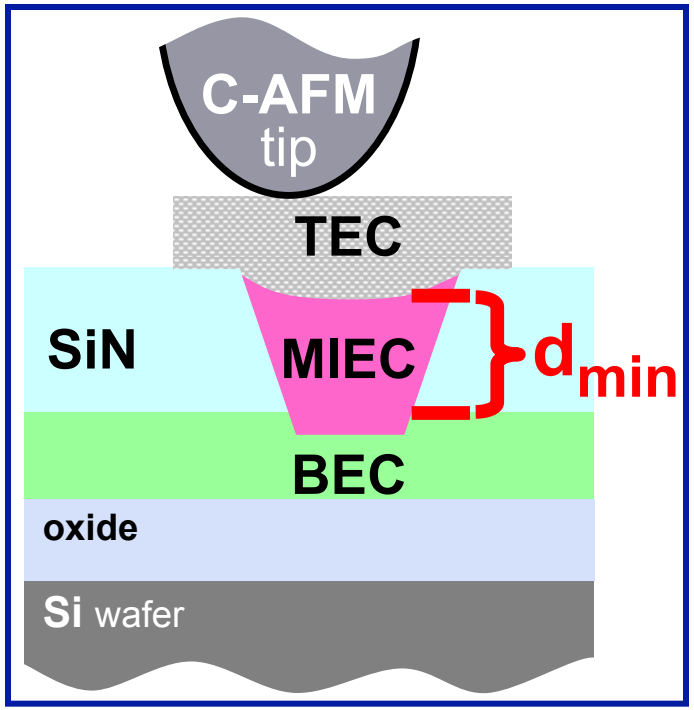




- **100% yield** and **tight distributions** in 512 kbit 1T-1MIEC array

(Burr *et al*, 2012 VLSI Tech. Sym.)

C-AFM Short Loop for MIEC ADs



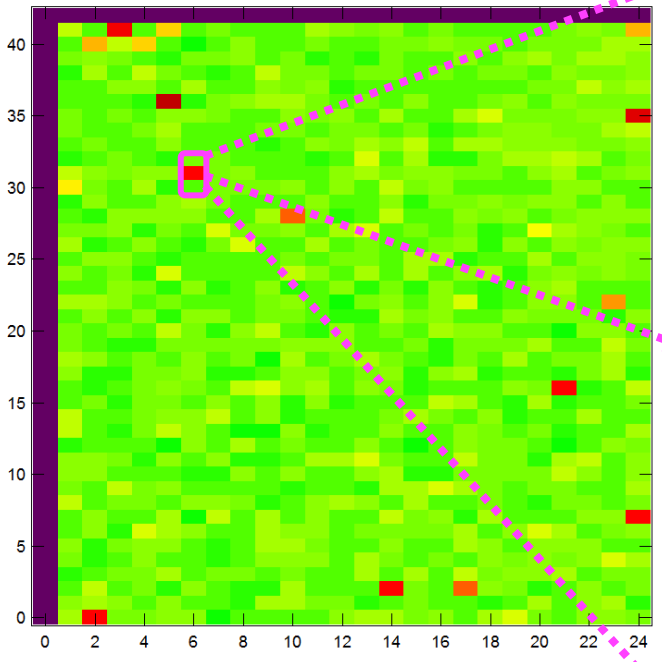
- **Conducting atomic force microscopy**
  with doped diamond and / or solid Pt probes
- Minimal wiring requiring **few lithography steps**
- **Diode-in-via (DIV) structure** the same as transistor arrays

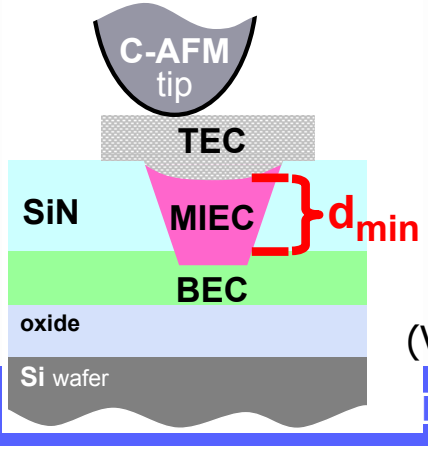
→ Vary SiN_x dielectric thickness for thickness scaling

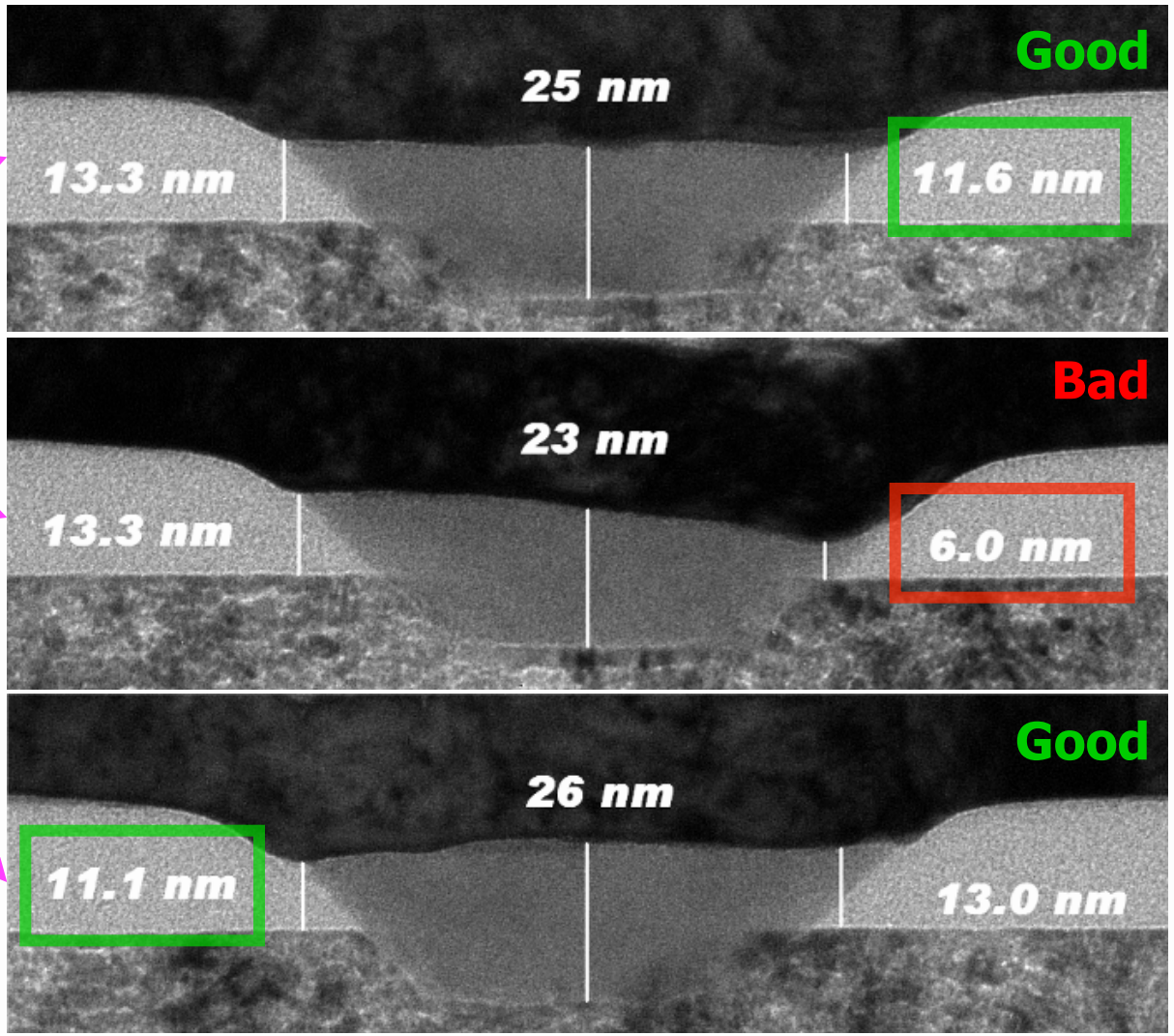
(Virwani *et al*, 2012 IEDM)

Thickness scaling of MIEC ADs

High-yield array of C-AFM short-loop devices



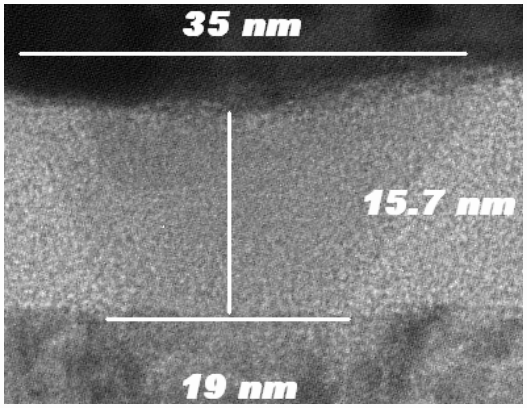


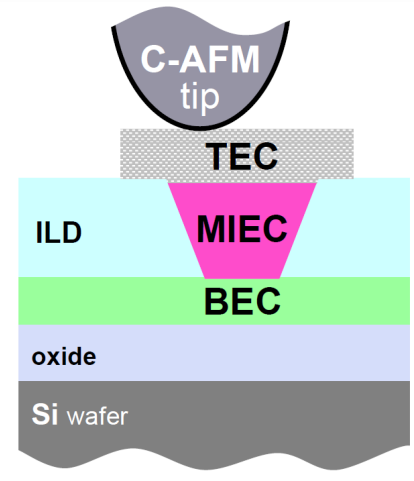


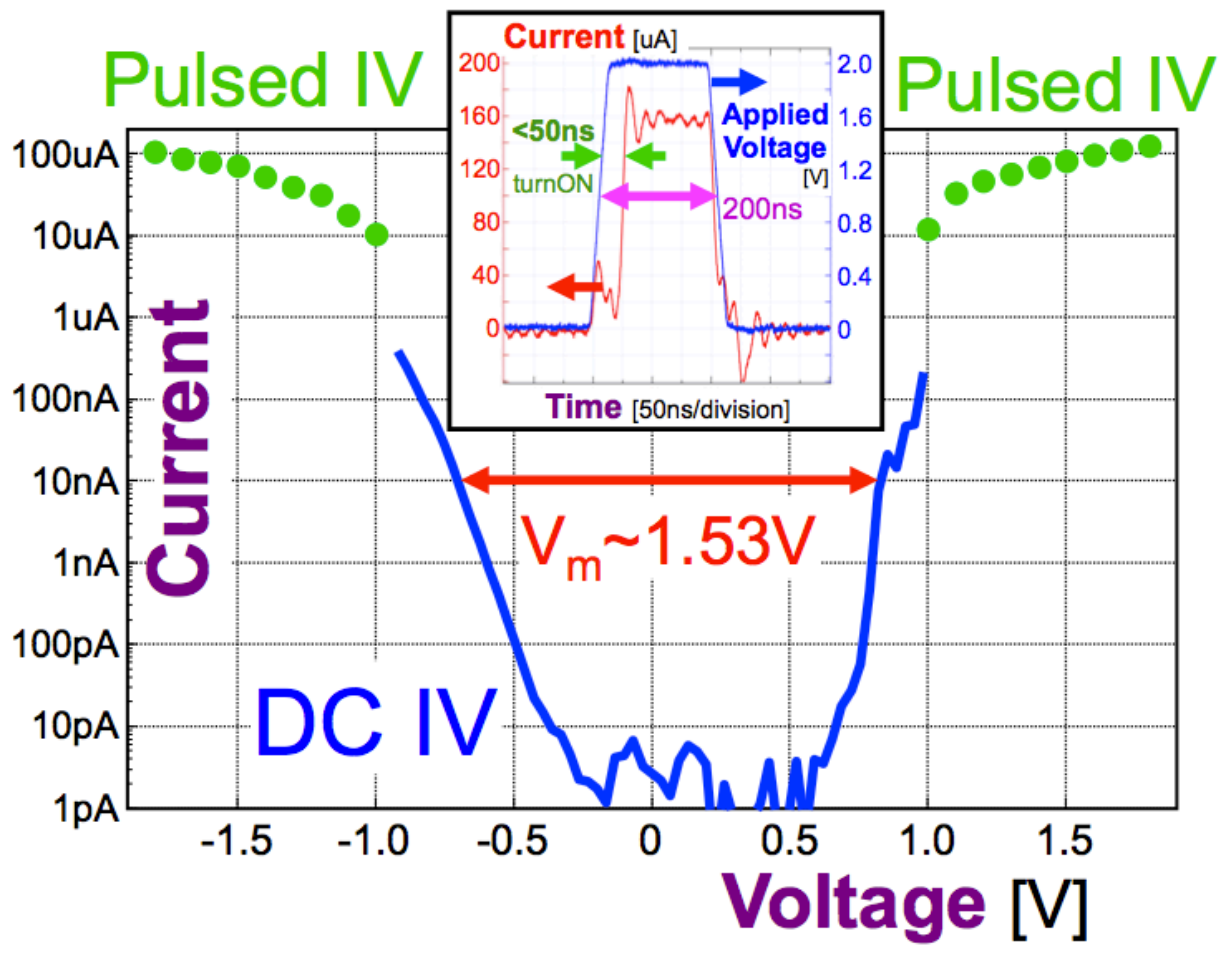
MIEC devices **work well down to 11nm thickness**
(6nm may be too thin)

(Virwani *et al*, 2012 IEDM)

MIEC Access Devices CD Scaling







- **Scaled MIEC** devices also offer **1e7 ON-OFF contrast** and **high speed**
- **Conduct ~150µA** pulse currents
- **CDs <30nm** demonstrated – **no lower CD limit yet identified**

(Virwani *et al*, 2012 IEDM)

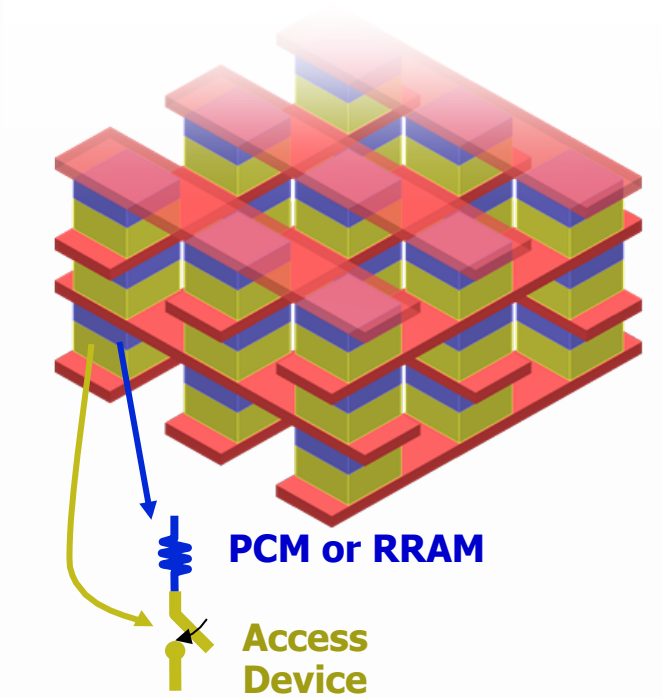
AD requirements for 3D Crosspoint Memory

✓ High ON-state current density
>10 MA/cm^2 for PCM / RRAM RESET

✓ Low OFF-state leakage current
>10^7 ON/OFF ratio, and
wide low-leakage (**< 100pA**) voltage zone to accommodate half-selected cells in large arrays

✓ Back-End process compatible
<400C processing to allow 3D stacking

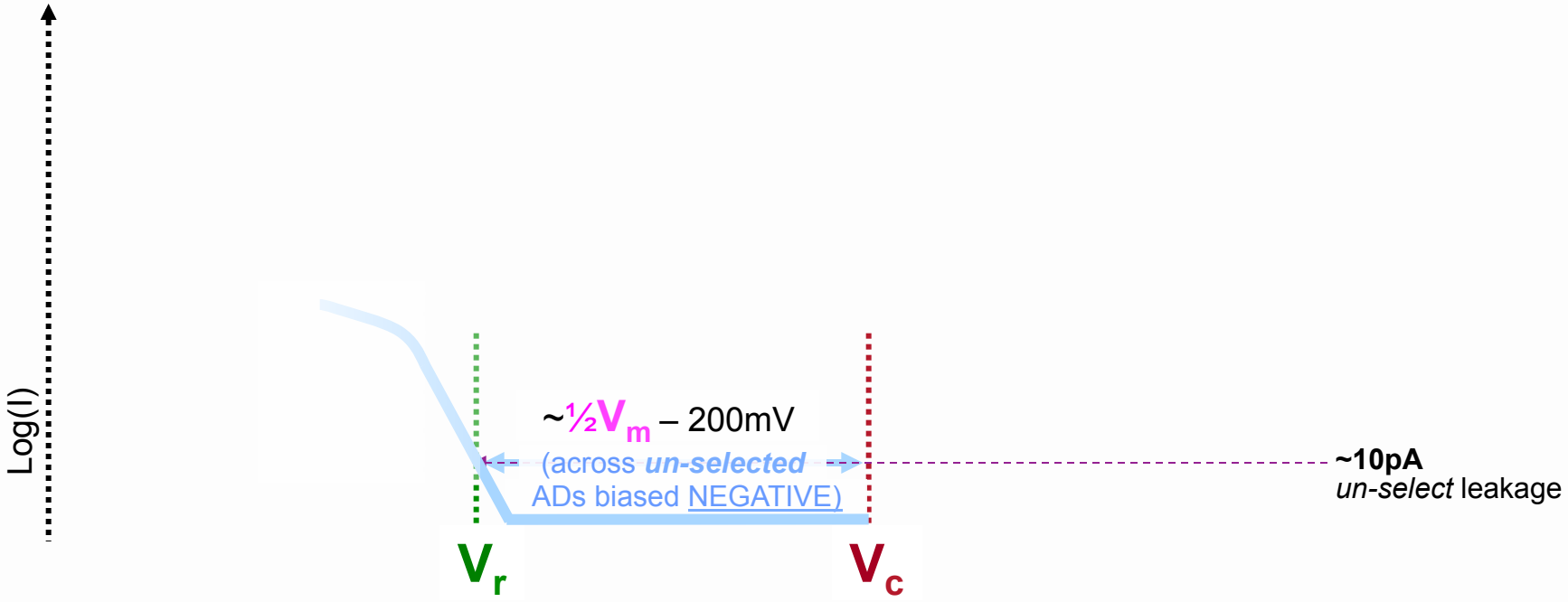
✓ Bipolar operation
needed for optimum RRAM operation

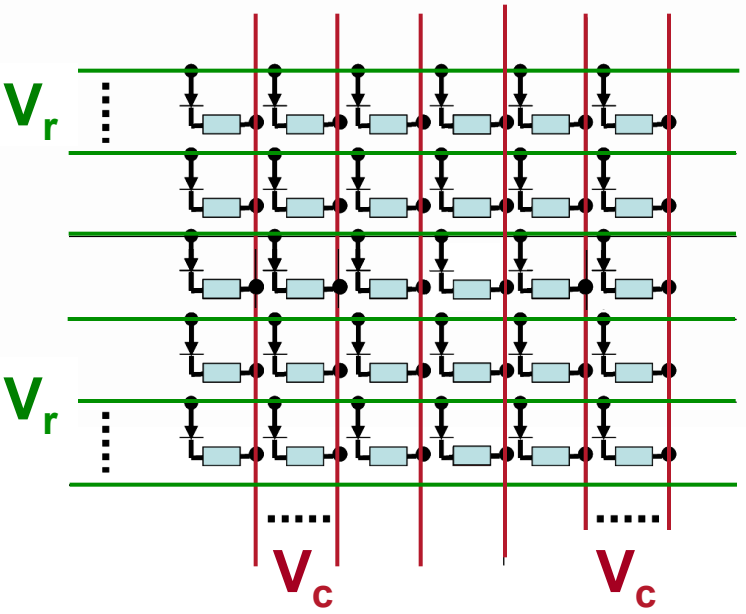


- ✓ variability?
- ✓ yield?
- ✓ scalability?
- ✓ co-integration with NVM?
- ✓ turn-ON speed for write?
- ✓ endurance?
- ✓ manufacturability?

- long-term leakage?
- turn-OFF speed?
- turn-ON speed for read?

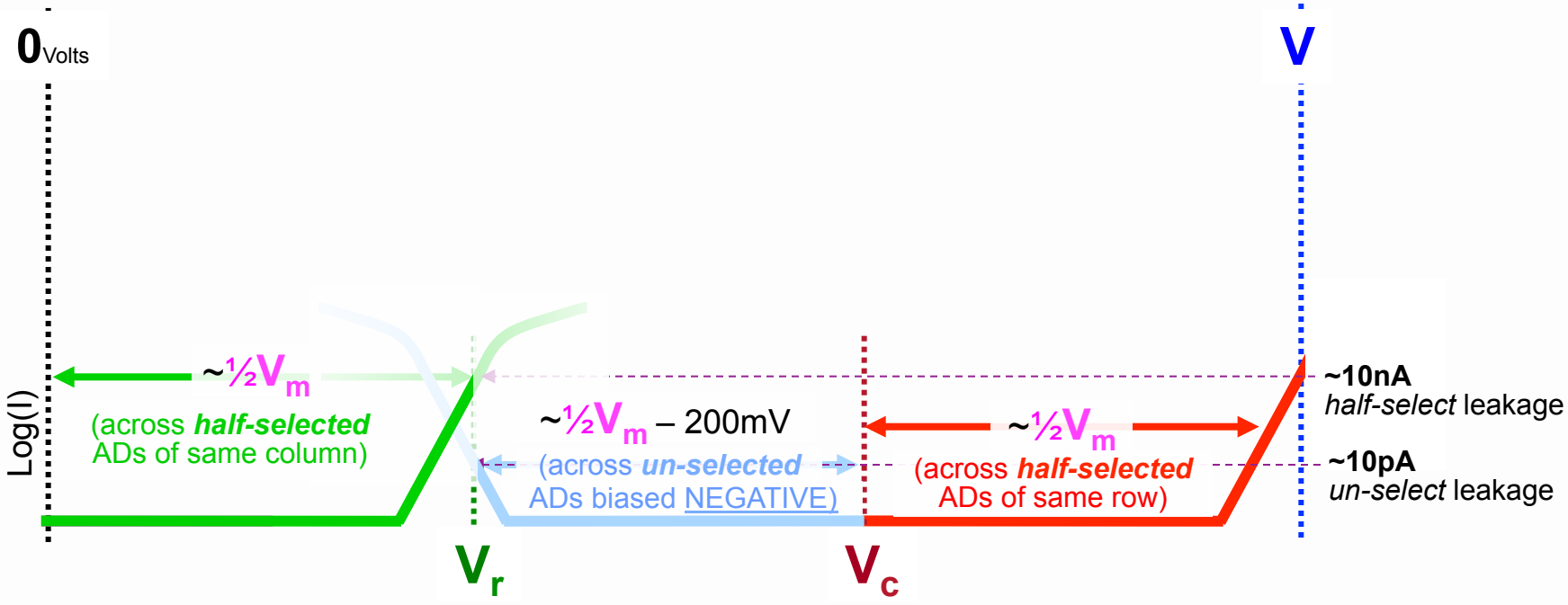
Crosspoint "roles" of the MIEC device

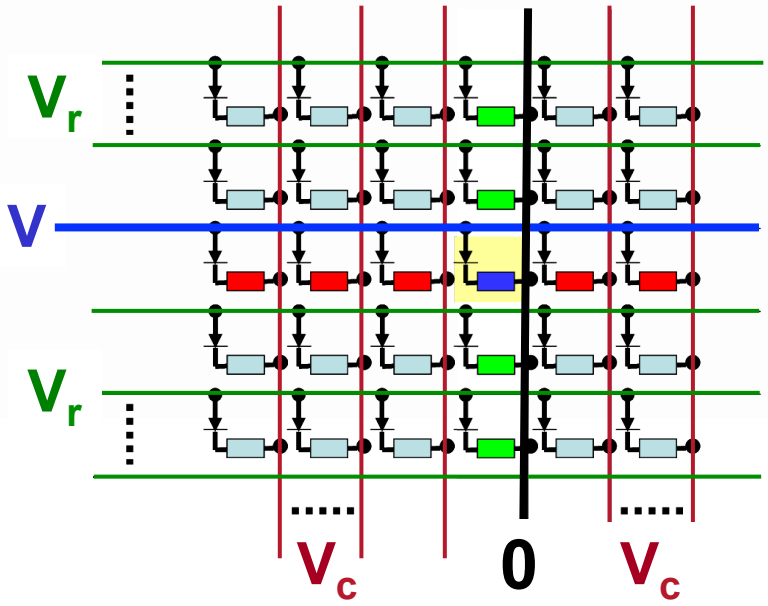




1. ***un-selected* state**
   – shown to be stable over hours

Crosspoint "roles" of the MIEC device

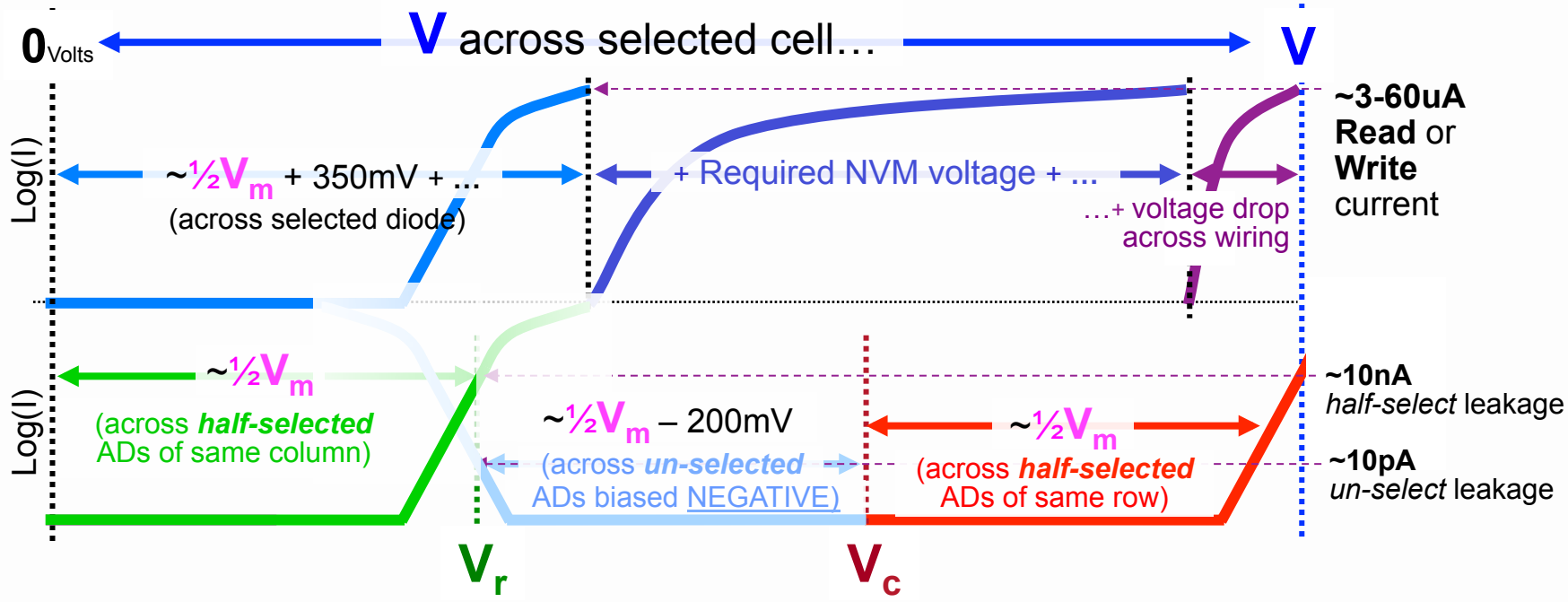


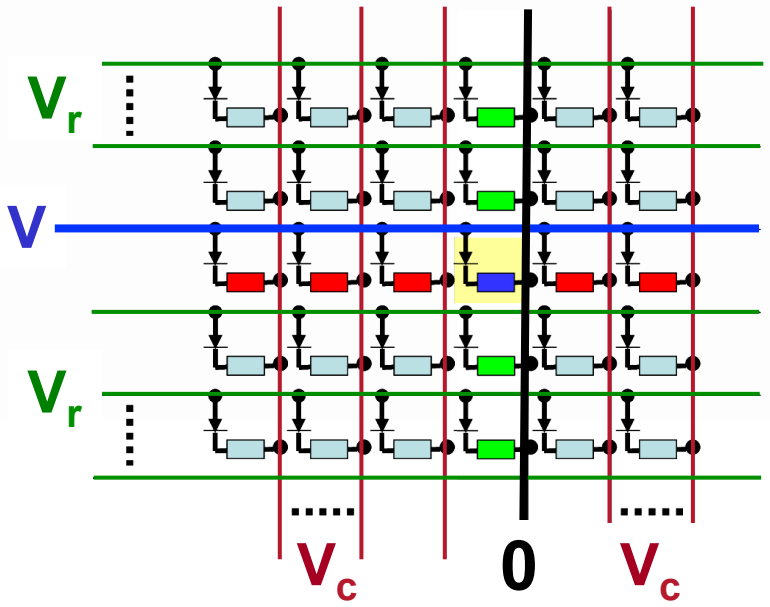


1. ***un-selected* state**
   – must be stable over long periods
2. ***half-selected* states**
   – must be maintained while same **row** (or **column**) is accessed

→ shown to be stable for seconds: **millions** of successive read/writes

Crosspoint "roles" of the MIEC device

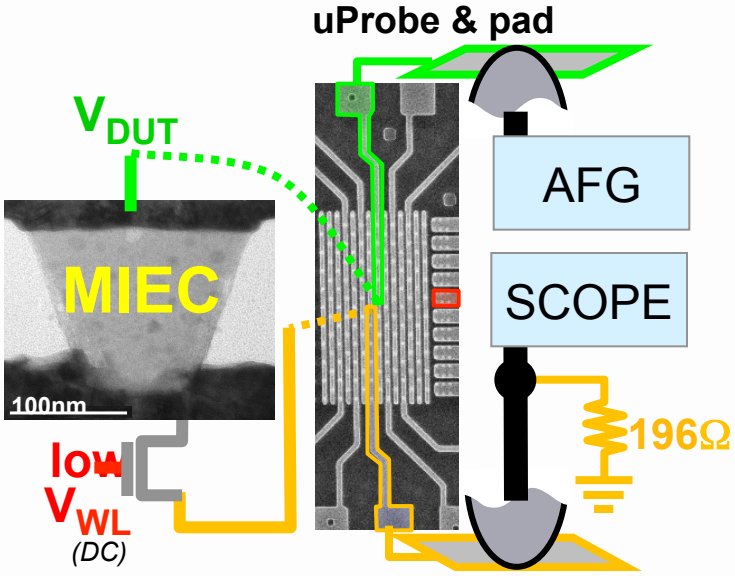


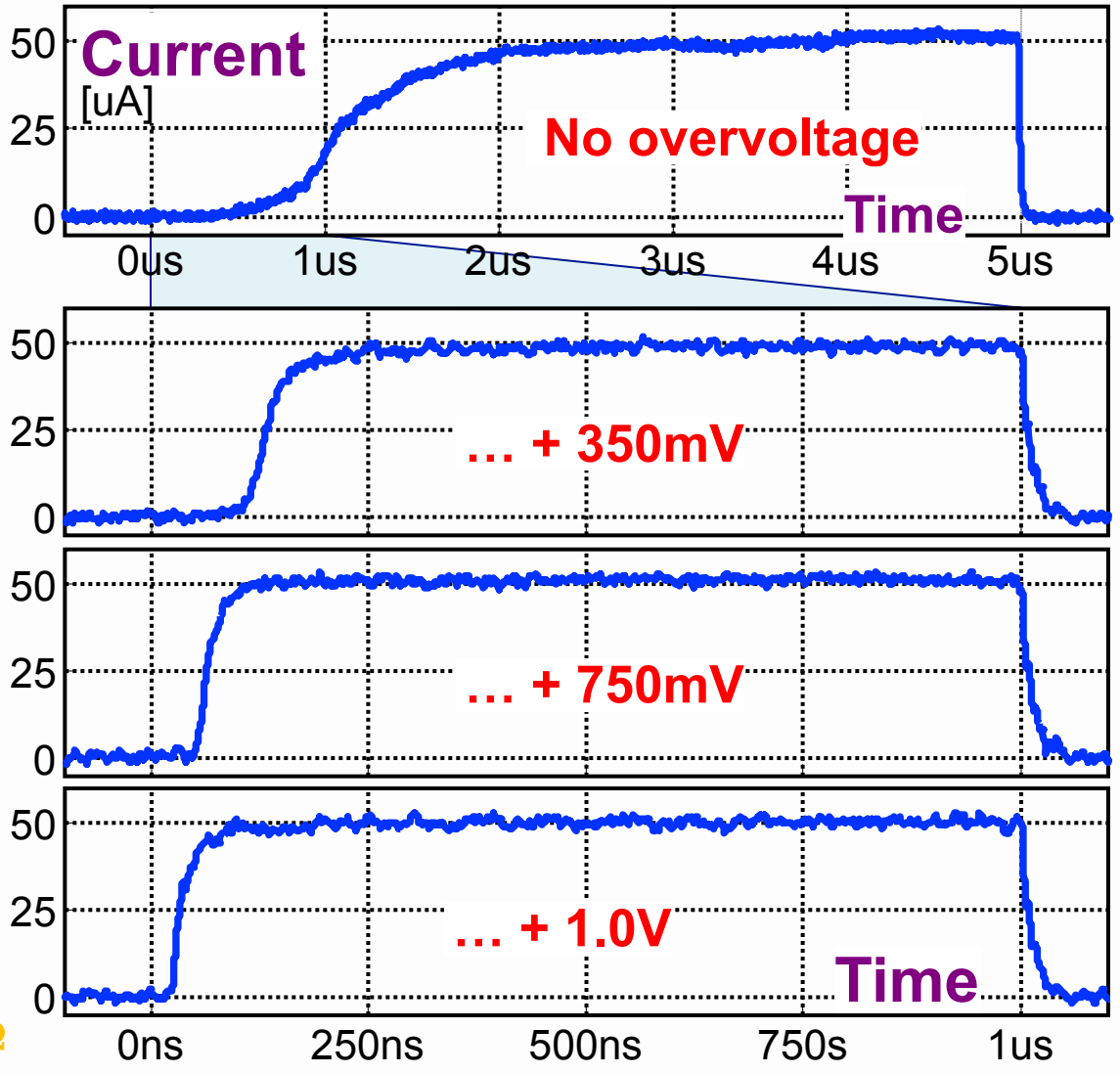


1. ***un-selected* state**
   – must be stable over long periods
2. ***half-selected* states**
   – must be maintained while same **row** (or **column**) is accessed
3. **selected** (for **read** or **write**)
   – must pass desired current quickly then return to low leakage

Write pulses depend on overvoltage

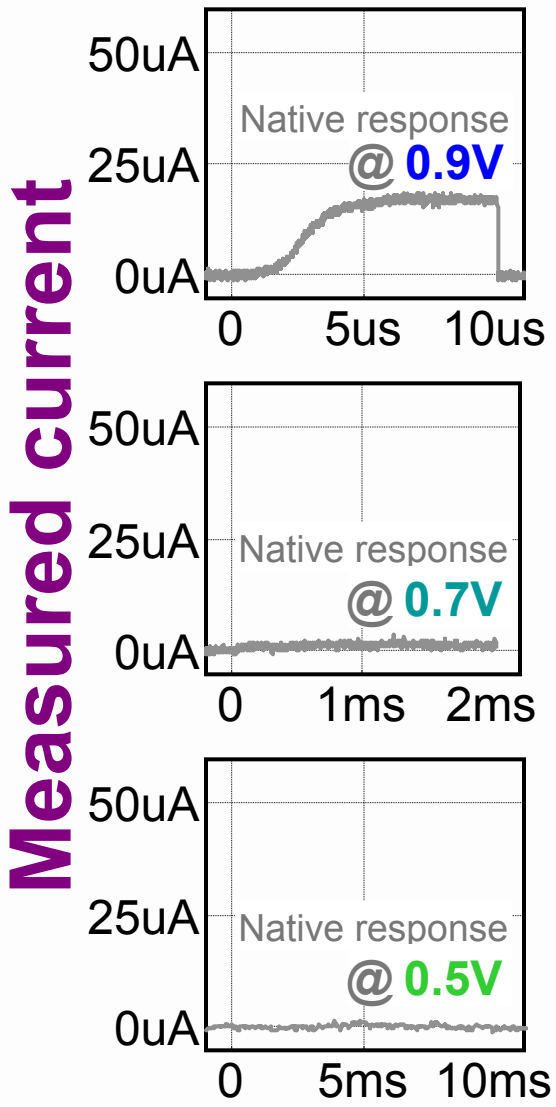
- **Turn-ON delay** (50uA write pulses) can be **greatly reduced** by **overvoltage**





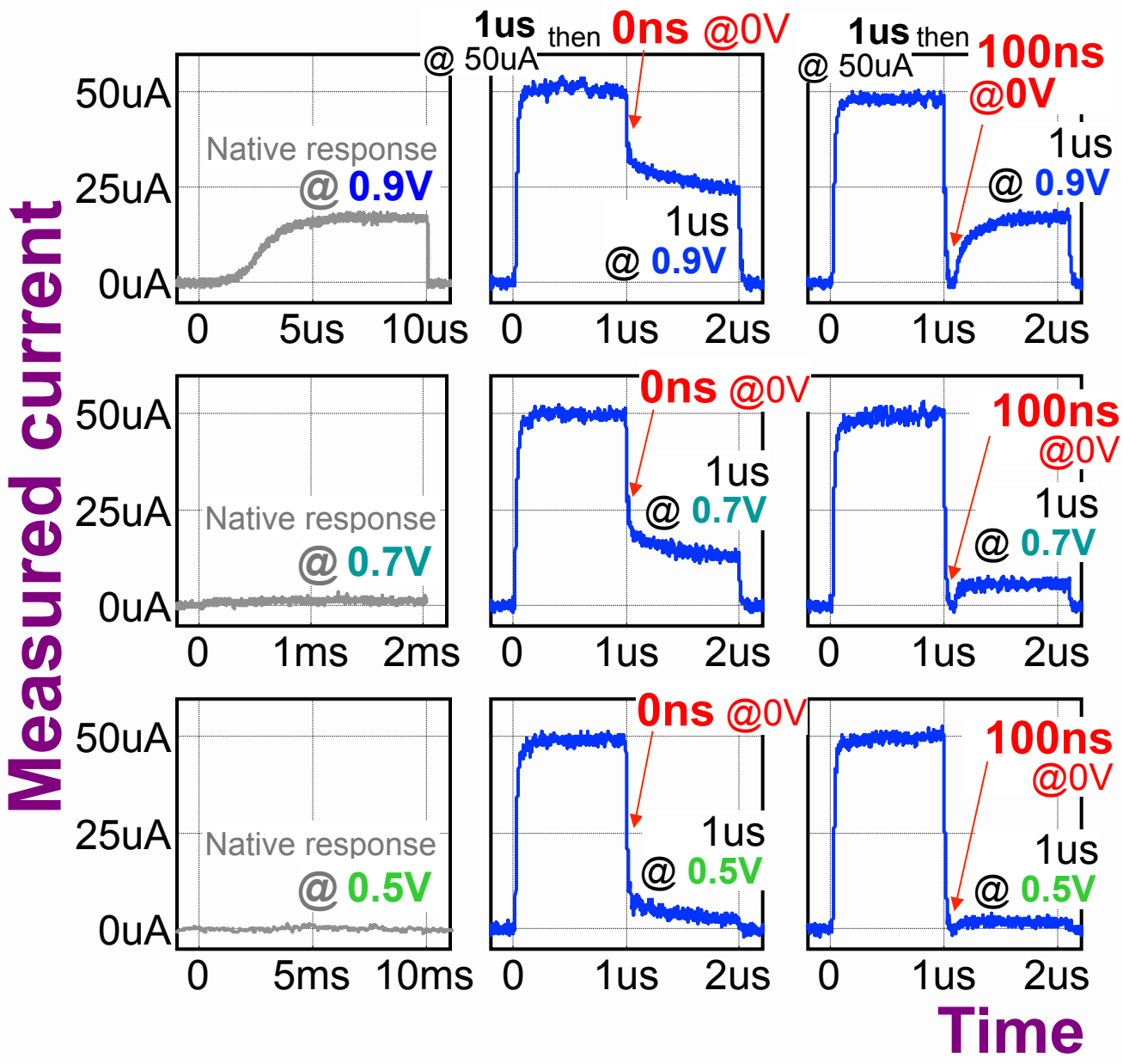
(Burr *et al*, 2013 VLSI Tech. Sym.)

Native response at lower voltages



(Burr *et al*, 2013 VLSI Tech. Sym.)

How fast do devices recover after writes?

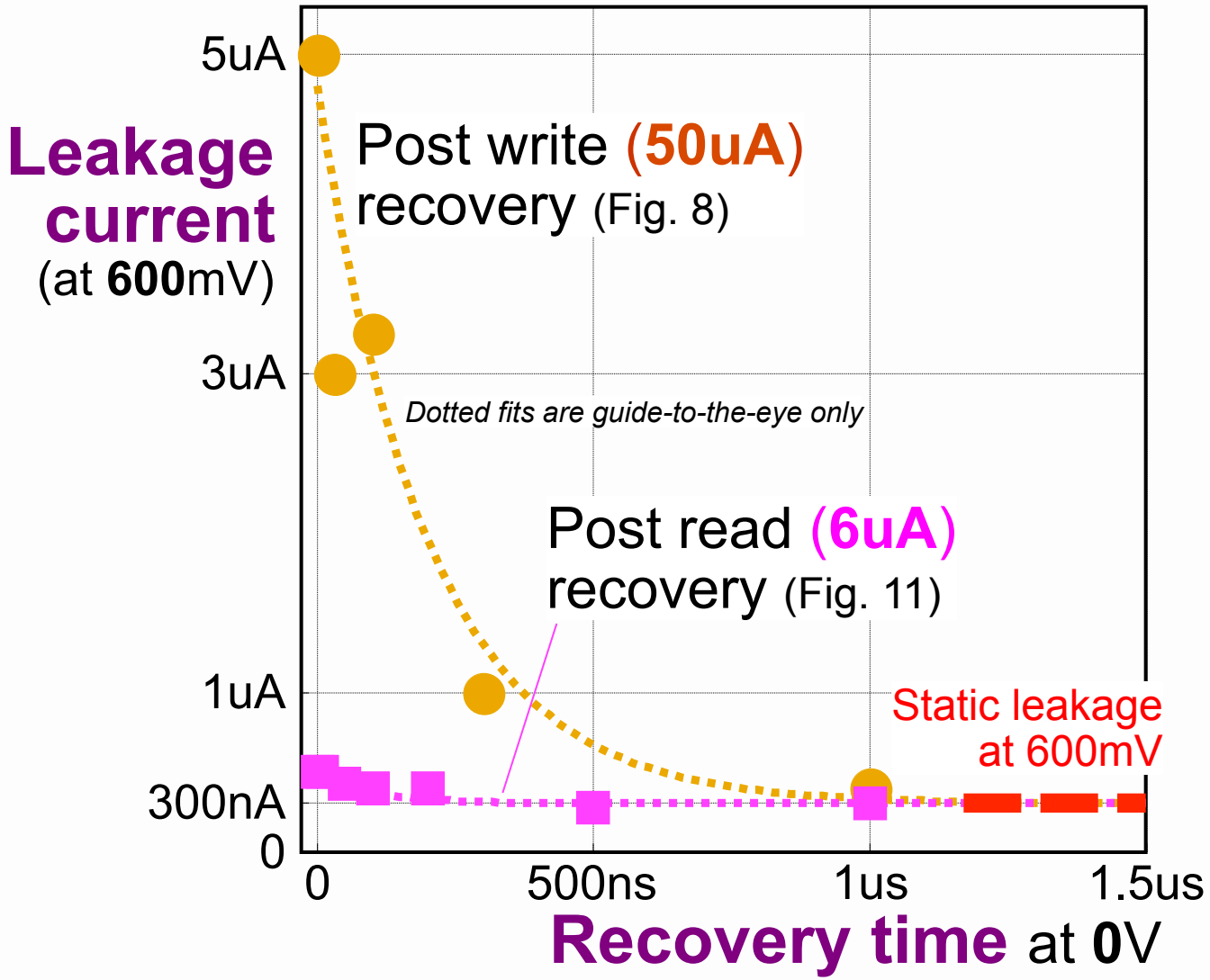


After a strong write pulse (50uA for 1us), MIEC AD response is affected:

- **devices remain ON**
- don't require any overvoltage acceleration to turn back ON
- at lower voltages where leakage should be undetectable, **measurable currents can persist.**

(Burr *et al*, 2013 VLSI Tech. Sym.)

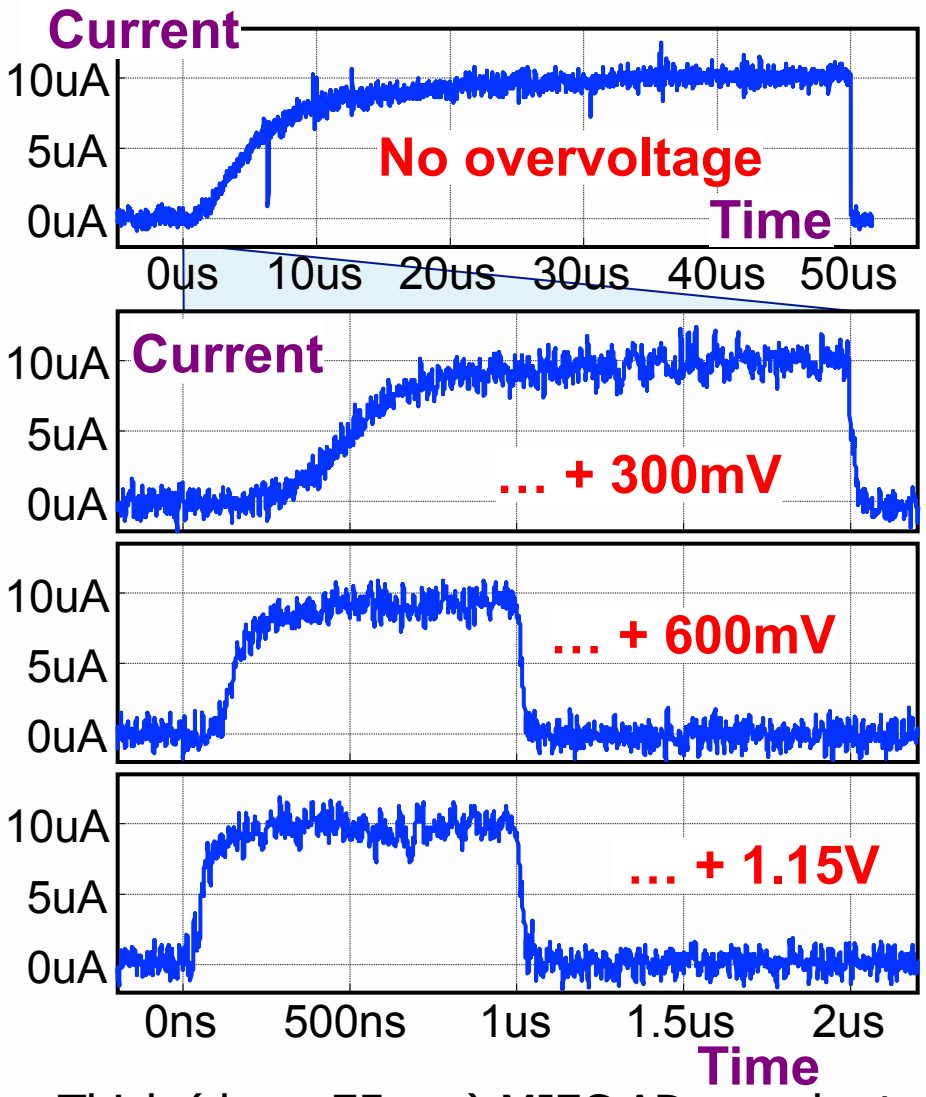
MIEC device recovery dynamics

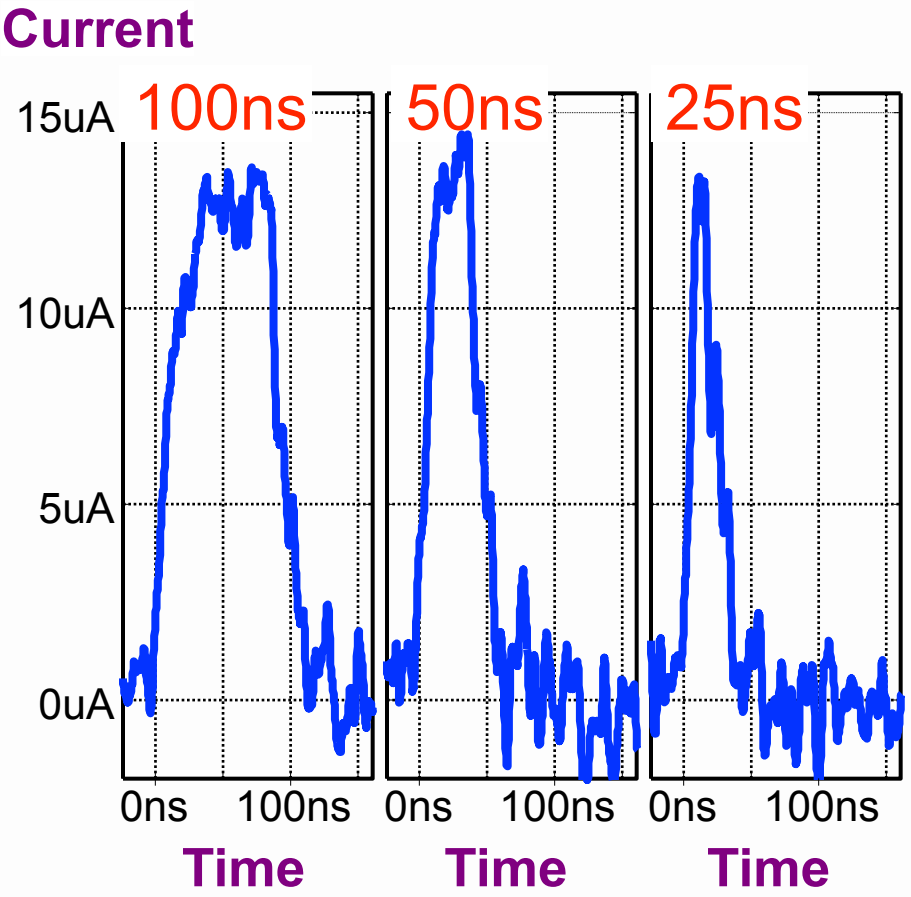


- Recovery even after a **50uA write** pulse takes place within **1-2us**

(Burr *et al*, 2013 VLSI Tech. Sym.)

"Read" turn-on also accelerated by overvoltage

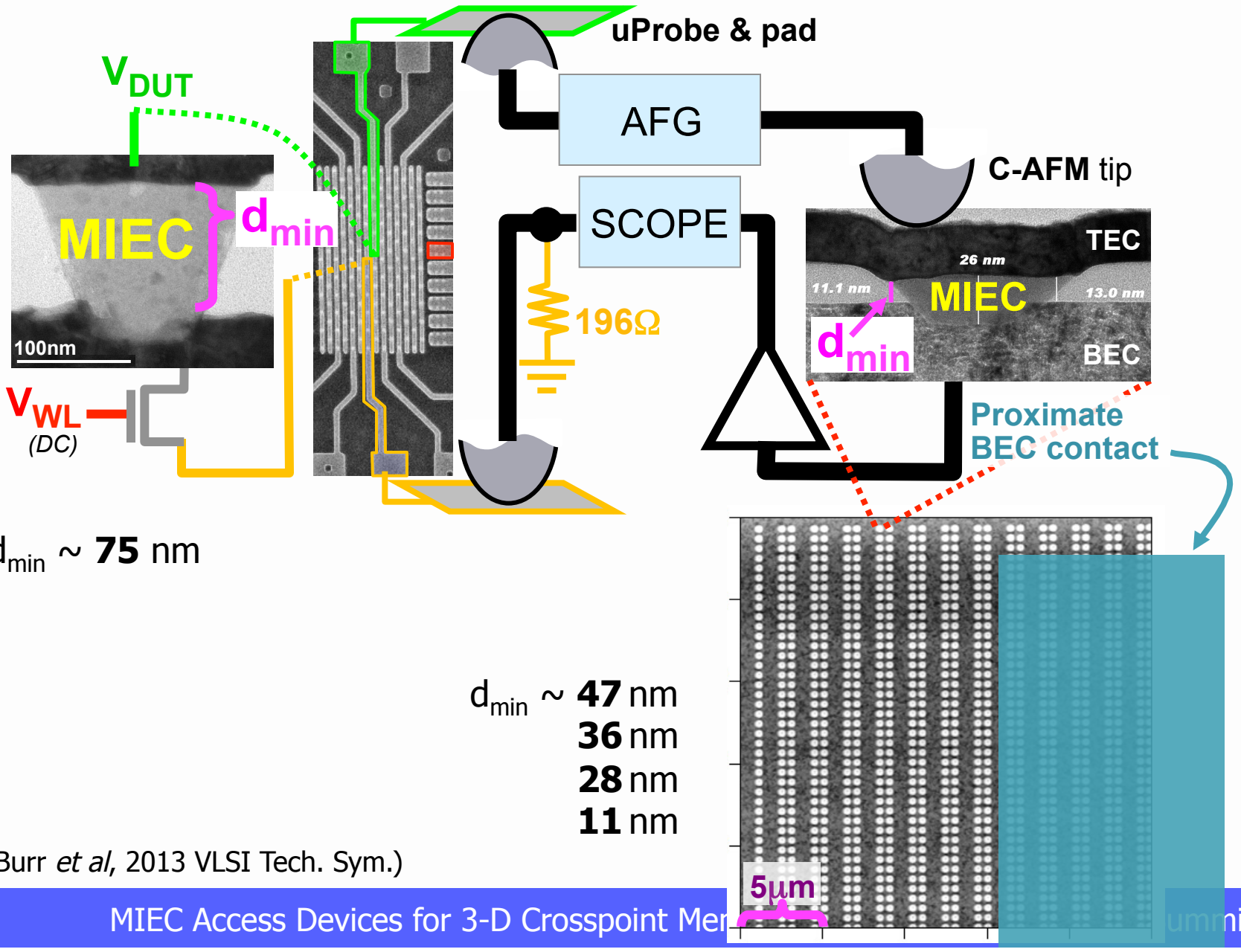




- Thick (d_{min} ~75 nm) MIEC ADs can be turned ON rapidly with large overvoltage
  → transition from half-select to **~10uA read currents in <50ns**

(Burr *et al*, 2013 VLSI Tech. Sym.)

Conductive-AFM testing → thinner MIEC devices

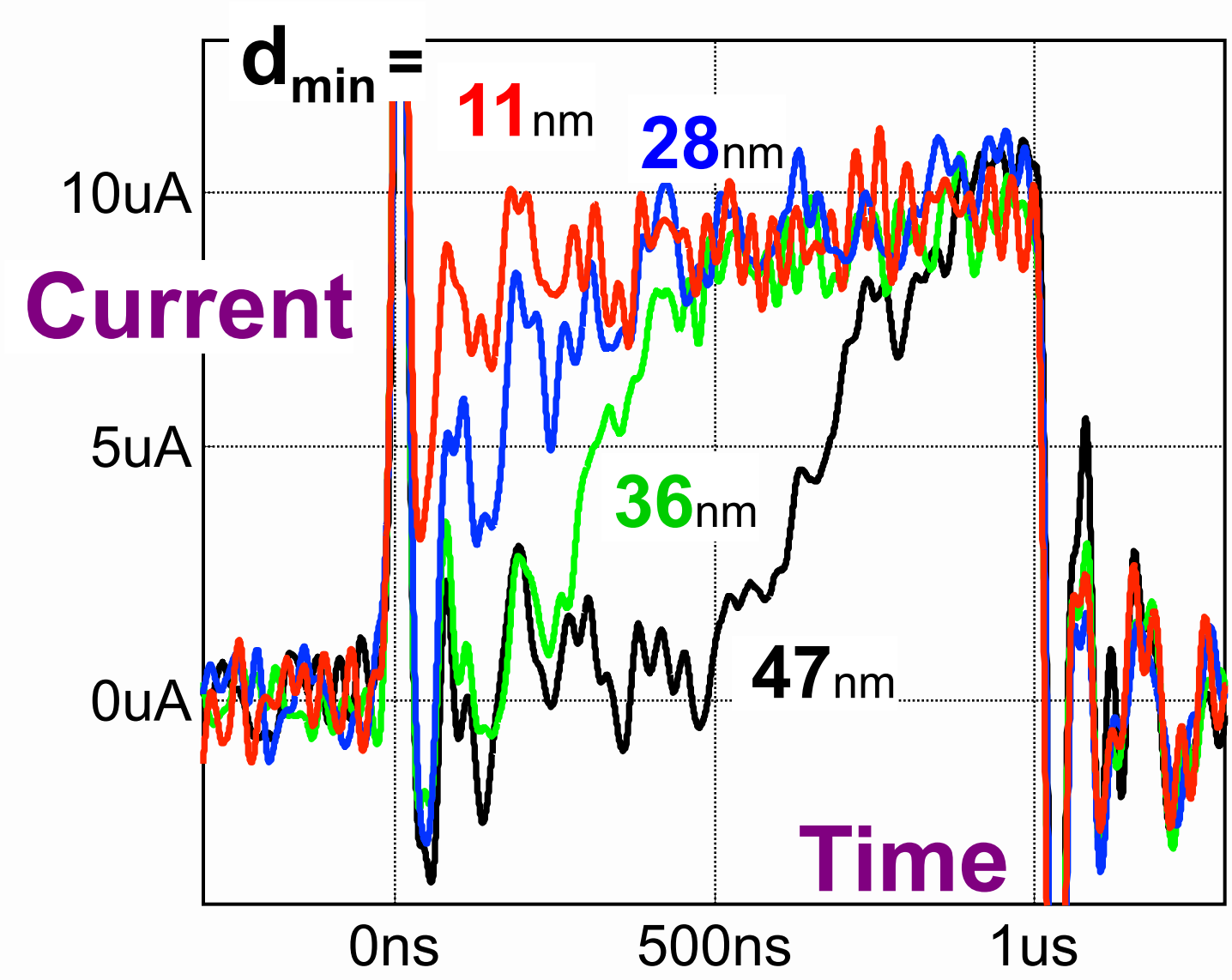


d_{min} ~ **75** nm

d_{min} ~ **47** nm
36 nm
28 nm
11 nm

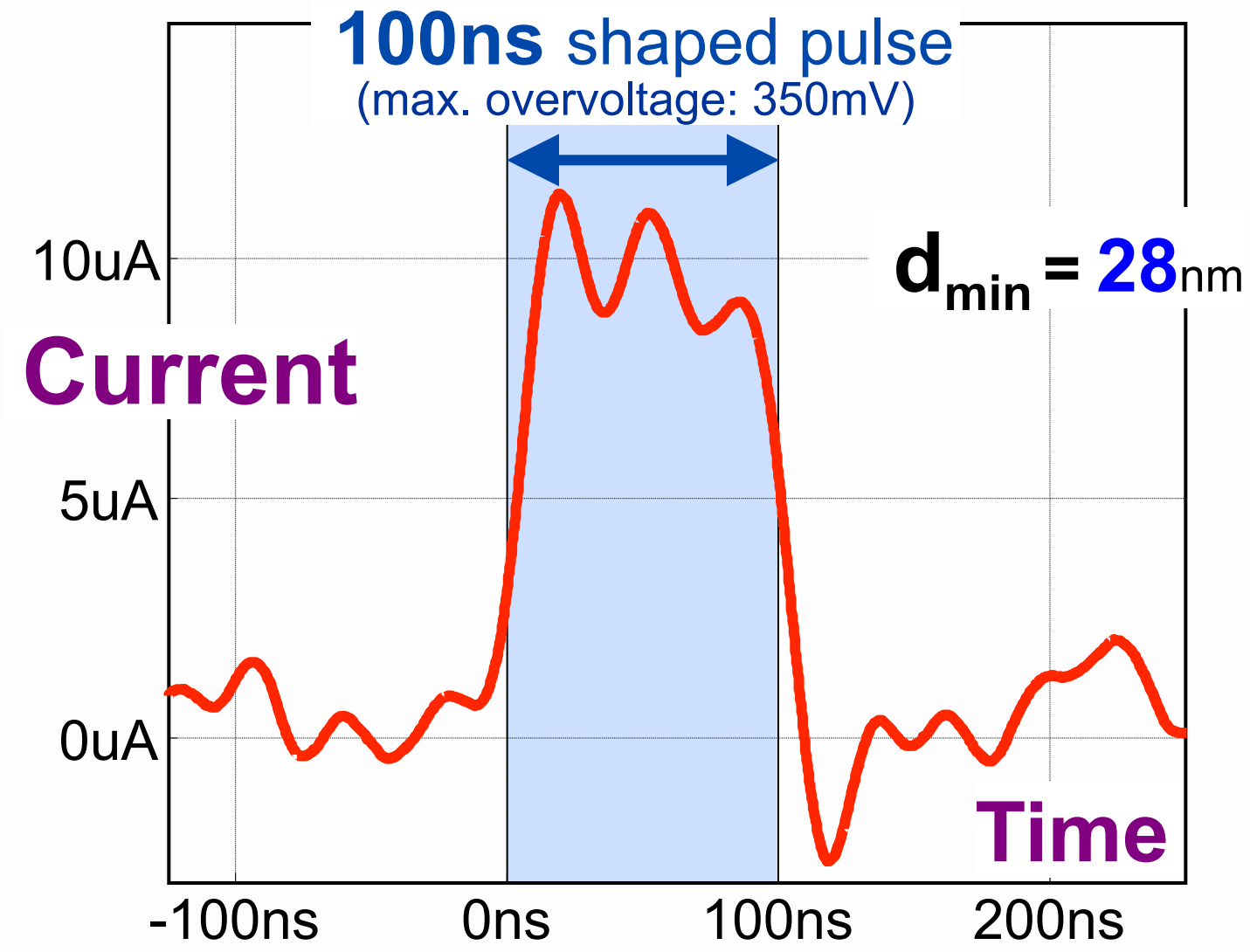
(Burr *et al*, 2013 VLSI Tech. Sym.)

Thinner MIEC devices are inherently faster



(Burr *et al*, 2013 VLSI Tech. Sym.)

Thin MIEC devices → fast at modest overvoltage



(Burr *et al*, 2013 VLSI Tech. Sym.)

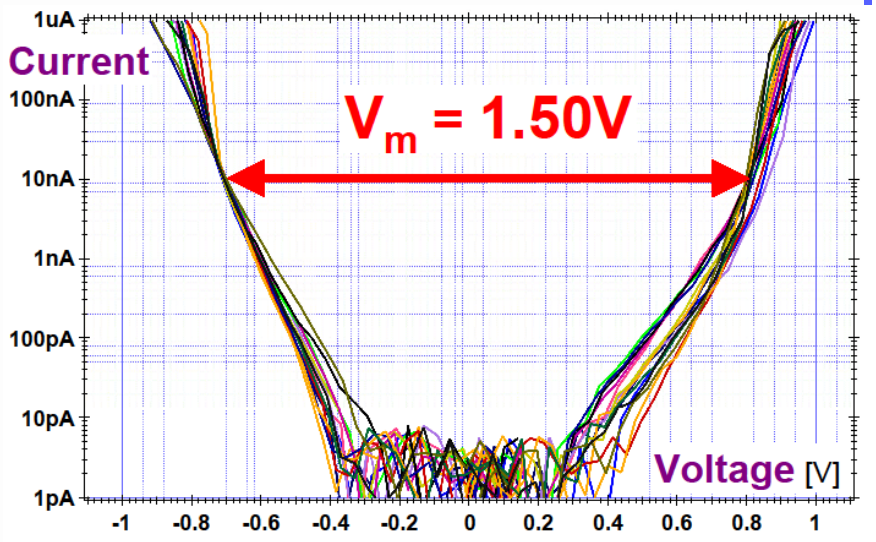
Summary: Mixed-Ionic-Electronic-Conduction (MIEC) Access Device

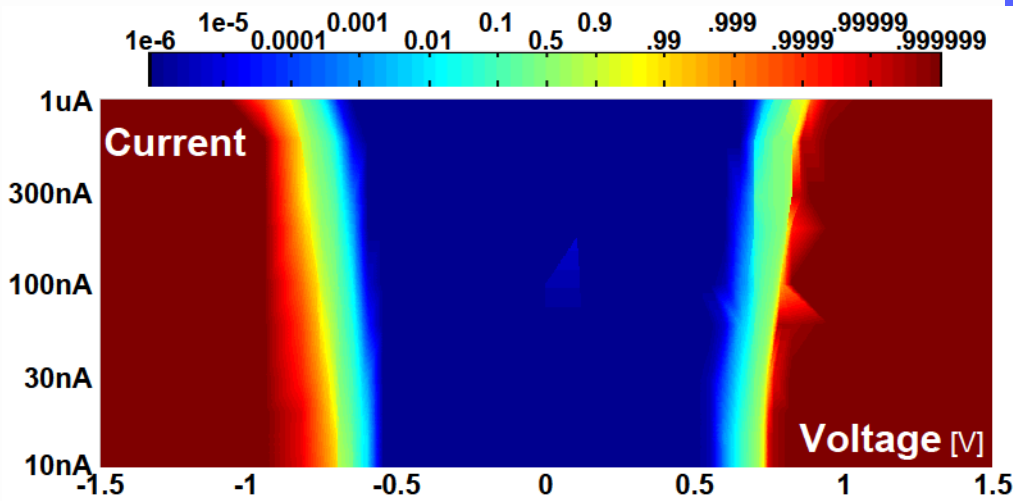
Strengths

- **High** enough **ON currents** for PCM – cycling of PCM has been demonstrated
- **Low** enough **OFF current** for large arrays
- Very large (>>1e10) endurance for typical 5uA read currents
- Voltage margins > 1.5V with tight distributions → sufficient for large arrays
- CMP process demonstrated
- 512kBit arrays demonstrated w/ **100% yield**
- Scalable to <30nm CD, <12nm thickness
- Capable of 15ns write, 50ns read
- Highly stable in un-/half-select conditions

Weaknesses

- Maximum voltage across companion NVM during switching must be low (1-2V) → influences half-select condition and thus achievable array size
- **Endurance during NVM programming** is strongly dependent on programming current





Gopalakrishnan, VLSI 2010
Shenoy, VLSI 2011

Burr, VLSI 2012
Virwani, IEDM 2012
Burr, VLSI 2013

Acknowledgements

- **Teya Topuria, Phil Rice, Eugene Delenia, Leslie Krupp, David Hepner,** and **David Erpelding** - expert analytical and processing support
- **Microelectronics Research Laboratory** (MRL) at IBM T. J. Watson Research Center
- **Stanford Nanofabrication Facility** (SNF)
- Colleagues at IBM Almaden and IBM T. J. Watson Research Centers
- Management support from
  Dr. Chung Lam, **Dr. Winfried Wilcke**,
  Dr. Spike Narayan, and **Dr. T. C. Chen**

Thank you for your attention!

Questions? Please contact *kvirwan@us.ibm.com*

For more information & *MIEC team*

• Overview of storage class memory and MIEC → http://researcher.watson.ibm.com/researcher/view_project.php?id=3631

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