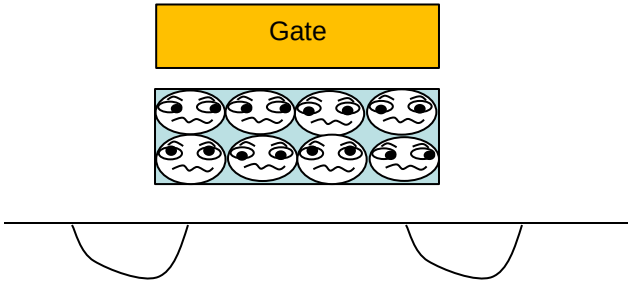
NAND Flash PHY Units for Advanced SSD Design

Hanan Weingarten, CTO, DensBits Technologies

Paradigm change

- 2-Plane NAND Technology is hitting a wall:
  - Sub 1xnm devices suffer from pronounced reliability issues
  - Simple ECC alone is no longer sufficient
  - Handling reliability issues requires a myriad of new techniques – a Memory Modem™
- Next generation products will need to be much more complex or deliver very limited reliability



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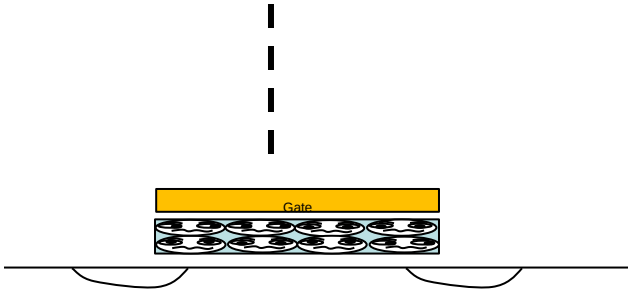


Outline

- FTL and PHY Separation?
- What does the Memory Modem™ Do?
- What does the FTL Do?
- Modular Approach
- Summary

Why separate FTL and PHY-Memory Modem™

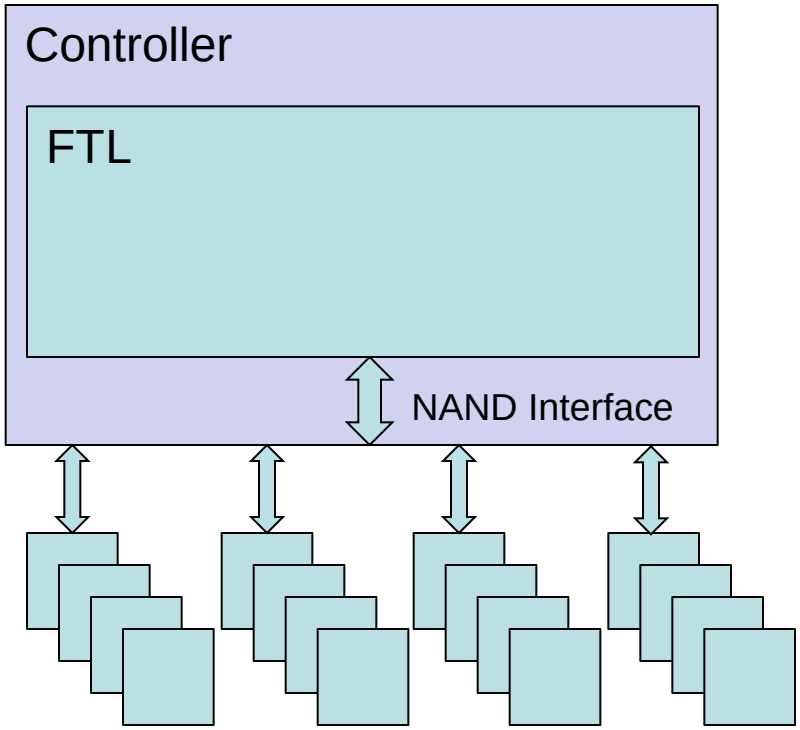
- Time to Market:
  - NAND Flash from different vendors require very different techniques – with different overheads.
    Yet, FTL may remain the same
  - Different applications using same NAND need only FTL changes and no Memory Modem™ change
- Engineering Resources Management:
  - Completely different type of SW expertise
  - Modular design

PHY-Memory Modem™ Integration With FTL

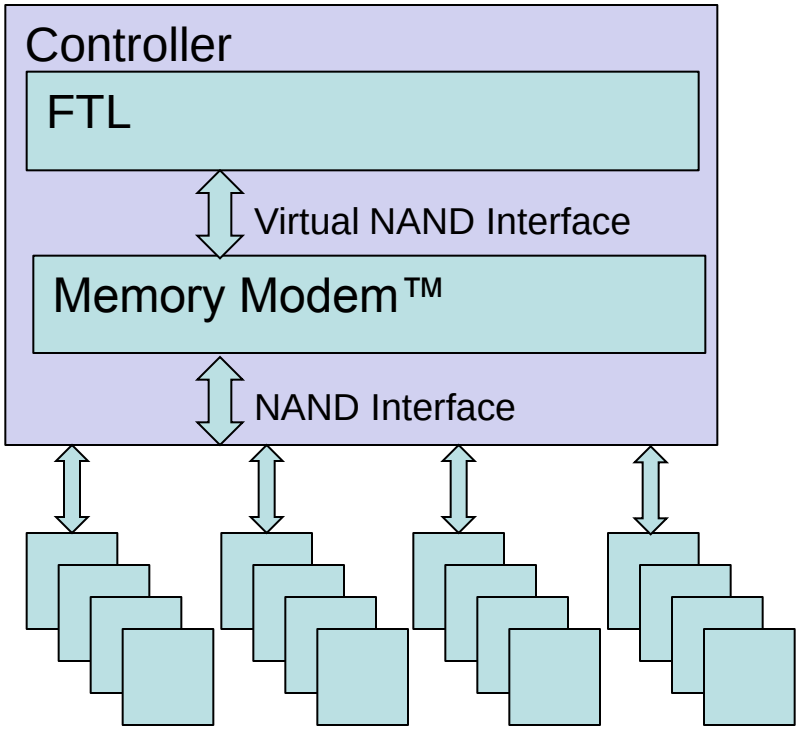
- Memory Modem on Controller:
  - Clear NAND Constrained Design
  - FTL specific adaptation of PHY
  - Resource Sharing

Conventional FTL vs. Separated

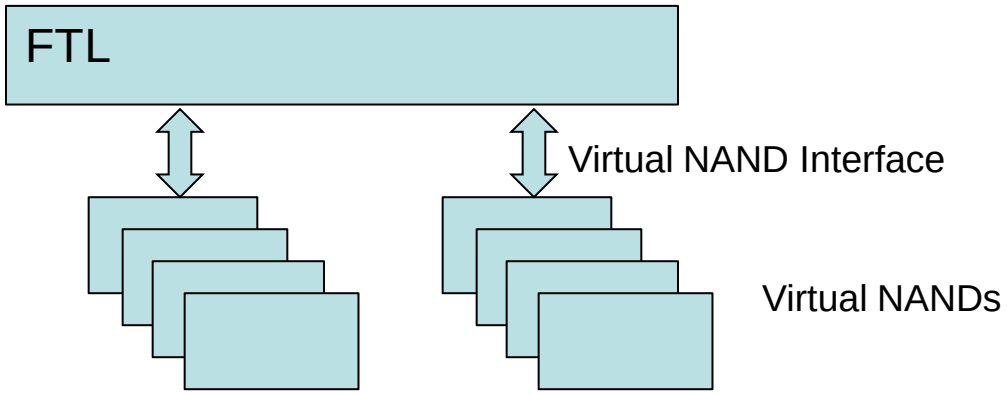
Standard FLASH Controller



Separated FTL - PHY approach



FTL Point of View in a Separated System



- Virtual NAND:
  - Reliable
  - Virtual Block not necessarily same size as Physical block
  - Virtual page size may be larger than a single die page

What does the Memory Modem™ do? (1)

- Handle all reliability issues due to:
  - Endurance
  - Retention
  - Read disturbs
  - Sudden power loss
  - Different block types
  - …
- Optimize raw performance for given NAND Flash type and state:
  - Programming Speeds
  - Read Speeds

What does the Memory Modem™ do? (2)

- How does it do it:
  - Powerful, configurable, low power ECC (not BCH nor LPDC) which performs both hard and soft decoding
  - DSP
  - Low Level Management: Data allocation across NAND blocks and dies to optimize reliability

Memory Modem™ – ECC

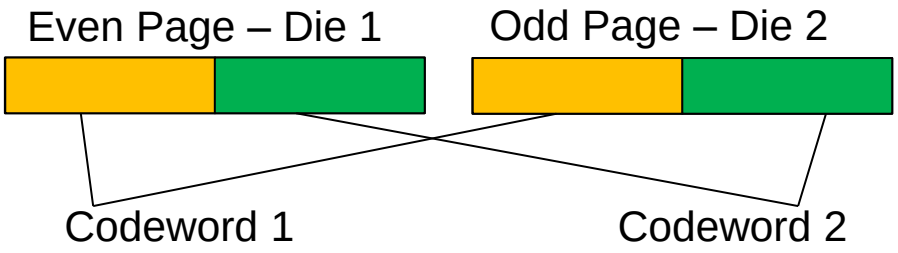
- Near optimal reliability – close to theoretical bound
- Performs both hard and soft decoding
  - Hard decoding determines the joint reliability – performance point
  - Soft decoding performance depends on sampling speeds
- Optimal and high performance hard decoding
- Low power
- Configurable: Code size, code rate, code capabilities

Memory Modem™ - DSP

- Tracks block state
- Modifies NAND trim parameters according to block state to optimize read results
- Modifies NAND trim parameters during programming to optimize reliability and performance (tProg)
- Detect different disturb factors to inform FTL:
  - Stale blocks
  - Read Disturbs
  - …
- Ungraceful power-downs:
  - Detect
  - Recover Data

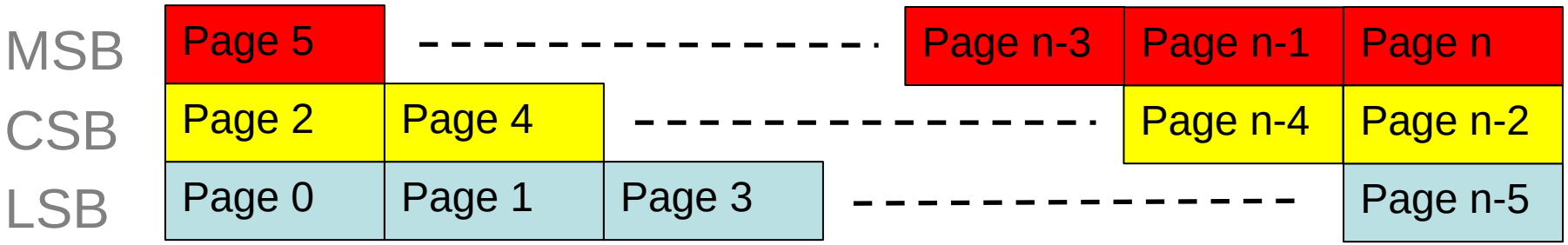
Memory Modem™ - Low Level Management (1)

- Data allocation within blocks and dies can reduce the effect of worst case pages:
  - Example: TLC NAND Flash has 3 types of pages with different BERs: MSB, CSB & LSB (Lower, Middle, Upper)
  - Interleaving between MSB and LSB pages averages BERs
  - Alternatively, variable rate coding may be used



Memory Modem™ - Low Level Management (2)

- To support interleaving or coupling between pages of different types, buffering may be required:
  - Example: Buffering some of the data into SLC to allow striping / coupling between MSB pages of first rows with LSB pages of the last rows



Memory Modem™ - Low Level Management (3)

- Interleaving / Coupling / Variable rate coding schemes:
  - Highly dependent on target devices
  - Dynamic, changing depending on Flash state
  - Choice may affect buffering

- Handled by Memory-Modem, without (or hardly) involving FTL:
  - Buffering should be hidden
  - FTL is ignorant of the choice of data allocation scheme
  - Data allocation scheme may change to support different performance requirements

Memory Modem™ – Adaptive/Dynamic Behavior

- Memory modem™ dynamically tracks NAND Flash state and changes the following:
  - DSP Trim parameters during programming and reading
  - Codeword size, Codeword rates
  - Data allocation strategy: stripping, page coupling, variable rate coding

What Does the FTL Do? (1)

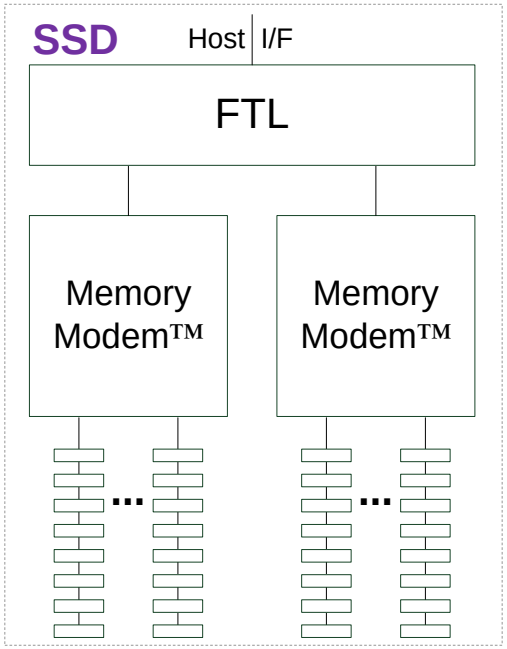
- Handle host interface
- Handle control data
- Data mapping
  - Performance optimized tables
  - De-duplication
  - Compression
  - SLC / MLC / TLC block mapping
- Encryption

What Does the FTL Do? (2)

- High level integrity handling:
  - Wear leveling
  - Bad block handling
  - Power-down recovery – control data
  - Scrubbing
  - …

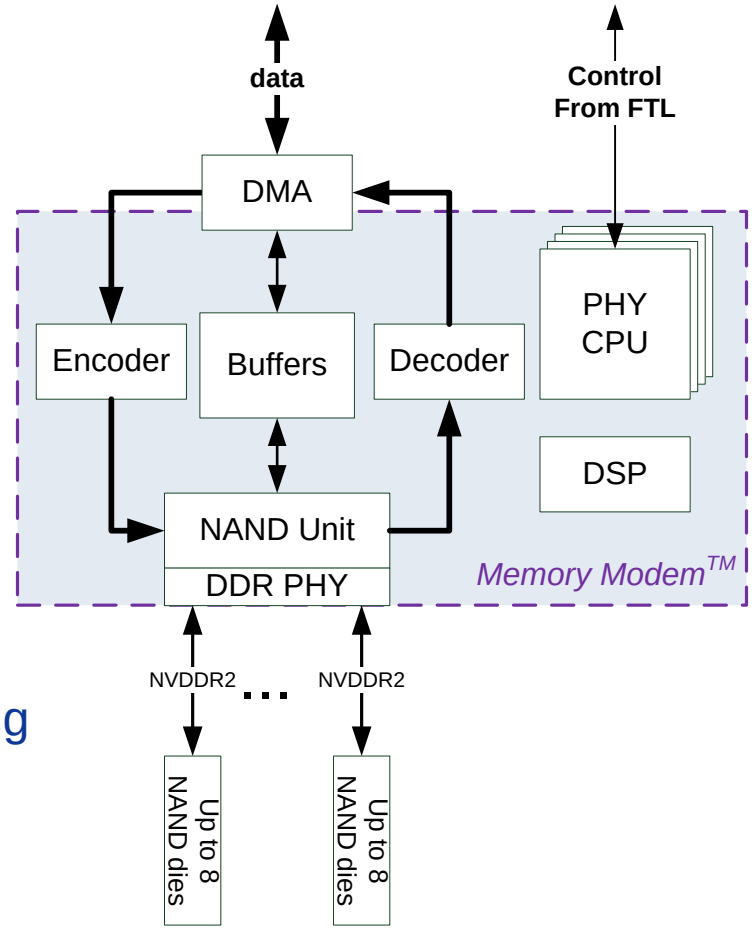
A Modular Approach

- Each Memory Modem™ handles a set of NAND channels
- Each Module may be customizable:
  - Throughput
  - Latency
- Scalable through instantiation:
  - Higher throughputs
  - Higher IOPs
  - Higher capacities
  - Same module may be used for price sensitive embedded systems as well as enterprise SSD



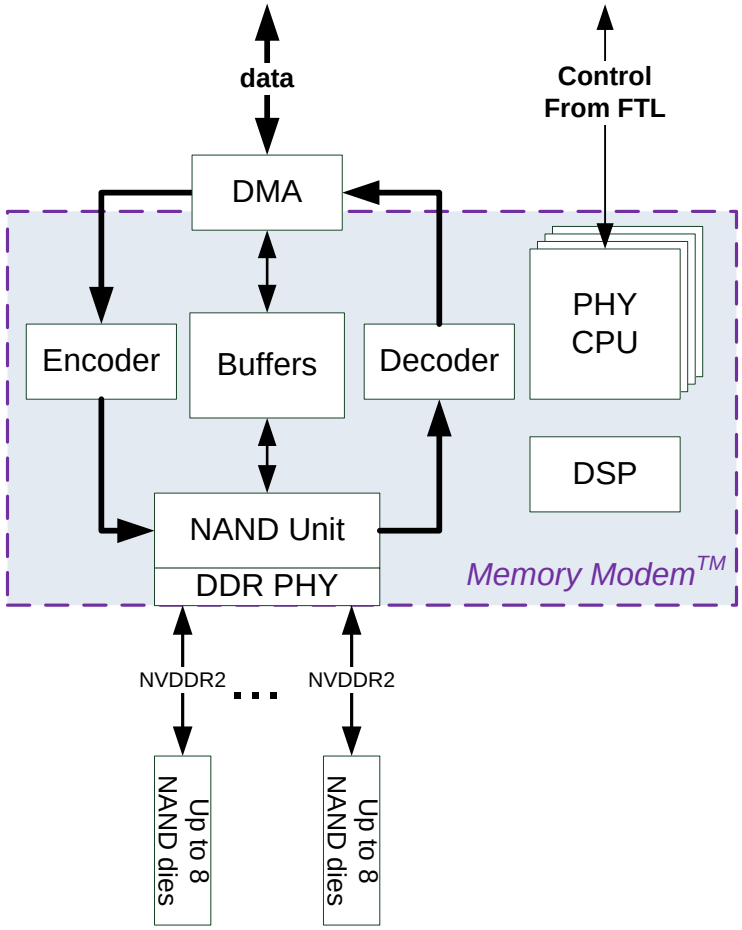
Memory Modem™ Architecture (1)

- ECC Encoder
  - Streaming data operation
- ECC Decoder
  - Hard and Soft decoding
  - High performance:
  - Low latency
- DSP
  - Flexible : adaptable per Flash device
  - Mainly SW
  - Full HW acceleration of data processing



Memory Modem™ Architecture (2)

- NAND Unit
  - High performance
  - High NAND channel utilization
  - Flexible: configurable per Flash device
  - Configurable # of channels and # of dies per channel
- Control Interface FTL to PHY:
  - PHY is slave to FTL level
  - Commands are sent from FTL to PHY
  - PHY sends responses to FTL
  - Large number of outstanding commands



PHY – FTL Interface (1)

- Interface required to support different types of messages:
  - Block refresh required
    - Read Disturb, High Retention, High BER Indication – PHY informs FTL and request block refresh
  - Recovery mode
    - PHY may indicate that entire drive has undergone retention and should be refreshed entirely
  - S.M.A.R.T

PHY – FTL Interface (2)

- Power down indications:
  - Regrets messages
  - Enables Power / Performance Optimization
  - Optimization of boot time
- Internal PHY NCQ:
  - FTL handles operations at PHY Module level

PHY Architecture Customization Continued

- PHY Module Customization :
  - Random Read Requirements → Number of CPUs
  - Sequential Read Requirements → Number of Channels
  - (system / die) Capacity
(system / die) write bandwidth
Channel capability → Max number of devices per Channel
  - Datapath BW
Read performance
Recovery performance end of life → Encoder/Decoder
  - Ungraceful Power Down handling
Write flow
Recovery flow → Buffer Memory Size
- Over all PHY Performance → number of PHY modules

Summary

- New generation of NAND Flash devices require a strong PHY
  - PHY = ECC + DSP + low level management + Flash interface
- FTL-PHY separation modular approach allows scalability and easy adaptation to different applications