Flash below 20nm : What is coming and When

Aug. 13 2013
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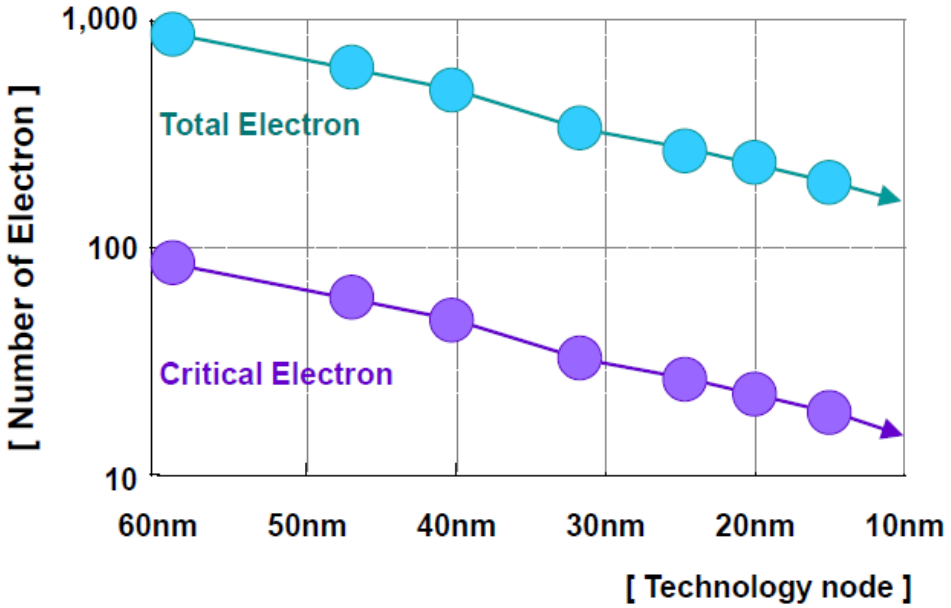
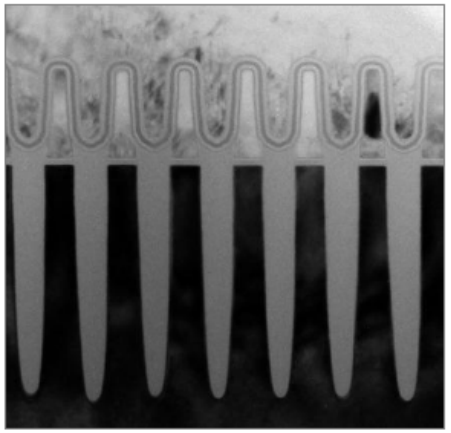
Since the Invention of NAND

There has been big technical breakthroughs,

- Pocket P-well Scheme for Bulk Erase with HVMOS in P-Sub.
- Self Boosting for Reducing Program Disturbance.
- MLC with ISPP Scheme.
- Dynamic Read.
- 3 bits per Cell Invention
- Other Controller Assisted Algorithm

In sub 1x nm cell, limitation in F/G cell is the number of stored electrons





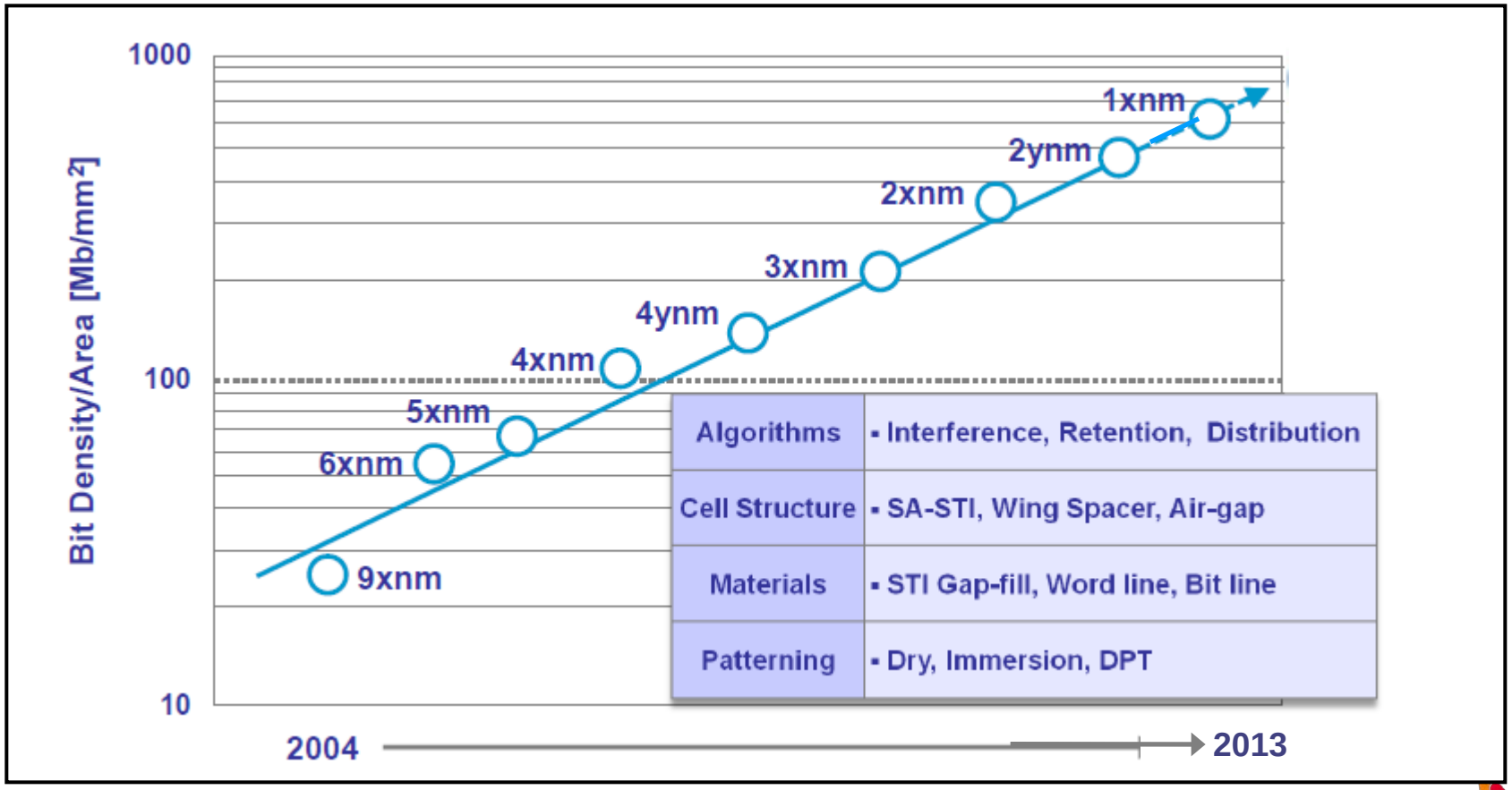
In sub-1x nm,

how to manage 10 electrons is the most critical technical barriers.

NAND Process Scaling : Cost Reduction

We have successfully Increased bit density/area by ~50% per year.

Hynix Technology node during past 10 years. One Tech – node per year



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In addition to the numbers of stored electrons, there are many technical problems,

Issues with 10nm FG		Solutions
X - direction	CG poly-Si void	Device and process optimization, Air Gap in X,Y direction NAND Operation Algorithms for Stress Reduction. Controller Assisted algorithms for reliability
	Interference	
	Bit-Line loading	
Y - direction	WL bending	
	Interference	
	WL-to-WL leakage	

By the process/device optimization and operation algorithms,

SK Hynix successfully developed 16nm technology,

the smallest FG cell dimension.

And SSD of 16nm NAND is displayed in Flash Memory Summit 2013

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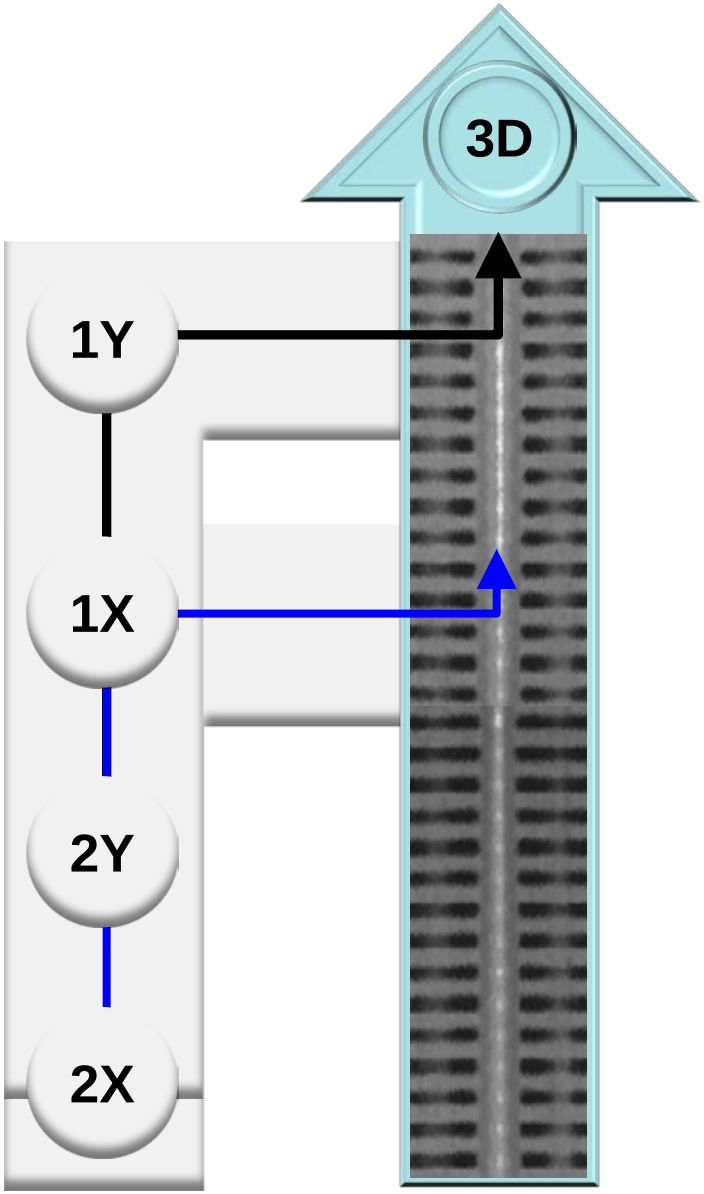
And NAND flash is in



Each company has each strategy of 3D NAND Product

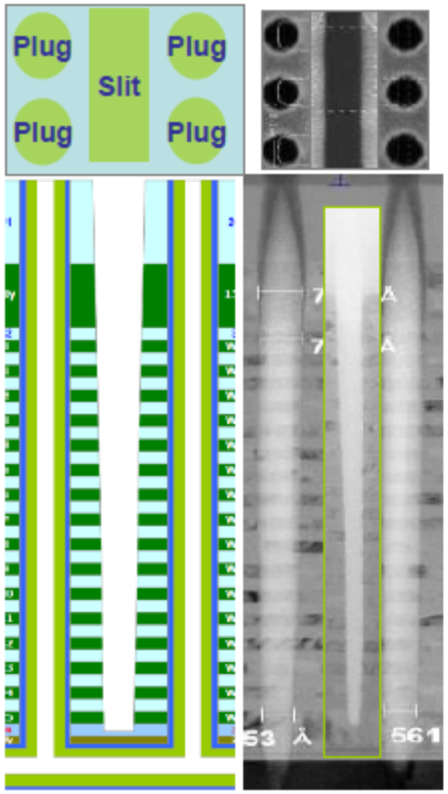
Company A : after 1x technology.

Company B : after 1y technology.

It depends on the Investment and development policy

For a while, FG and 3D NAND will coexist and compete each other in terms of reliability, performance and density.

However, all the 3D NANDs are facing challenges in Yield & Retention



For Yield improvement

- Stabilization of multi-stack patterning
- Metrology
- Defect monitoring for deep inside 3D-structure

For retention

- Needs careful cell optimization

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As progress done in SK Hynix during F/G era, especially in 1y nm technology,

Needs in 3D will be overcome by ….,

- Deeper understanding of NWFET physics
- Stabilization in Etch and Thin Film Process
- Mobility enhancement in pillar type channel
- Higher Work Function Gate material
  and higher K dielectric for stable erase.
- New storage site, such as dots rather than SiN,

3D product will be available in the end of this year.

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Thank you for your attention.

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