Flash Below 20 nm: What is Coming and When?

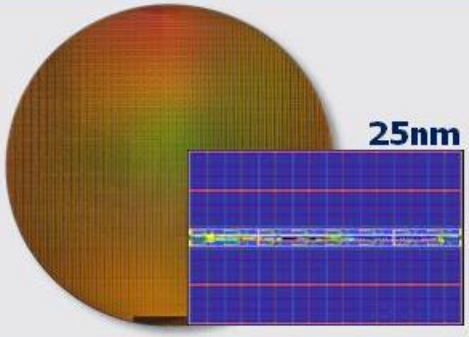
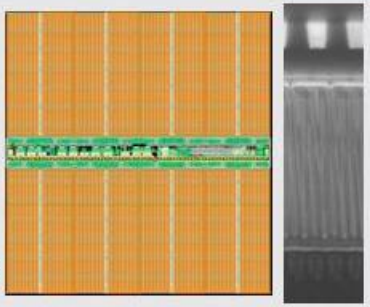
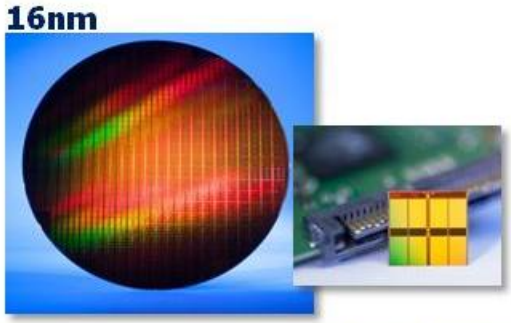
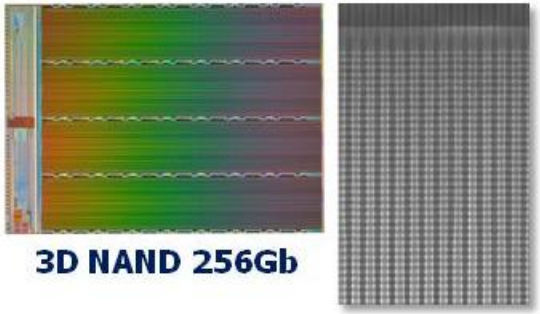
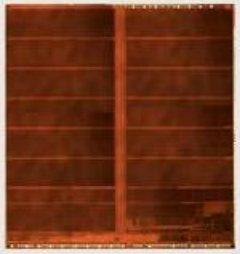
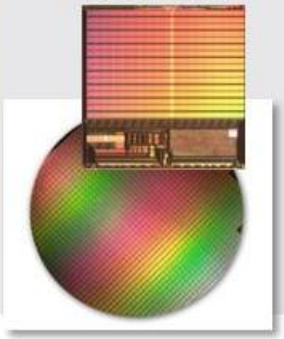
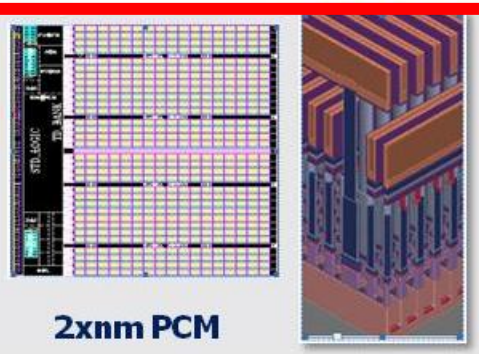
Chuck Dennison

Senior Director NAND Process Integration

Micron Technology

©2013 Micron Technology, Inc.

Micron's Industry Leading Diversified Semiconductor Product Portfolio

	Leading Edge Production	Next Node
DRAM		
NAND		
NOR PCM	 	

Images are not to scale.

NAND Sees Large Growth From Mobility and SSD

Demand Growth is in Balance With Expected Supply Growth

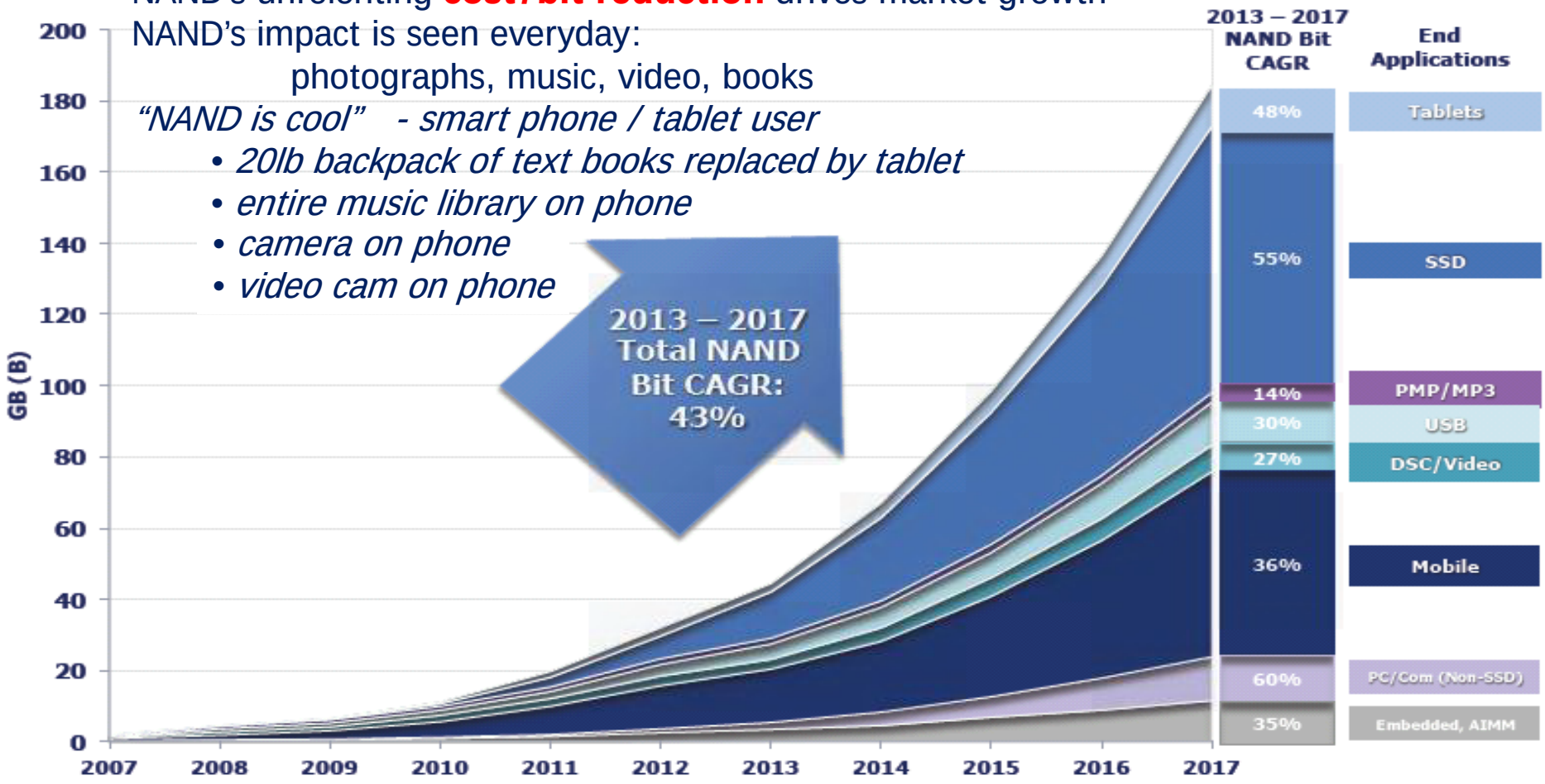
NAND's unrelenting **cost / bit reduction** drives market growth

NAND's impact is seen everyday:

photographs, music, video, books

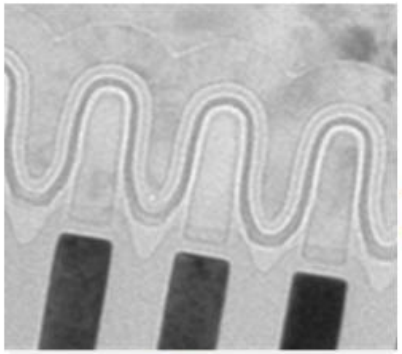
"NAND is cool" - smart phone / tablet user

- *20lb backpack of text books replaced by tablet*
- *entire music library on phone*
- *camera on phone*
- *video cam on phone*

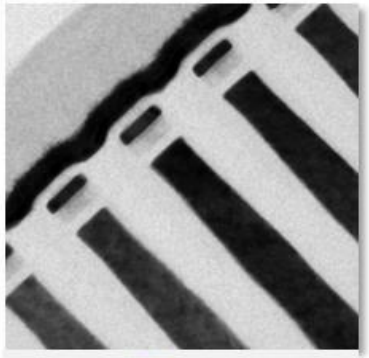


Source: Gartner 2Q13; Cards included in Mobile and DSC

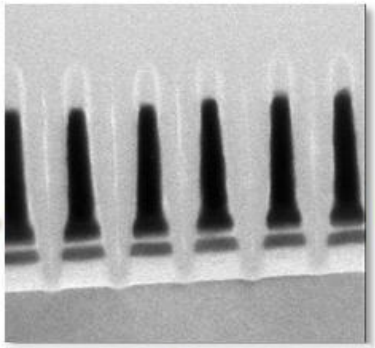
Micron NAND Technology Scaling Path



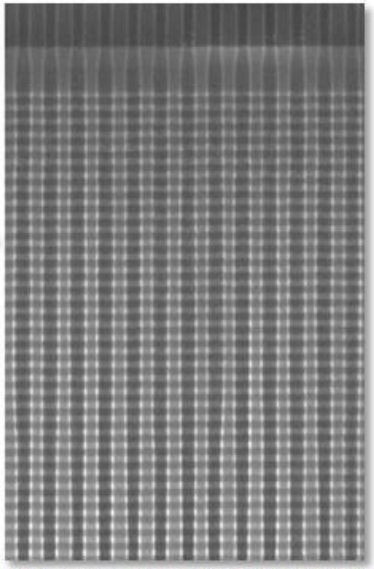
25nm



20nm

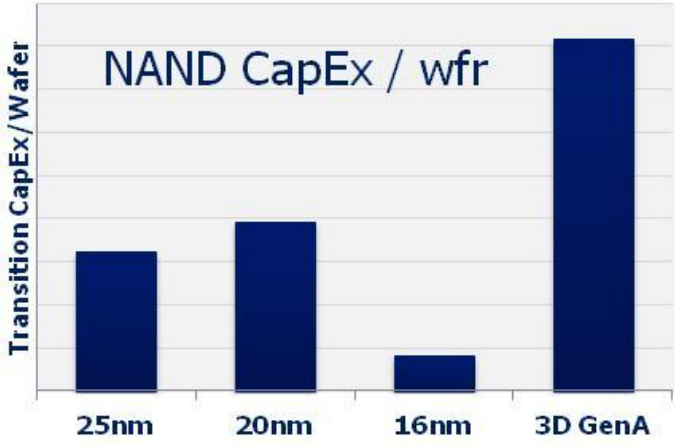


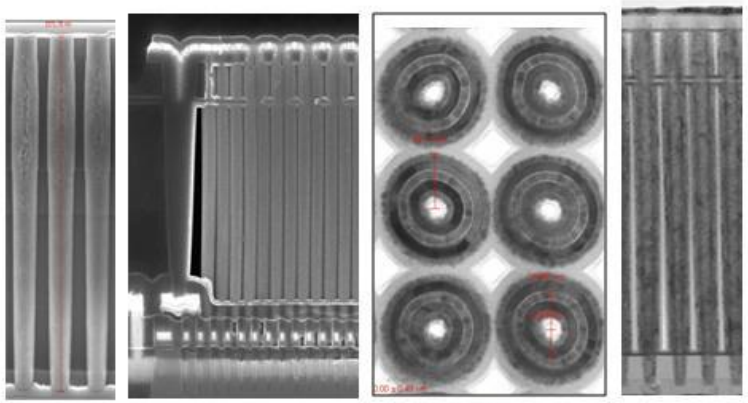
16nm



Micron-Intel 3D NAND

- Proprietary Intel/Micron High K Planar NAND cell enables minimum CapEx expenditure for transition from 20 to 16 nm
- HVM DRAM module process expertise leveraged in 3D NAND
  - ➢High aspect ratio etching, ALD fill, planarization of large array topog





HVM DRAM Modules

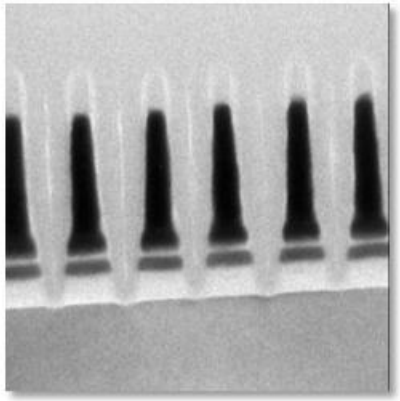
3D NAND: Very Cool

Non-volatile Memory Technology Strategy

Inflection point ➔ Planar to Vertical NAND Technology

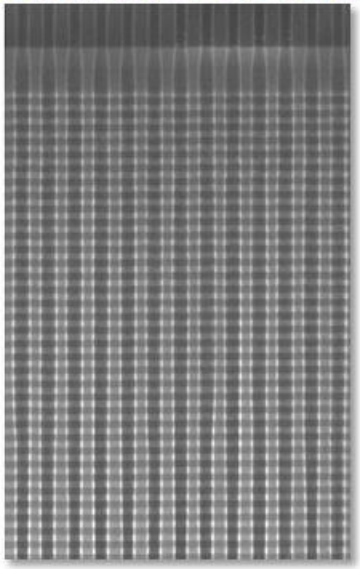
Inflection point ➔ Performance enabling new memory technology

16nm planar NAND



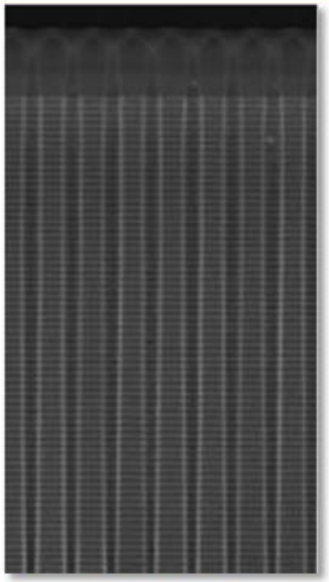
Micron/Intel unique cell technology enables differentiation in performance and cost for planar NAND.

Micron-Intel 3D NAND

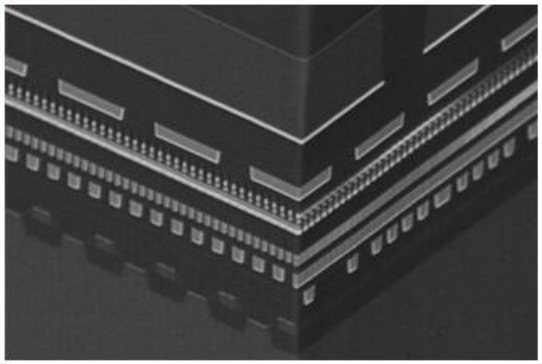


Transition to Vertical NAND at 256Gb density based on significant cost/bit and performance benefit relative to strong planar 16nm node.

Allows Micron to introduce 3D NAND *when it makes financial sense.*

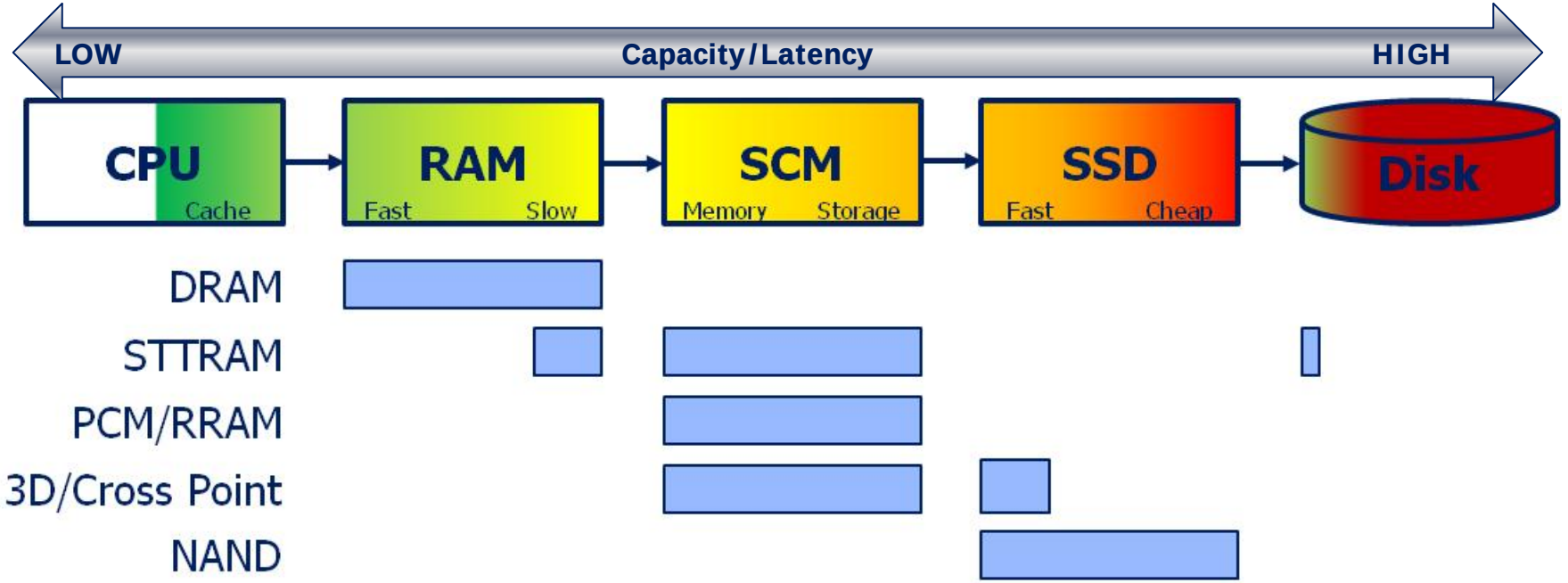


Vertical NAND Scaling: Cost Optimized Storage



New Memory Technology: Performance Differentiated

Differentiation Opportunities with Emerging Memories



- NAND and DRAM continue to exclusively cover significant portions of memory applications
- Emerging NV: lower latency compared to NAND, enhances system level power/performance
  - selectively displaces, rather than replaces DRAM or NAND
- Multi-layer cross point: 3D memory technology, but requires 2-3 minimum litho patterning per layer compared to 3D NAND which patterns multiple layers (24+) in a single step.
  - Technology Scaling Roadmap not held hostage waiting for "cost effective" EUV
- Transition to 3D NAND enables continuation of cost reduction, remains largest memory segment and continues to expand into new applications, thus keeping "*Very Cool*" status

Micron®
Focused on Memory | Engineered for Innovation