



Flash Memory Summit 2013
Plenary Session: Flash Below 20 nm:
What is Coming and When

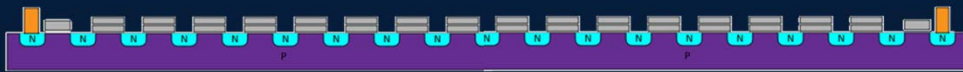
Challenges in 3D NAND



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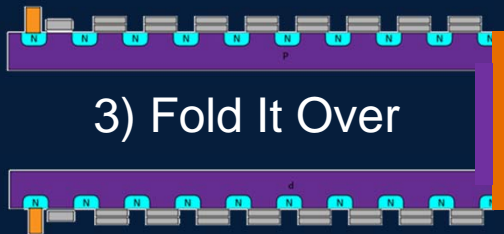
3D NAND



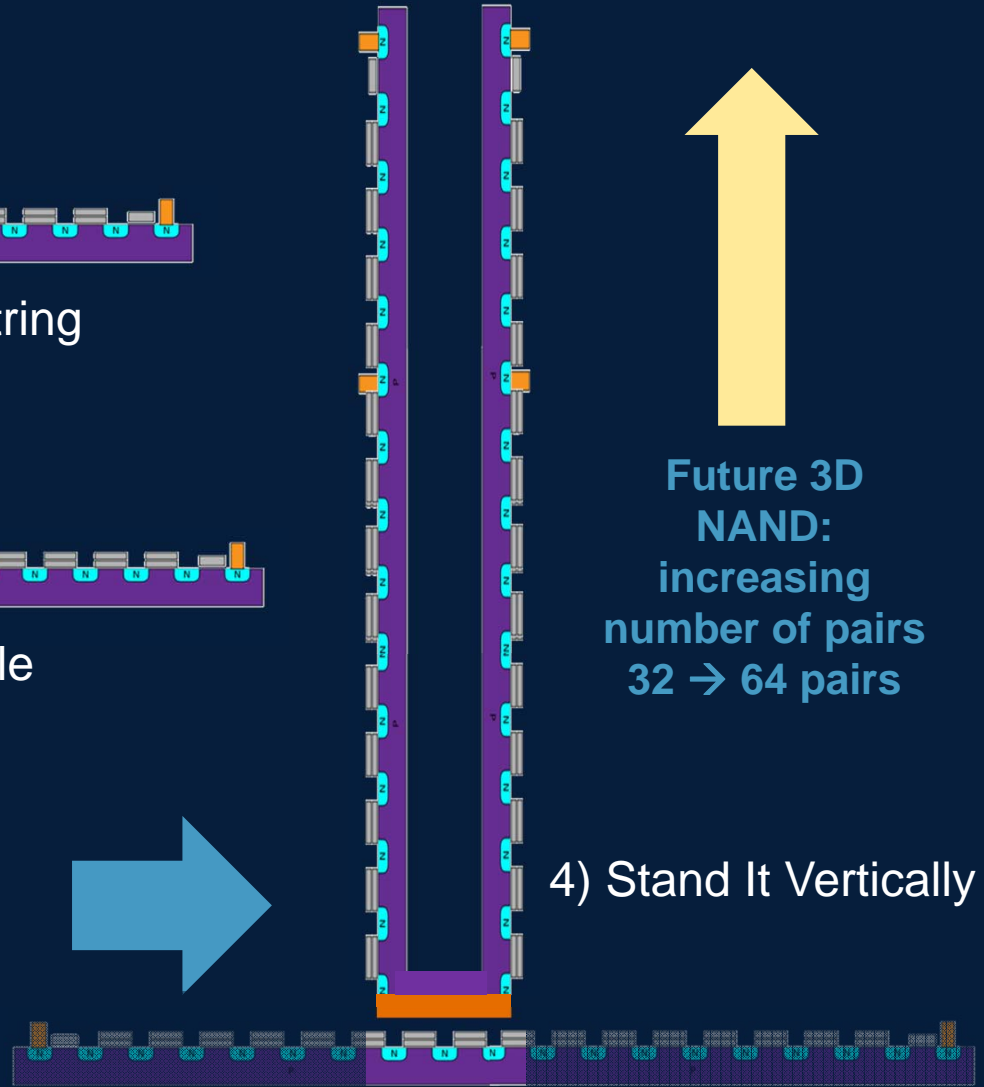
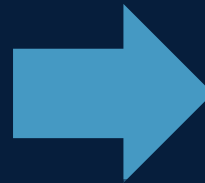
1) Typical Planar NAND Cell String



2) Stretch It Out In The Middle



3) Fold It Over



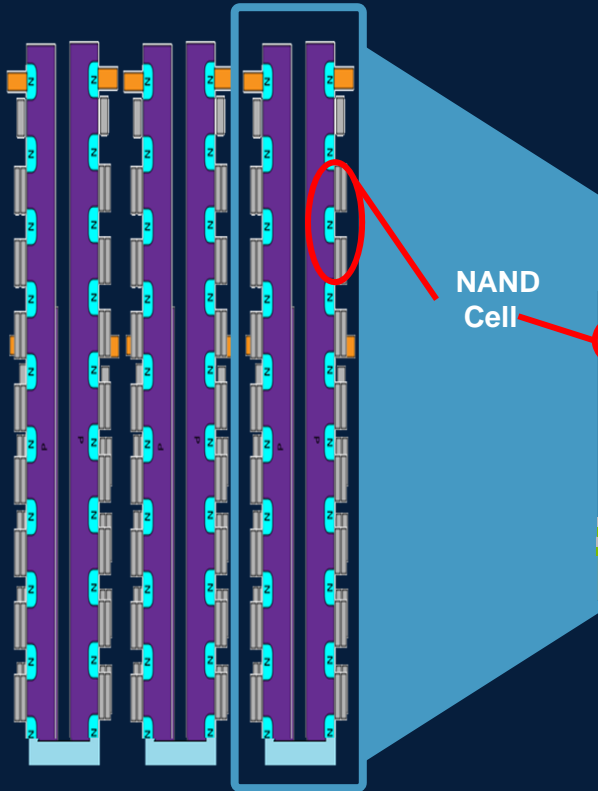
Future 3D
NAND:
increasing
number of pairs
32 → 64 pairs

4) Stand It Vertically

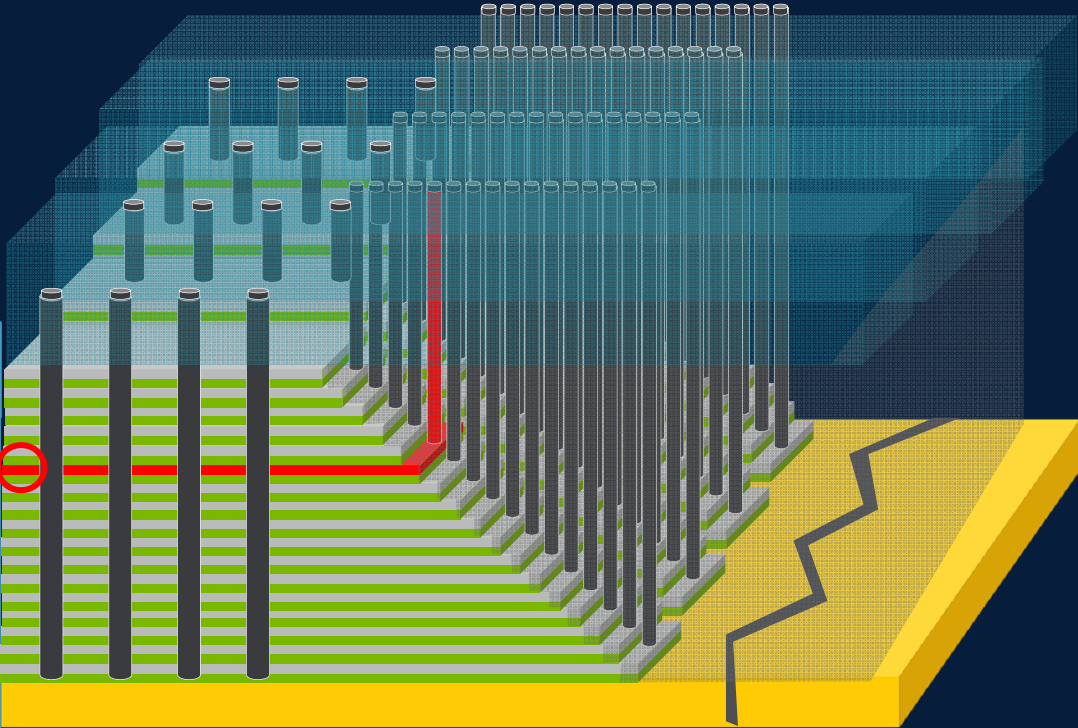
**3D NAND Uses Less Wafer Area Than 2D
For Same Bit Density**

3D NAND

5) Replicate

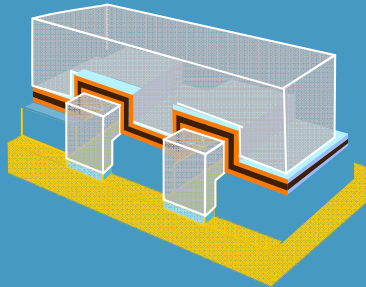


6) Make contact to staircase vias



3D NAND does not require leading-edge lithography, but it will require new deposition and etch technologies.

3D NAND: Game Changer for Etch and Deposition



PLANAR

3D NAND



1

CD DEFINITION AND SCALING ($<15\text{nm}$)

Lithography

CD DEFINITION AND SCALING ($\sim 50\text{nm}$)

Etch and Deposition Grows
Lithography drops

2

ETCH

Lower aspect ratios
Multi-patterning (SATP, SAQP)

ETCH

High aspect ratios
Staircase patterning (trim and etch)

3

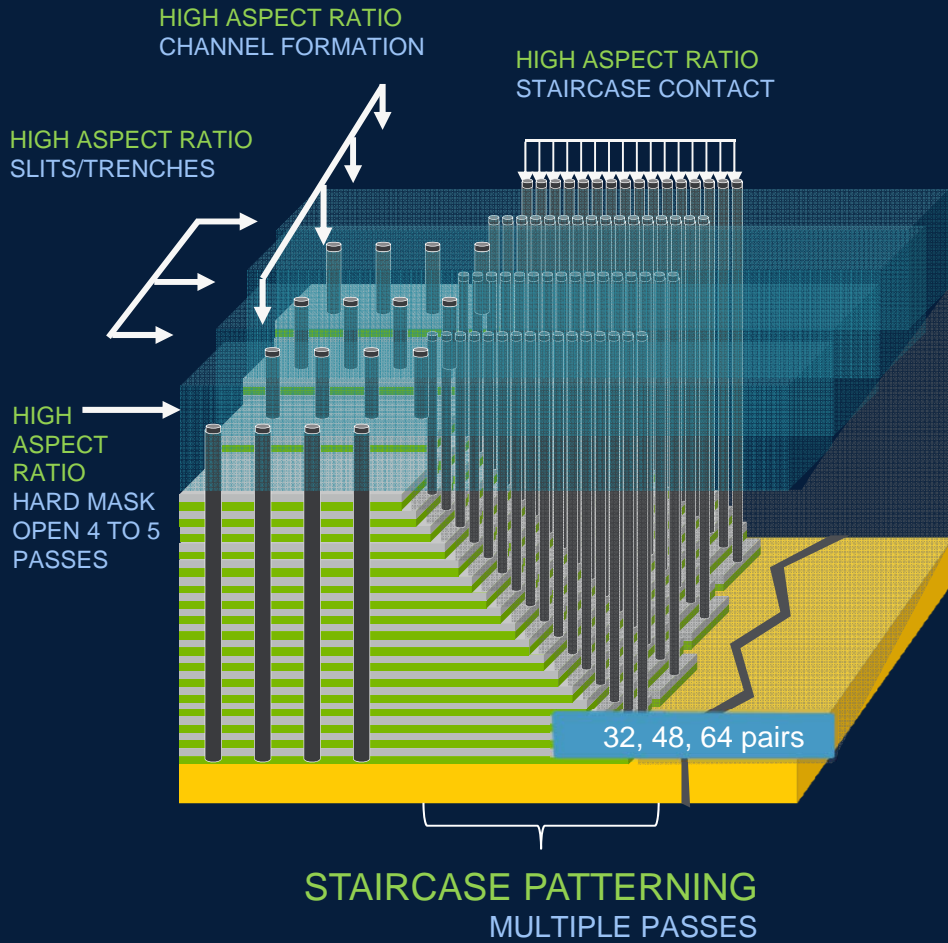
DEPOSITION

Single layer
Thinner films

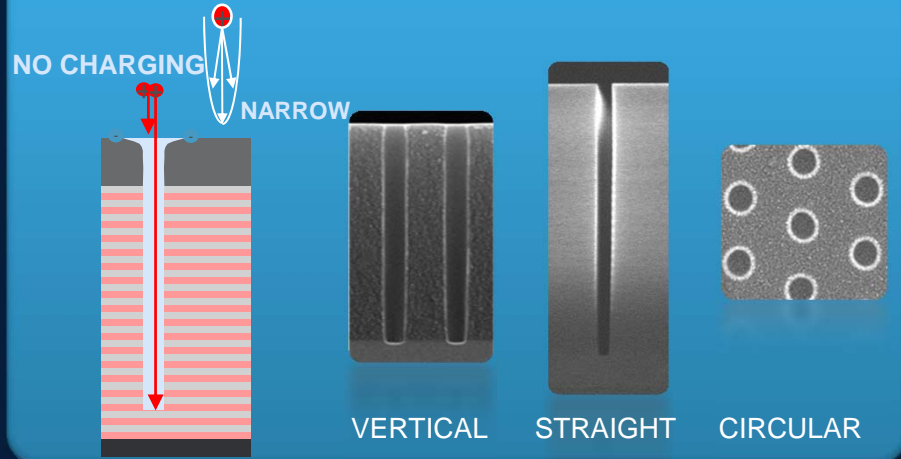
DEPOSITION

Multi-layer stacks
Thick films (active and hardmask)

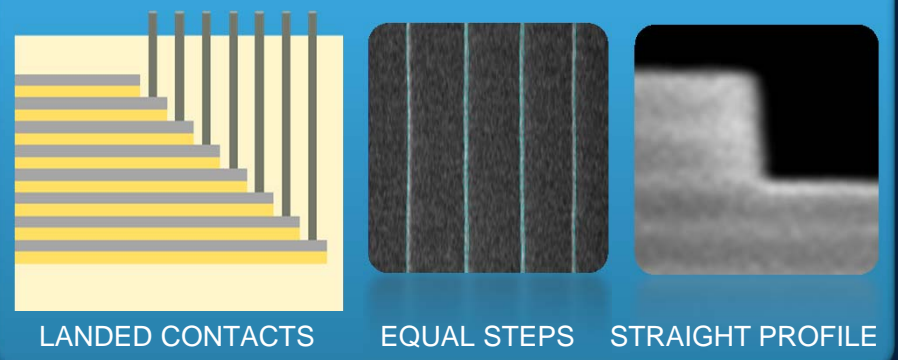
3D NAND: New Etch Applications



HIGH ASPECT RATIO



STAIRCASE PATTERNING



Sources: VLSI and IEDM

3D NAND: New CVD Applications

Critical Hardmask

Channel, Word Line, Metal Contact
High Aspect Ratios up to 60:1

Gate Stack

Oxide/Nitride or Silicon

CVD Gapfill

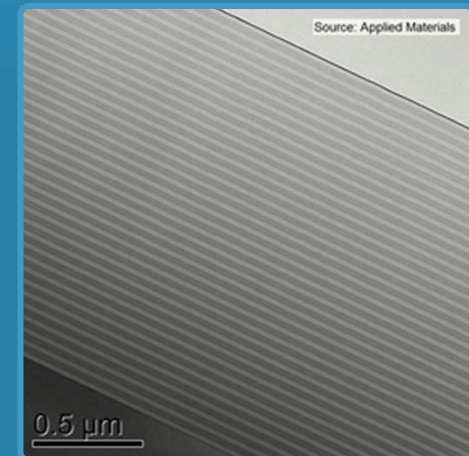
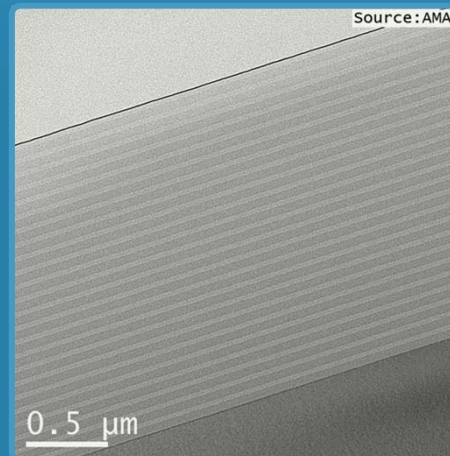
Isolation
and Interlayer
Dielectrics

Gate Stack Challenges:

- Film Thickness determines Gate Length; Uniformity is Critical
- Manufacturing costs will pace adoption due to lower throughputs

Gate Stack Solution:

- Innovative Precision CVD Chamber Design with
 - Uniform deposition with layer-to-layer precision
 - Superior repeatability with independent station control
 - Higher Chamber throughput efficiency with lower operating cost



Sources: VLSI and IEDM

