

# SanDisk®

**Flash Memory Summit 2013 Plenary Session**  
**Flash Below 20 nm: What is Coming and When**

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# Forward-Looking Statement



During our presentation today we may make forward-looking statements.

Any statement that refers to expectations, projections or other characterizations of future events or circumstances is a forward-looking statement, including those relating to revenue, unit sales, pricing, market positions, market growth, product sales, industry trends, expenses, gross margin or other financial measures, capital investments, cash flow, use of cash, customer relationships and partnerships, strategic investments and other strategic transactions, competition and competitive advantages, future memory and other technologies, production capacity, technology transitions and future products.

Actual results may differ materially from those expressed in these forward-looking statements including due to the factors detailed under the caption “Risk Factors” and elsewhere in the documents we file from time-to-time with the SEC, including our annual and quarterly reports.

We undertake no obligation to update these forward-looking statements, which speak only as of Aug 13, 2013.

# SanDisk NAND Memory Roadmap



	2012	2013E	2014E	2015E	2016E
2D-NAND	19nm X2,X3	1Y X2,X3		1Z X2,X3	
BiCS (3D-NAND)				BiCS Pilot	BiCS Production

Note: Box denotes start of meaningful production for the lead products

19nm lowest cost technology in production

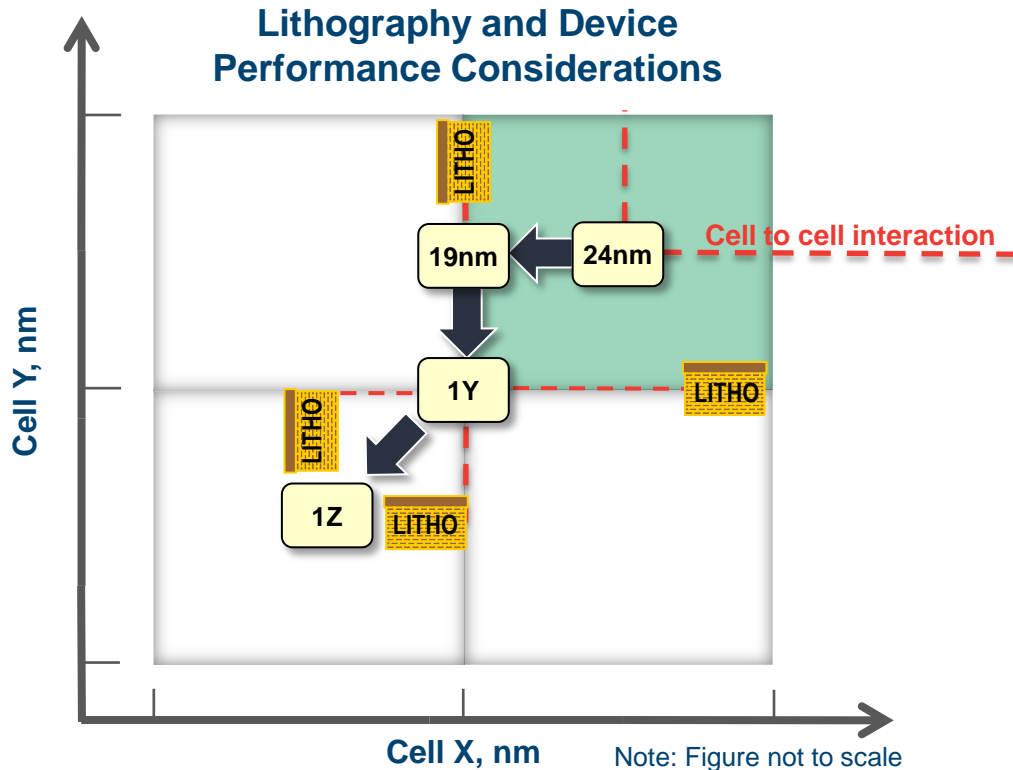
1Y NAND ramp-up in 2H-13

1Z NAND feasibility established

BiCS (3D-NAND) targeted to provide meaningful cost reduction versus 1Z

From 2013 Investor Day, May 8, 2013

# 2D-NAND Scaling Path



Scaling 24nm  $\rightarrow$  19nm:  
Optimize available lithography  
and X dimension Cell to Cell  
solution

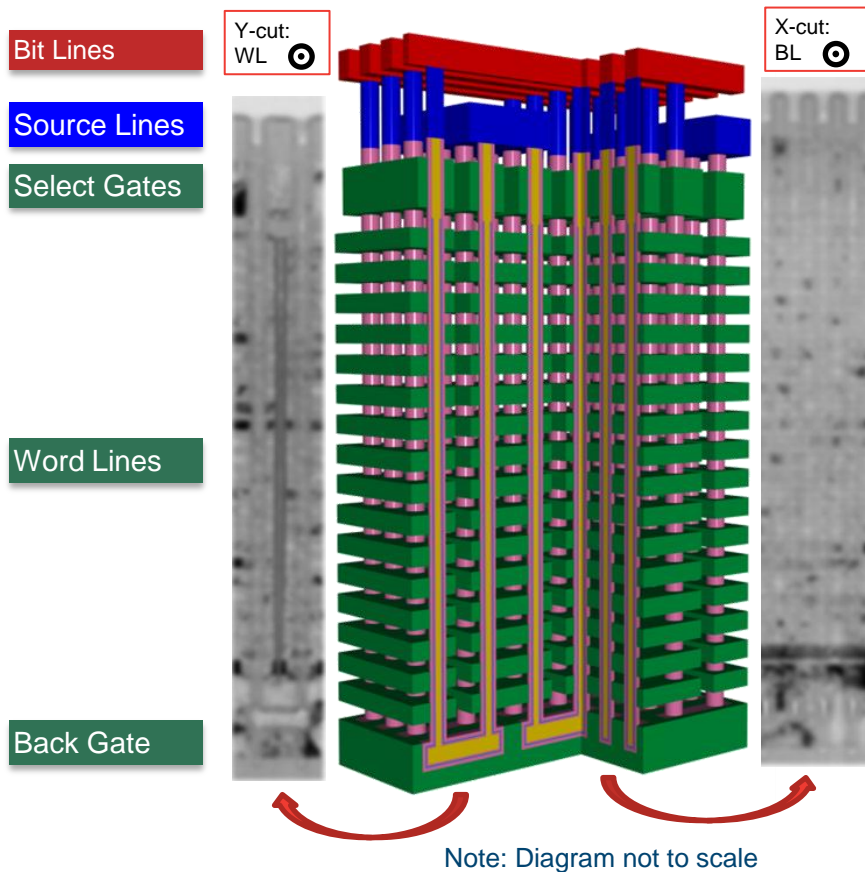
Scaling 19nm  $\rightarrow$  1Y: Implement  
Cell to Cell solution in Y  
dimension

Scaling 1Y  $\rightarrow$  1Z: Optimize  
both X, Y dimensions for  
available finer lithography

We believe this scaling path  
gives us the lowest cost  
and a clear technology  
leadership

From 2013 Investor Day, May 8, 2013

# BiCS 3D-NAND



BiCS delivers smallest chip area of any published 3D-NAND

BiCS U-shaped NAND string enables maximum array efficiency

- Leverages existing NAND Fab infrastructure. Does not need EUV.
- Scaling achieved by increasing number of layers

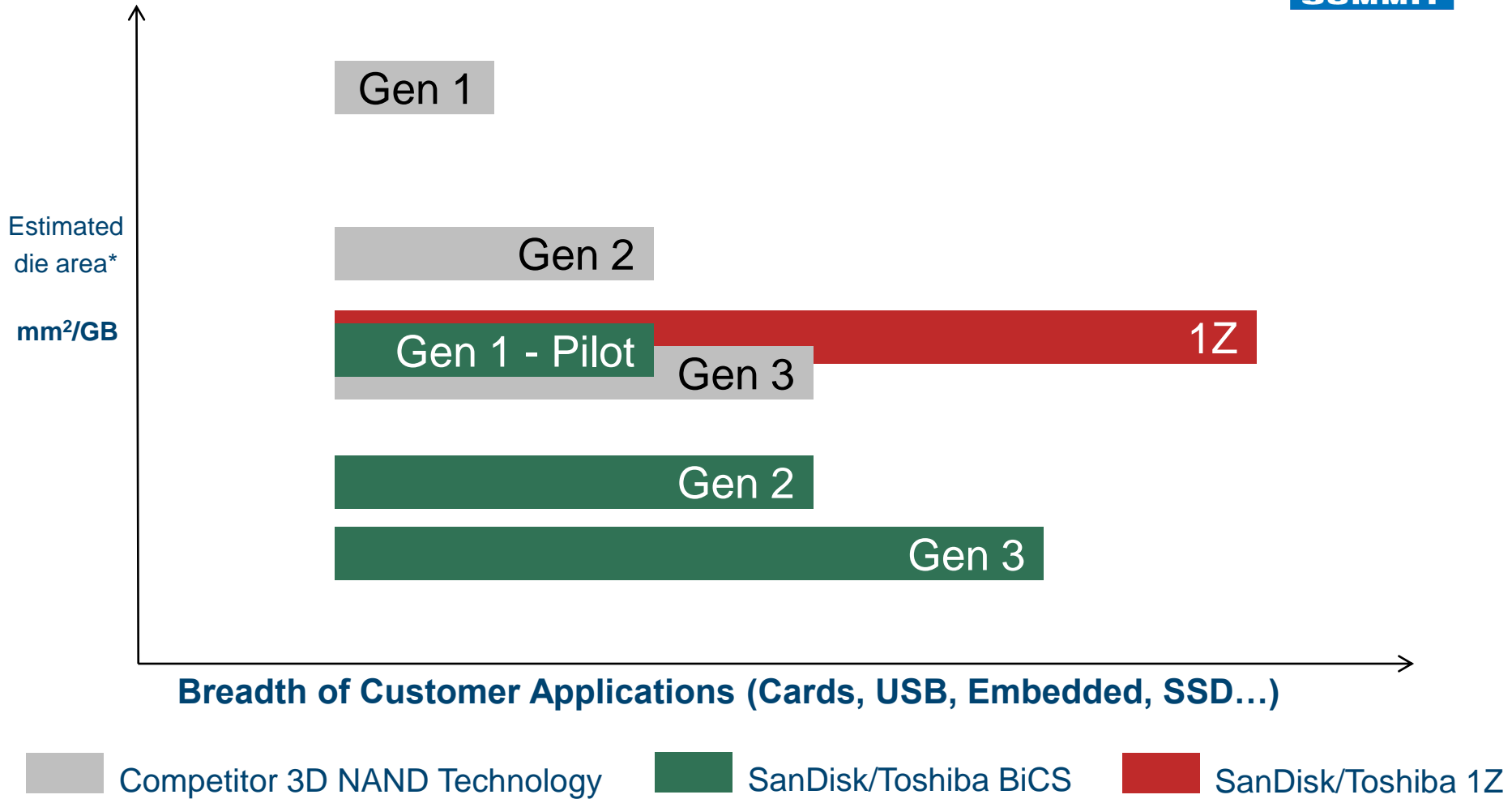
Good progress in BiCS development

Challenges for all 3D-NAND manufacturing

- NAND poly TFT devices, a first in volume manufacturing
- High aspect ratio etching of large number of layers and its control
- High volume manufacturing requires new etching equipment and techniques for scaling to high number of layers

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# Leadership Expected to Continue into 3D NAND



\* Estimates based on analysis of published 3D-NAND architectures

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# Key Takeaways



We see NAND scaling through 1Z: Ensures cost leadership

BiCS 3D-NAND will provide meaningful cost reduction versus 1Z NAND

3-D ReRAM research ongoing. Potential scaling to sub-10nm. Successor to NAND into the next decade

2D-NAND and 3D technologies will coexist this decade

Our conclusions on 3D-NAND remain the same as discussed on 2013 Investor Day

From 2013 Investor Day, May 8, 2013