

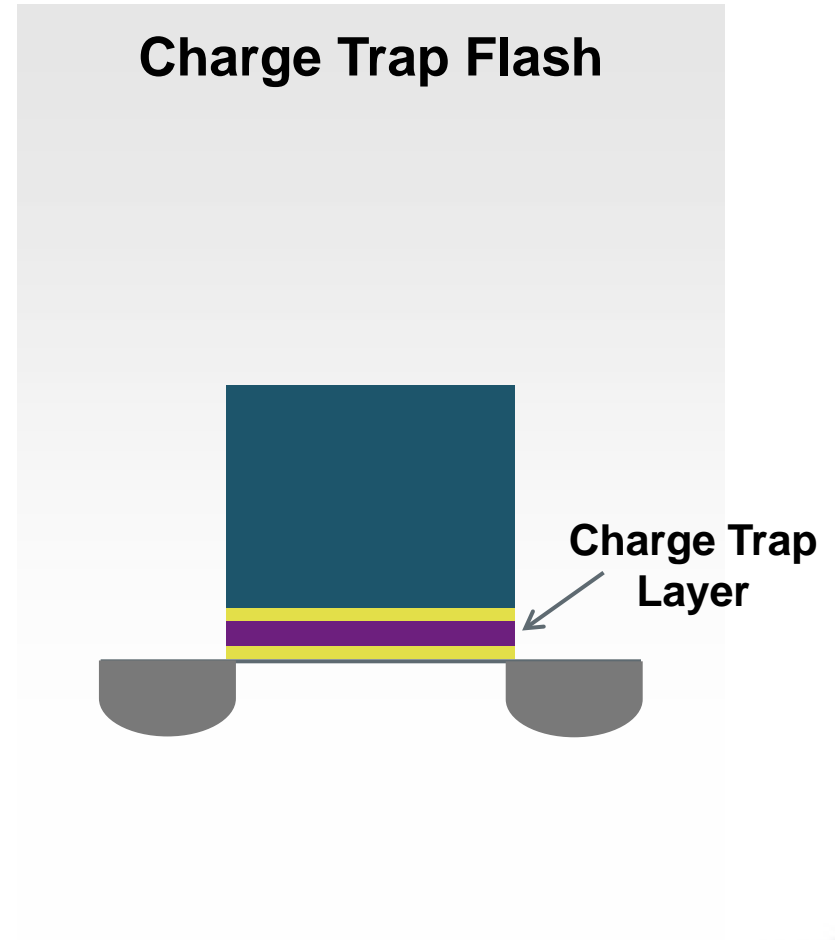
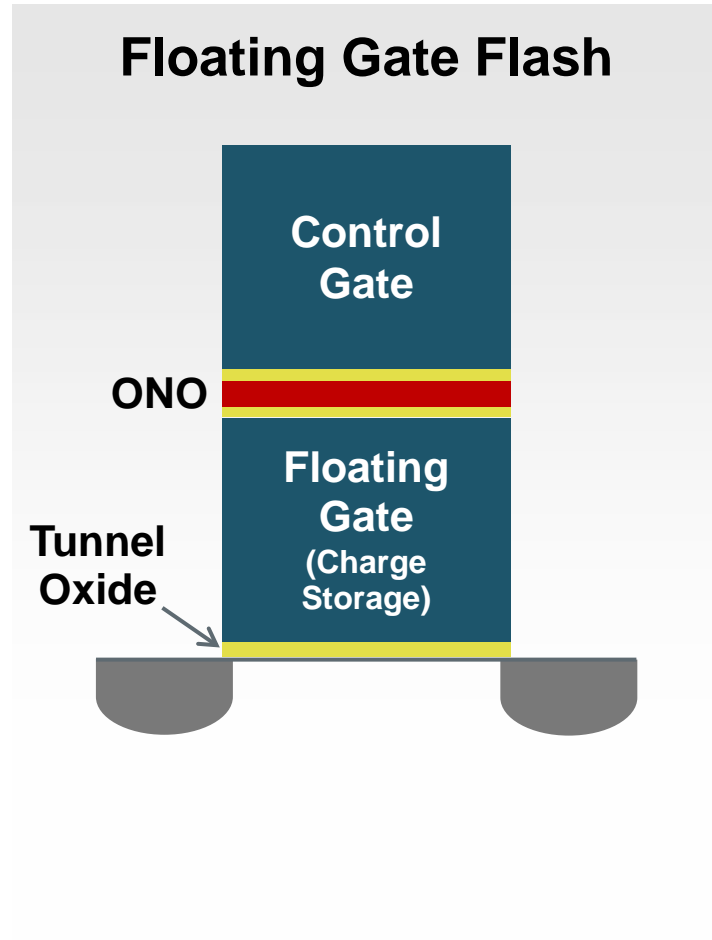


Advancement in Charge Trap Flash Memory Technology

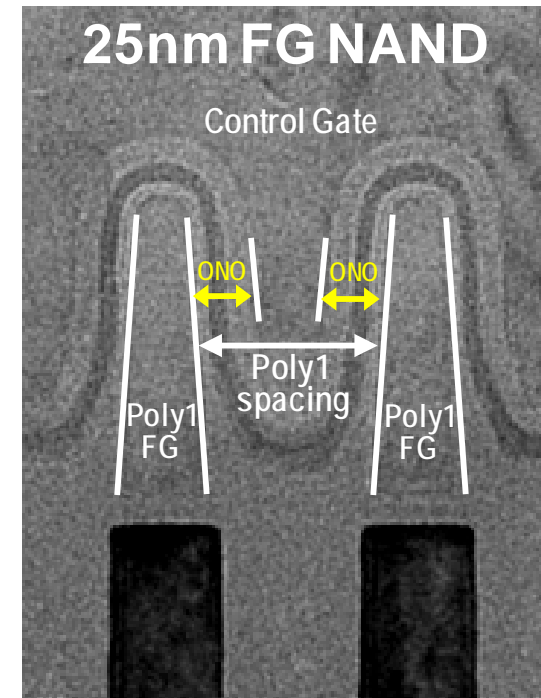
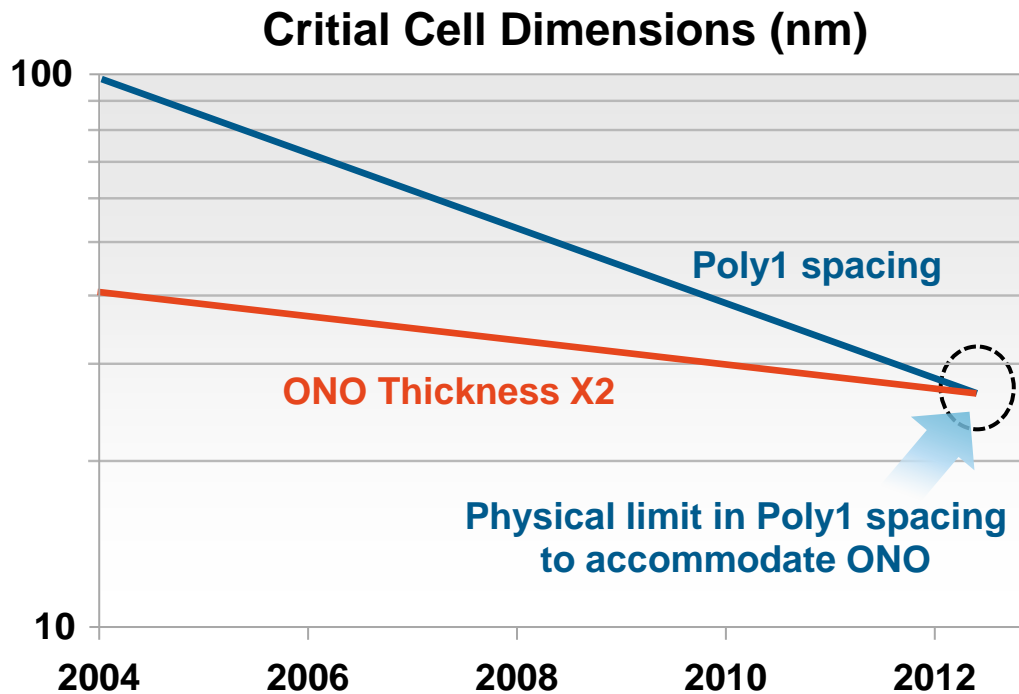
Saied Tehrani, CTO

Flash Memory Summit – August 13, 2013

Why Charge Trap Flash?

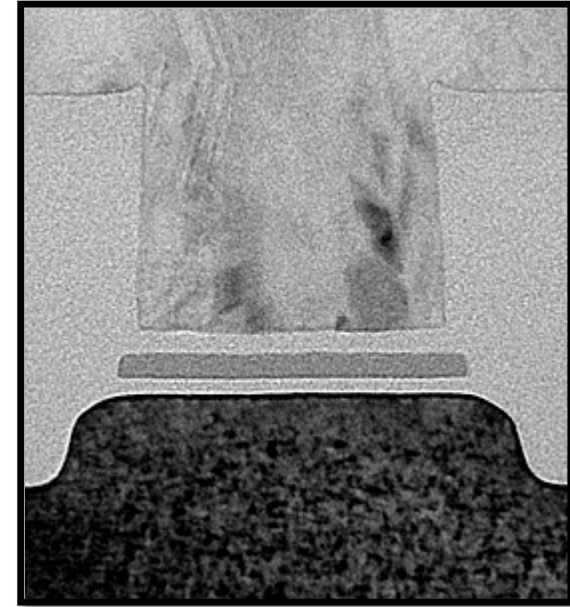
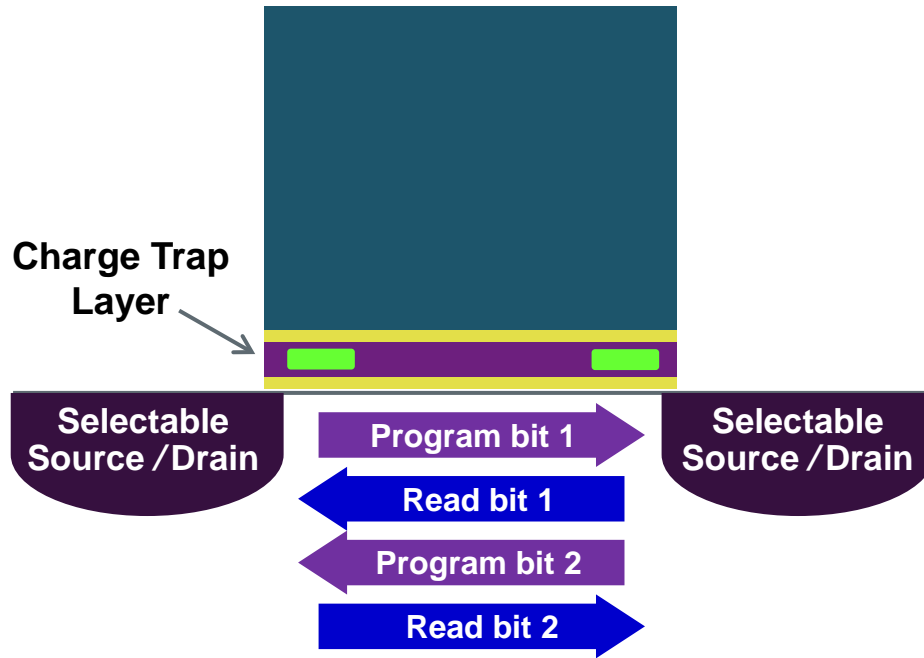


Floating Gate Scaling Limitation



FG NAND Below 20nm

- Difficult to fit ONO inter-poly dielectric in Poly1 spacing
- Cell-to-cell interference becomes increasingly troublesome



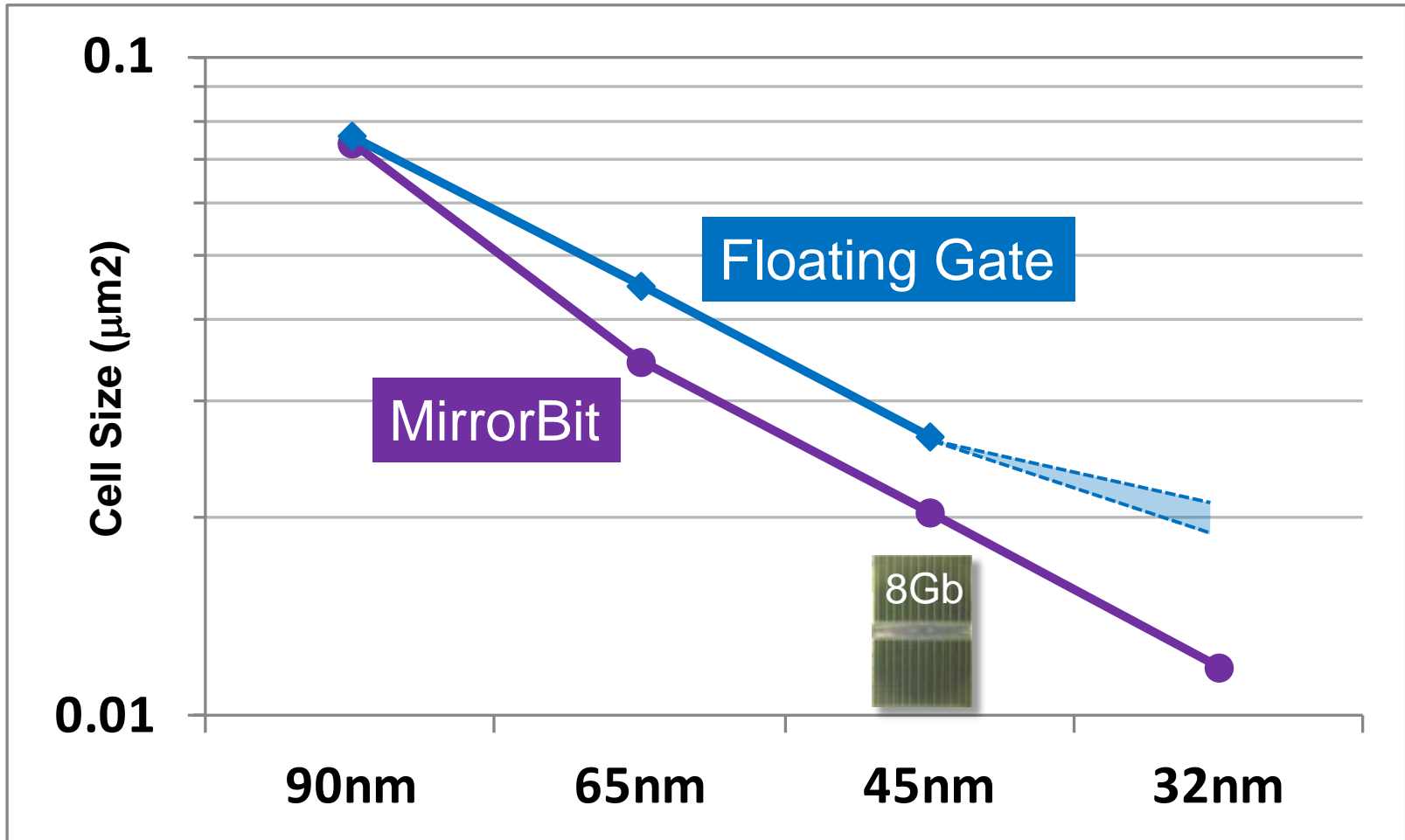
**Non-conducting
Charge Trap Layer**

- Charge stored in two locations in each cell (doubles bit density)

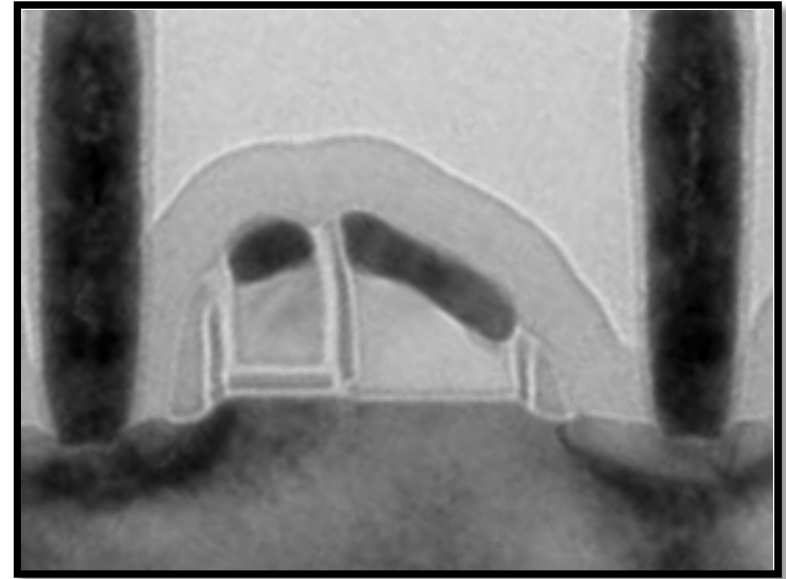
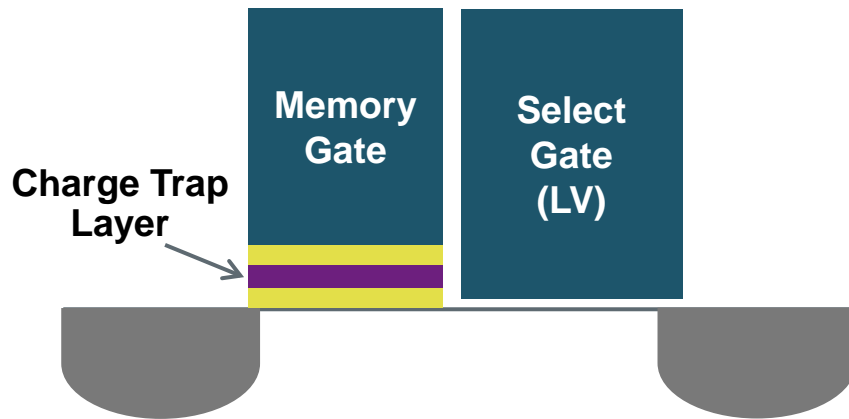
**Planar, Symmetric
Structure**

- Ease of manufacturing and better scalability

MirrorBit Core Cell Scaling Trend



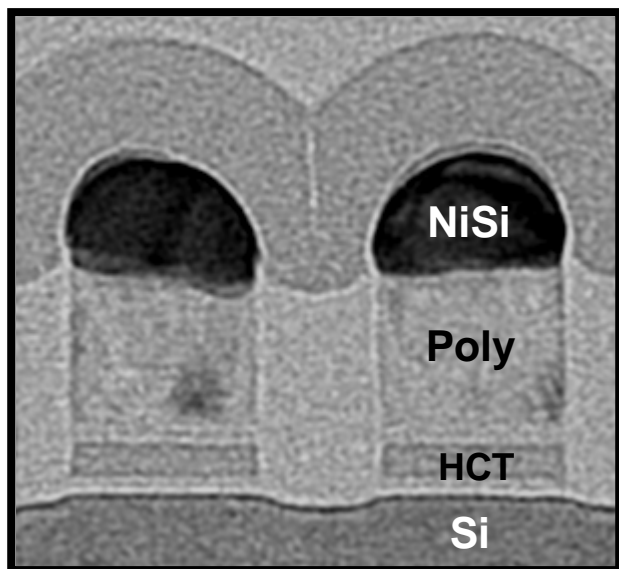
Embedded Charge Trap (eCT)[™] NOR Flash



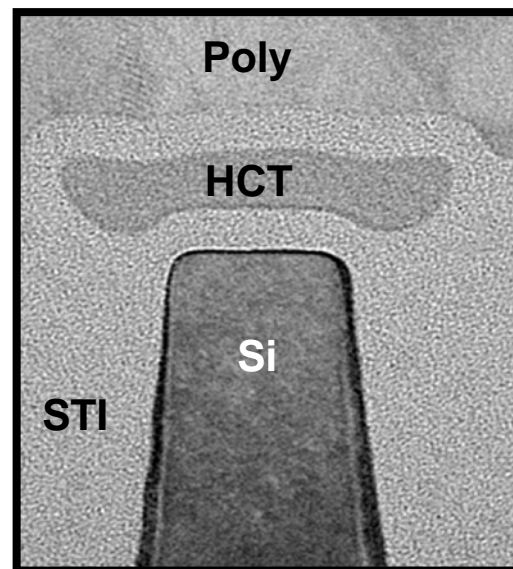
- Based on charge-trap technology used in MirrorBit
- Integrated with low-power Logic process
- Optimized for ultra-fast read, and low power

Heterogeneous Charge Trap (HCT)[™] NAND Technology

Along Bitline

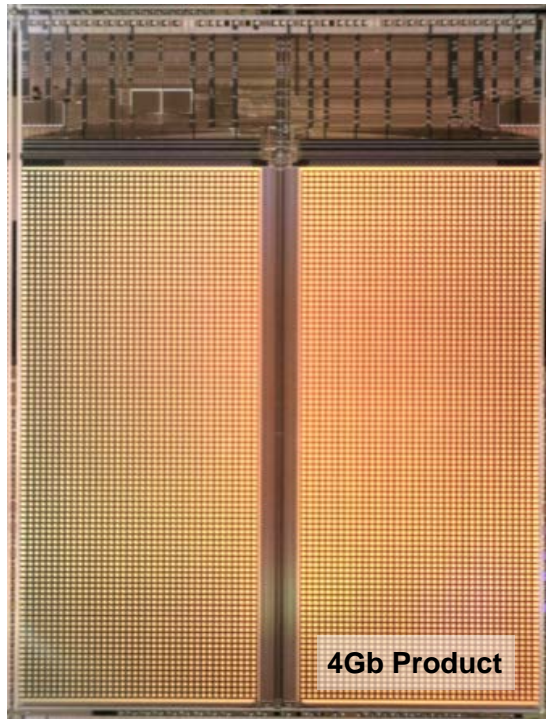


Along Wordline



- HCT film is a multi-layered stack optimized for performance and reliability
- Si content and thickness of each layer within HCT film are critical
- Shape of HCT also optimized for performance & reliability

HCT NAND Product Performance



HCT NAND Memory

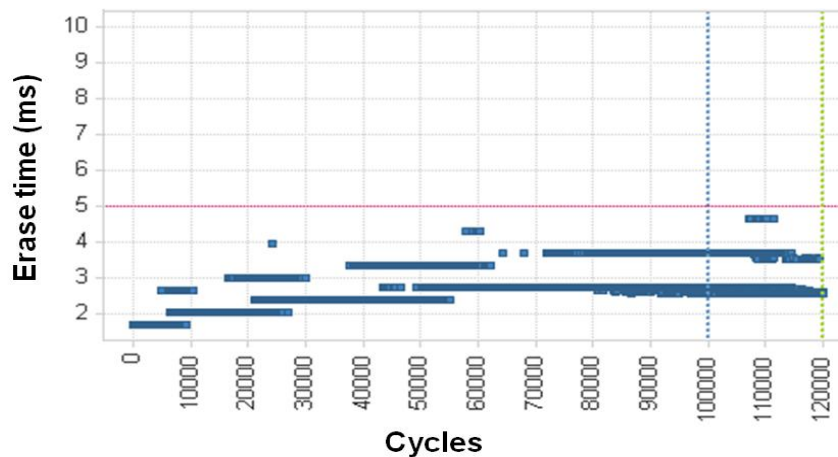
Page Size: 2KB (Main) + 64B (Spare)
Block Size: 128KB + 4KB
Endurance: 100K P/E Cycles
Retention: 10 Years

System Read Performance

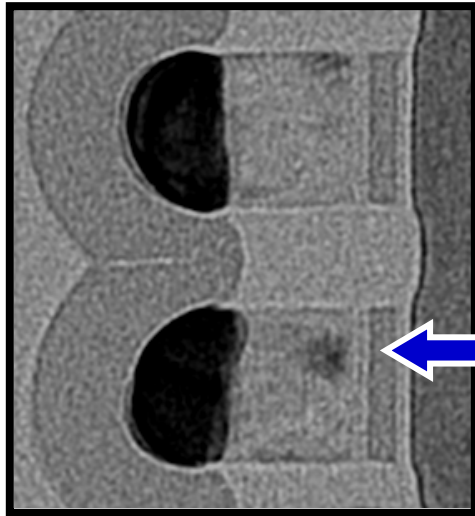
Random Read Time: 25 μ s
Sequential Read (async): 20ns

System Write Performance

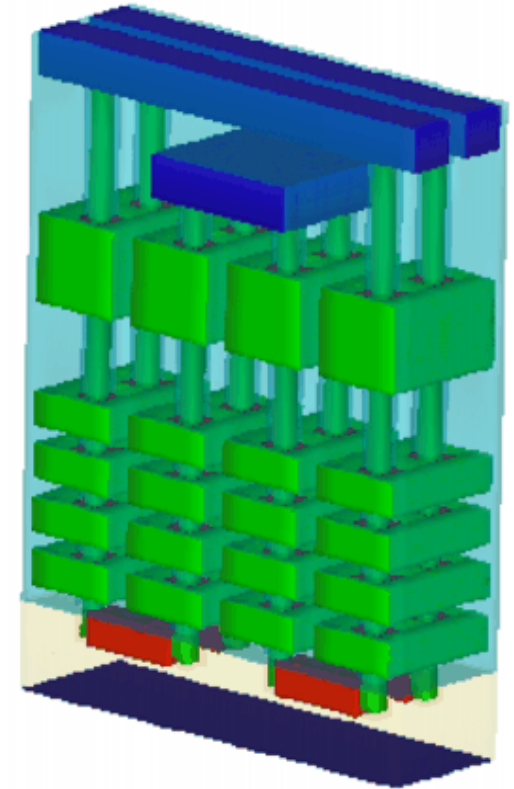
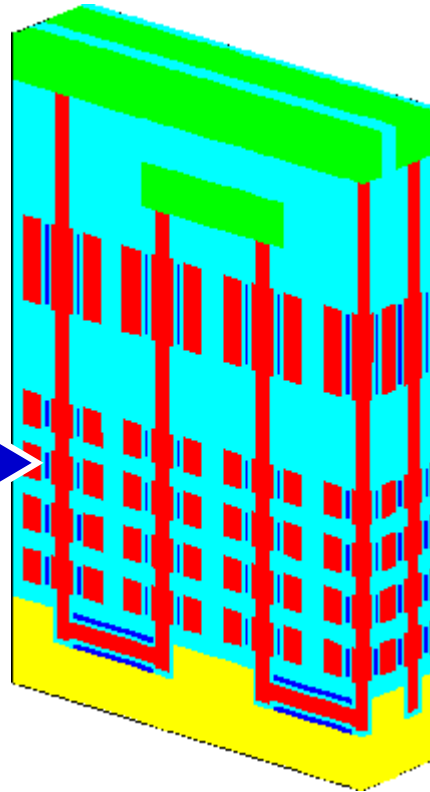
Page Program Time: 200 μ s
Block Erase Time: 5ms



Charge Trap Technology for 3D NAND



Charge
Trap
Layer



Advancement in Charge Trap Flash Memory Technology

- Charge Trap Flash Technology is scalable, reliable, and highly manufacturable
- Standalone NOR Flash Technology based on Charge Trap and 2bits per cell has been in production for >10 years and continues to scale to smaller nodes while maintaining high level of reliability and performance
- Charge Trap embedded Flash Technology integrated with advanced logic for SoC applications is demonstrated, delivering high performance and reliability
- Charge Trap NAND Flash Technology is scalable to <1Xnm and can be extended to 3D



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