Is Your Tester Ready for PCIe Gen 3.0?

A Signal Integrity Tutorial

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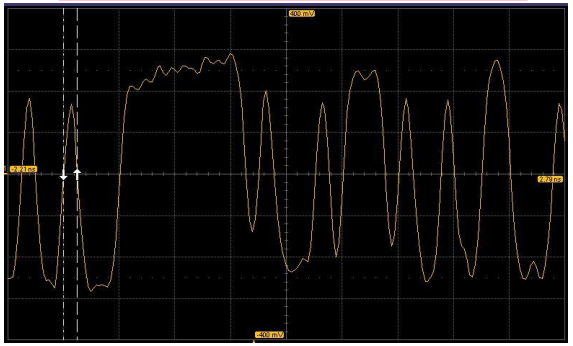
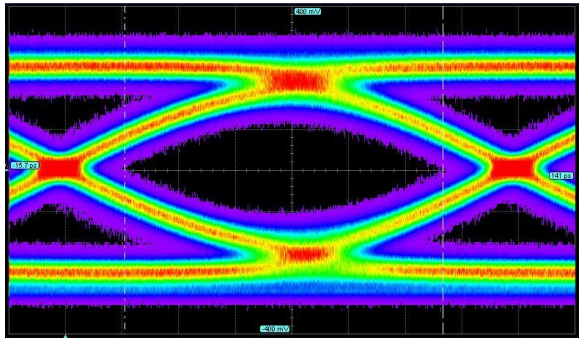
Outline

- How to Measure Signal Integrity
- PCI-SIG Specifications
- Signal Integrity Factors
  - Path Loss (Bandwidth)
  - Reflections
  - Crosstalk
- Conclusions

How to measure Signal Integrity

- Various measures of Signal Integrity
  - Risetime
  - Amplitude
  - Jitter
- The eye diagram encompasses all of the above.
  - PCI-SIG specifies the eye diagram for PCIe





PCI-SIG Specifications

- PCI-SIG determines the PCIe specifications
  - PCI_Express_Base_r3.0
    - Gives *component* specifications.
    - Volts and ps are at the chip package pins.
  - PCI_Express_CEM_r3_0
    - Card Electromechanical specification.
    - Compliance eye diagrams must be met for both the add-in card and a system board at the PCIe connector.
    - Tester is a system board.

Signal Integrity Factors

- Tester signal integrity challenge
  - Long signal paths compared to a motherboard
- Good signal integrity at the DUT requires control of:
  - Path Loss (Bandwidth)
  - Reflections
  - Crosstalk

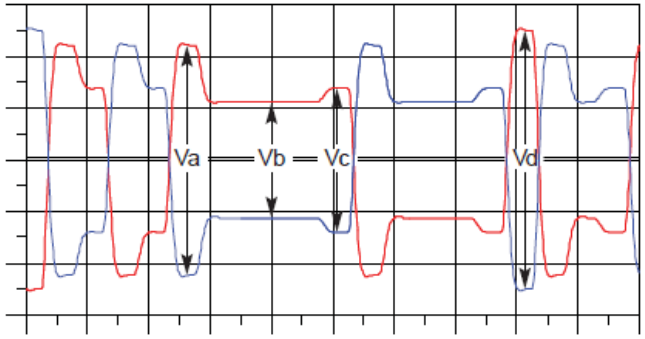
Path Loss (Bandwidth)

- Path Loss (Bandwidth)
  - Focus on losses at data rate / 2
  - De-emphasis, Pre-shoot, and Receive EQ make up for part of the signal loss.

Bandwidth

Attenuation marked at 4GHz.

De-emphasis and Pre-shoot

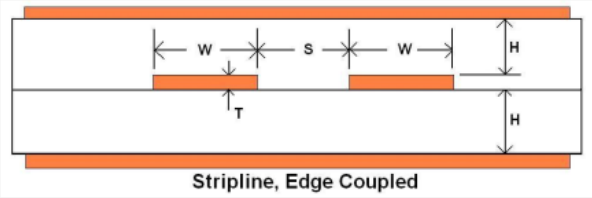


De-emphasis = $20\log_{10}$ Vb/Va
Preshoot = $20\log_{10}$ Vc/Vb
Boost = $20\log_{10}$ Vd/Vb

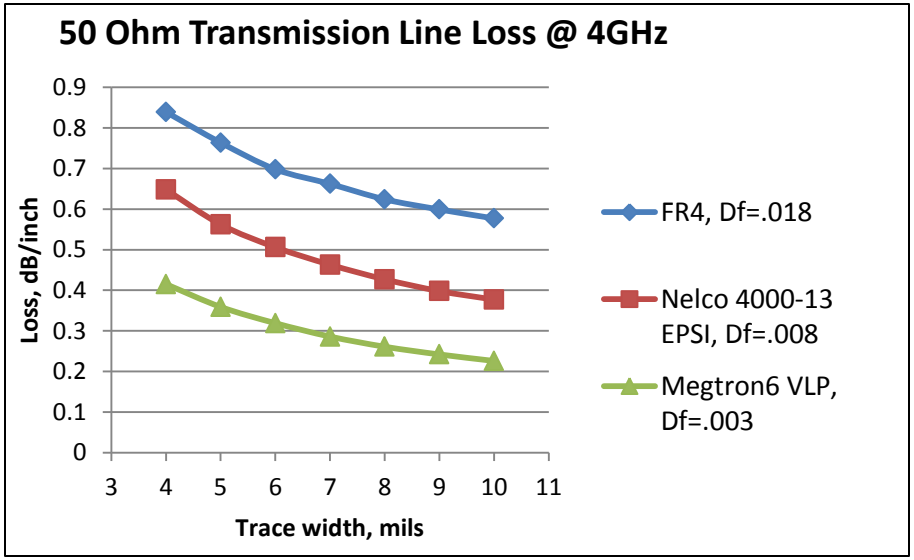
Source: Figure 4-42, PCIe Base Spec.

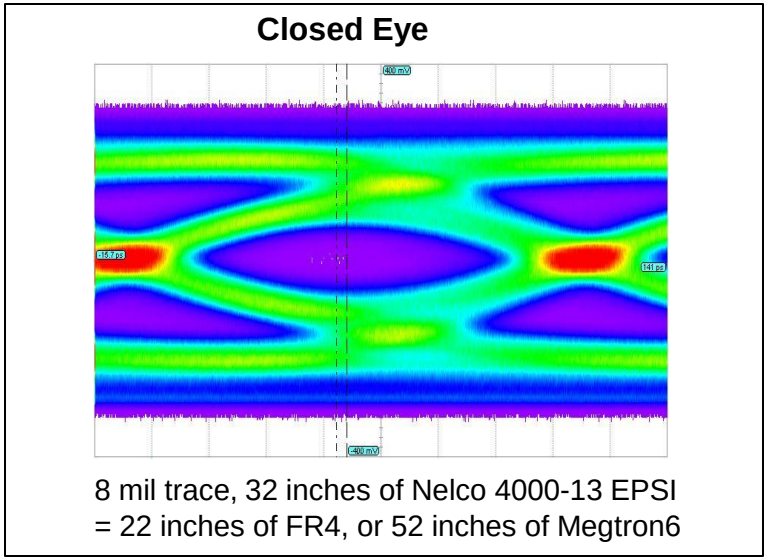
Path Loss (Bandwidth)

- PCB losses
  - Trace width and surface roughness (ohmic loss)
  - Dielectric loss (loss tangent, tan δ, Df)



Geometric scaling produces equal impedance

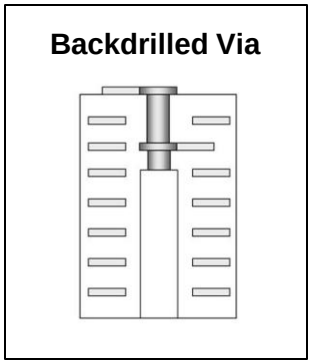




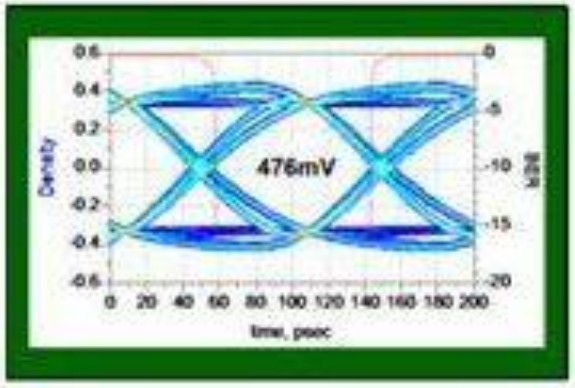
8 mil trace, 32 inches of Nelco 4000-13 EPSI
= 22 inches of FR4, or 52 inches of Megtron6

Reflections

- Reflections occur at impedance discontinuities.
  - Connectors
    - Often capacitive. 85 ohms helps.
  - Stubs
    - Vias - must be blind or backdrilled



A



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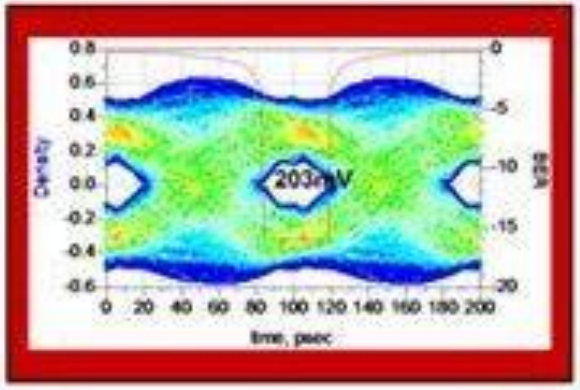


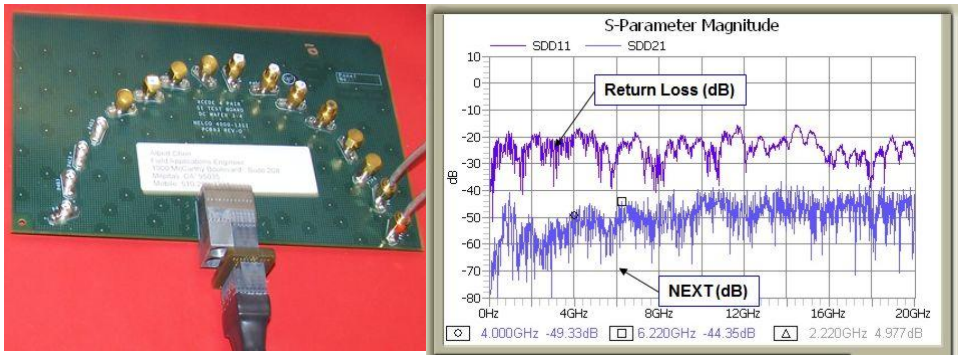
Eye Diagrams of a 10Gbps signal, A) with backdrilled vias, and B) without backdrilling.

Source: [1] and [2]

Crosstalk

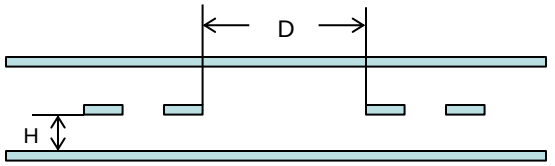
- Crosstalk
  - Connectors
    - Separate Tx and Rx
    - Ground shield or ground pins between signal rows
  - PCB Traces
    - Inter-differential pair distance

Connector Test



Connector test board shows -49dB crosstalk at 4GHz

Inter-pair spacing

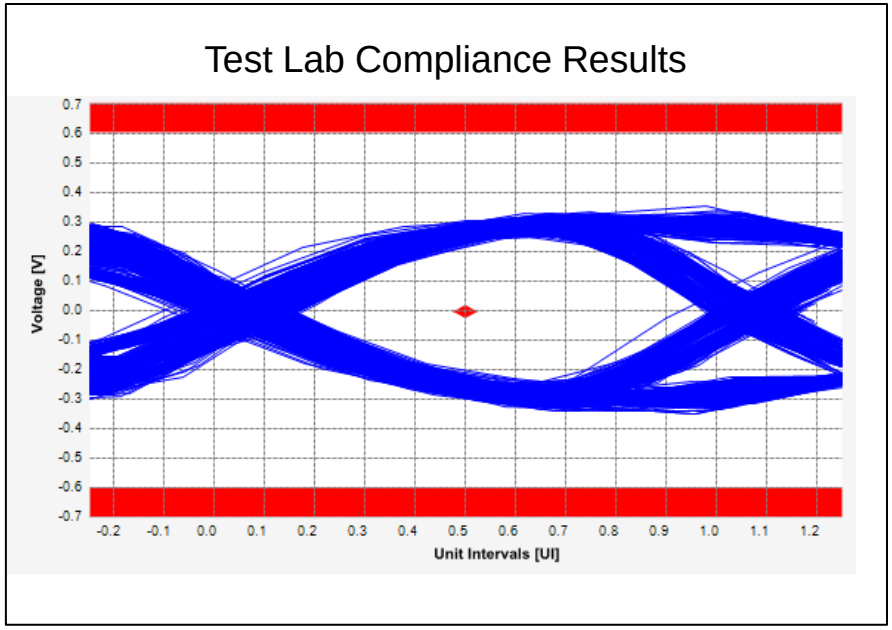


D = ~ 4 to 5 times H for > -40dB crosstalk.

Conclusions

- Careful design leads to good signal integrity results.

AT System



Footnotes

- [1] Bert Simonovich, “Bert's Practical Design Notes: An Overview of Vias”, http://www.pcbdesign007.com/pages/columns.cgi?clmid=61&artid=82810
- [2] Bert Simonovich, “Bert's Practical Design Notes: The "Stubinator" vs. Back-Drilling”, http://www.pcbdesign007.com/pages/columns.cgi?clmid=61&artid=83398