FPGAs and NVM types

PLD's Have Evolved!

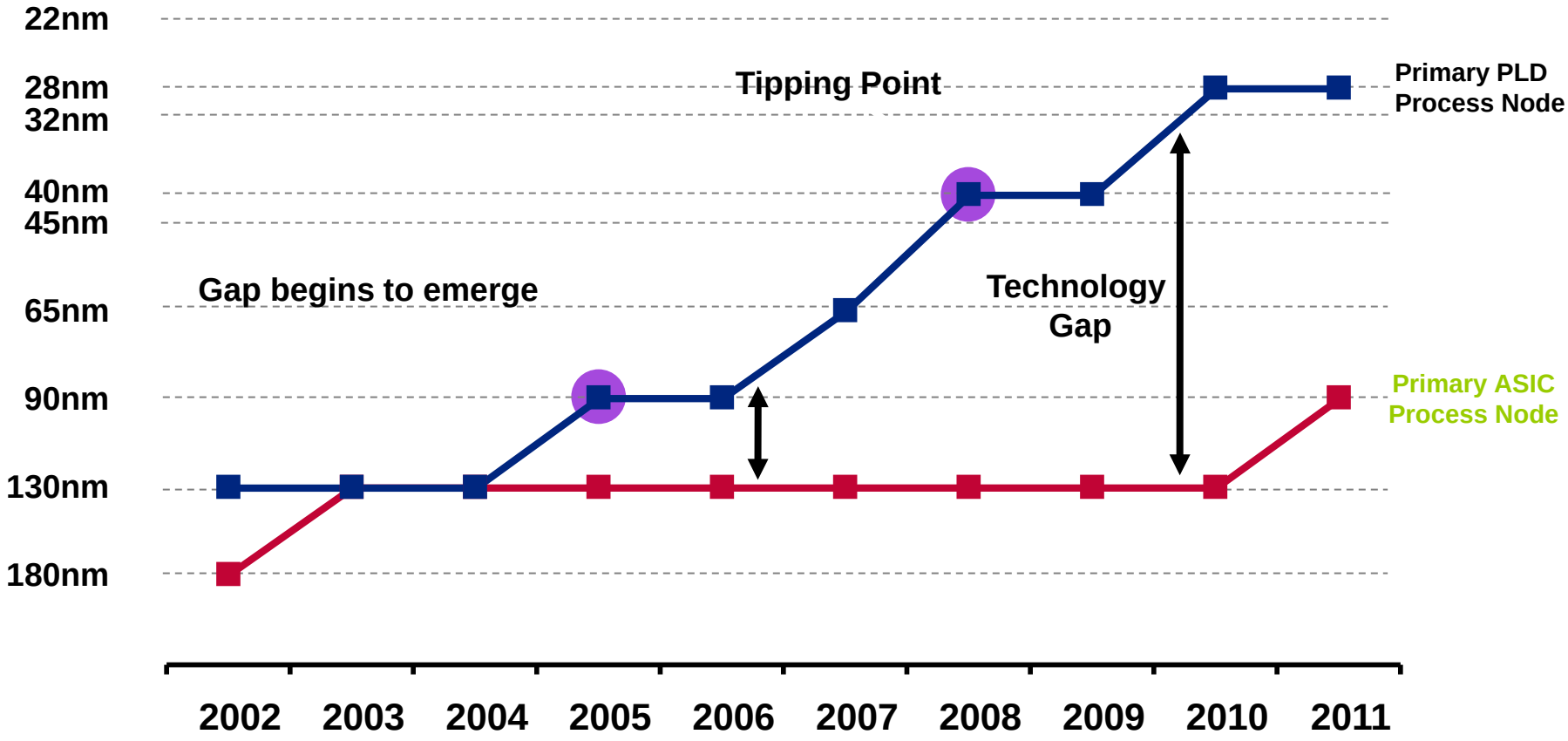
The Lab

Prototyping
1-250 units

The Data Center

Production
10ku-1Mu

PLD Tipping Point vs. ASICs



PLDs Outstripping Traditional ASICs in Technology and Total Cost of Ownership

Source: Altera; data applies to new design starts.

Flash Memory SUMMIT

ALTERA®

POWERING YOUR INNOVATION

MAX® Series	Cyclone® Series	Arria® Series	Stratix® Series	ENPIRION
CPLDs	***FPGAs***	***FPGAs***	***FPGAs***	***PowerSoCs***
Lowest Cost, Lowest Power	***Cost/Power Balance SoC & Transceivers***	***Mid-range FPGAs SoC & Transceivers***	***Optimized for High Bandwidth***	***High-efficiency Power Management***

RESOURCES

Embedded Soft and Hard Processors

Nios® II

ARM®

Design Software

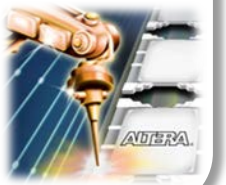
QUARTUS® II

DSP Builder

Development Kits

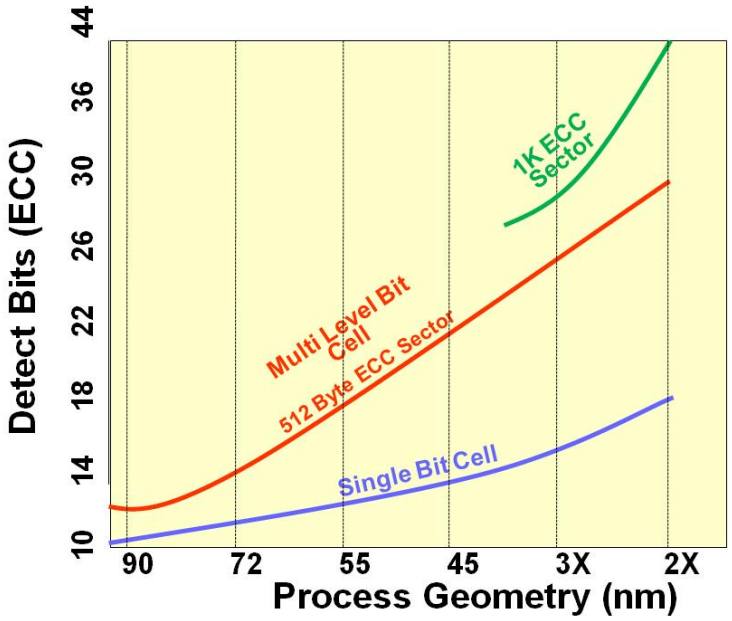
Intellectual Property (IP)

- Industrial
- Computing
- Enterprise



Flash Cache Challenges & Evolution

- Ongoing Challenges
  - Error correction cost increasing
  - Limited endurance (lifetime writes)
  - Slow write speed
  - SATA/SAS SSD interface is slow
- Storage over PCIe electricals
  - Faster than current SAS & SATA
  - SATA Express
  - NVM Express
  - HP SCSI Express
- Emerging flash technologies
  - Higher IOPS- more PCIe BW
  - **MRAM (Magneto Resistive)**
  - PRAM (Phase Change Memory)
  - RRAM (Resistive)
  - NRAM (Carbon Nanotube)



Flexibility Required to Support Emerging Memory Technologies

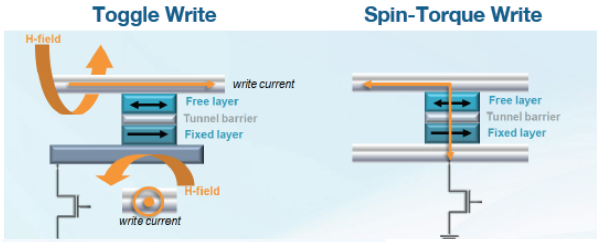
Spin-Torque MRAM – Next generation MRAM

Current generation MRAM uses a magnetic field for switching

Limits scaling due to constant magnetic field

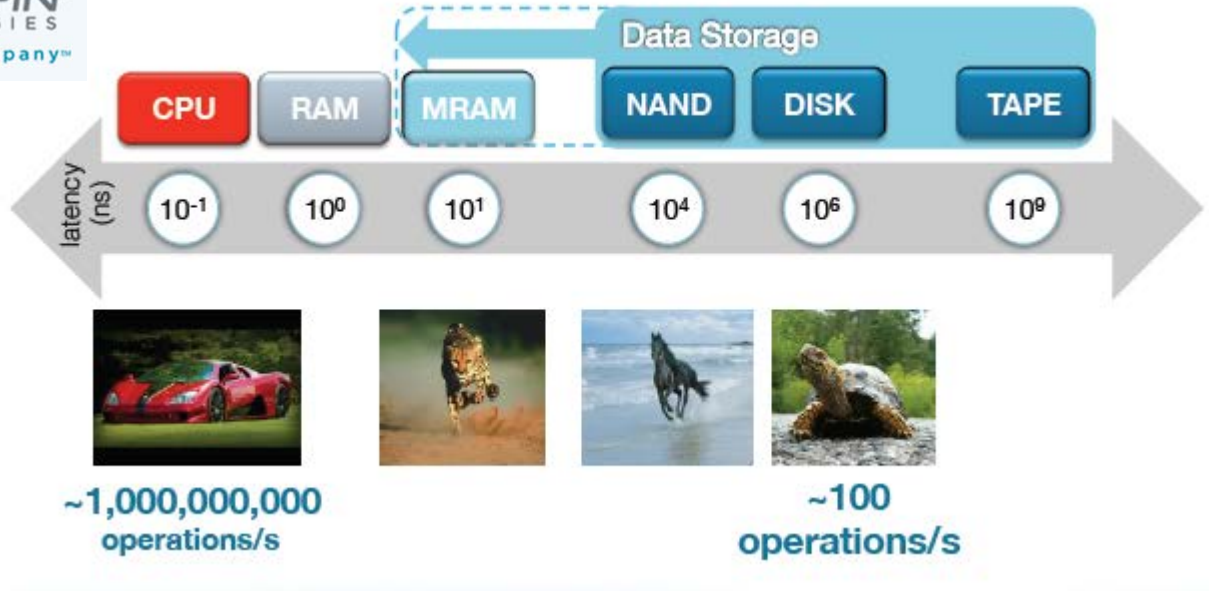
Next generation MRAM enables scaling to Gb densities

Everspin on track to deliver industry's first ST-MRAM



EVERSPIN TECHNOLOGIES
The MRAM Company™

- HDD leveraged as capacity optimized data storage
  - *Benefits : Lowest cost per GB/TB for data storage*
  - *Challenges: Random access, active power & power fail*
- NAND SSD leveraged as performance optimized storage
  - *Benefits : More IOPS, reduced latency & less overall power*
  - *Challenges: Write latency & variability, endurance, power fail*
- ST-MRAM leveraged as non-volatile buffer/cache for storage
  - *Benefits : DRAM like access, unlimited endurance & power fail*
  - *Challenges: New storage architecture, density & cost scaling*



Enabling Technology- Programmable Logic Devices

- Design Logic support
  - Increasing densities to support system on chip (SOC) programmability
- Increased Computational Performance
- Reduced Power
  - Intelligent power management
  - Hardened IP blocks
- High Speed Serial Interface Support
  - Embedded Transceivers
- Supports multiple memory types in the storage hierarchy