NAND Reliability Improvement with Controller Assisted Algorithms in SSD

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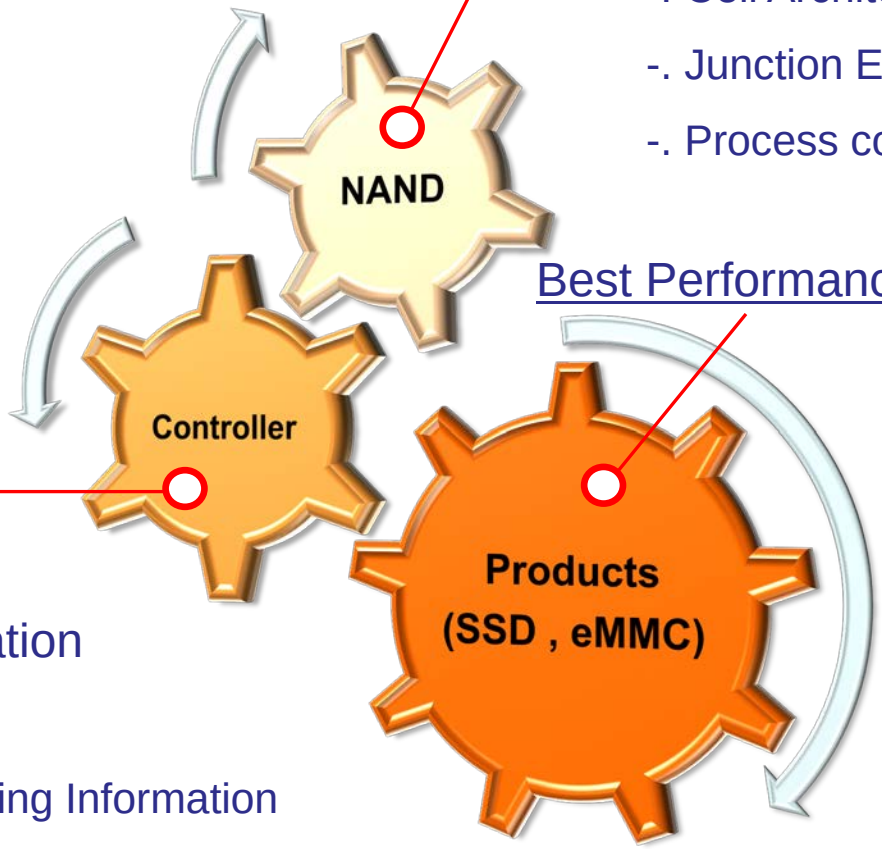
Introduction

Si Process Optimization

-. Cell Architecture.

-. Junction Engineering.

-. Process control.



Best Performance and Reliability Products

Controller Application

-. FTL

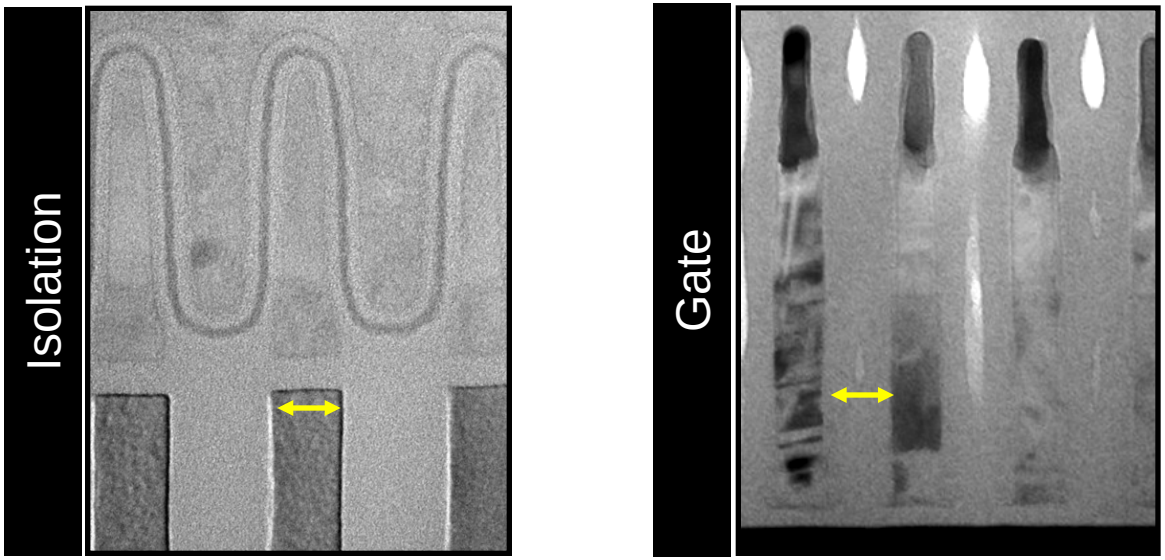
→ Using wear- leveling Information

→ Variable Program /Erase /Read Condition

Scaling Barriers in NAND Flash

Geometry	Small Coupling Ratio, Small On Current
Narrow Operating Window	Interference, Disturbance, P/E cycling Stress
Process Sensitivity	Less Tolerance in Process Variation

[NAND Flash Structure]



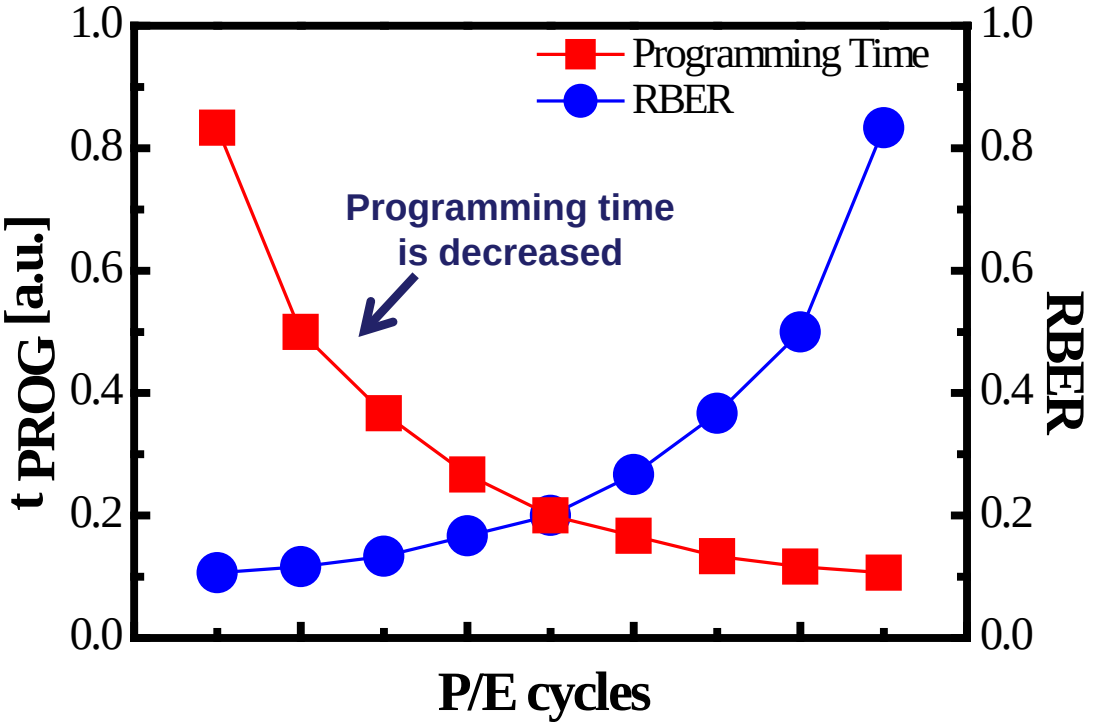
Program Operation

- ISPP Operation

-. Controller assisted ISPP algorithms as P/E cycles proceeds.

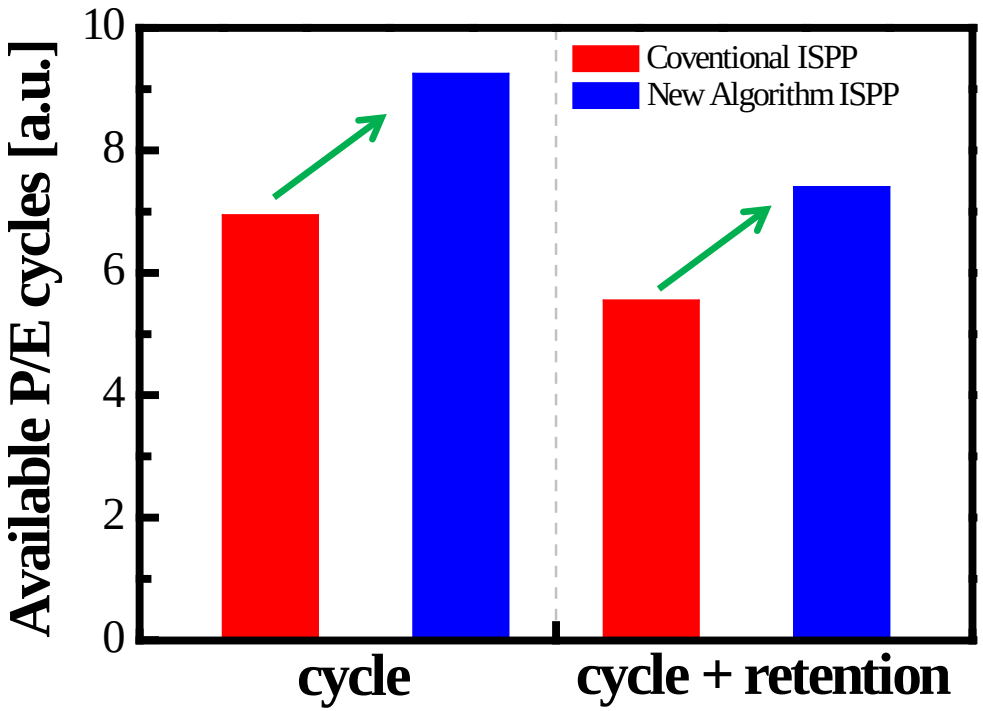
Performance and Reliability Characteristics as P/E Proceeds.

- After P/E cycling, cell Vth is rapidly increased and Vth distribution is widened, which means that performance of NAND flash is enhanced but reliability is degraded. We could transfer sufficient program performance margin to insufficient reliability margin as P/E cycle proceeds. Consequently, we have devised a method that can improve reliability by utilizing such characteristics.



New Algorithms ISPP Reliability Results

- By using the controller assisted new ISPP operation which modify the program condition, tracking the cell program, we improved cycle and retention characteristics in new ISPP than that of conventional ISPP operation.



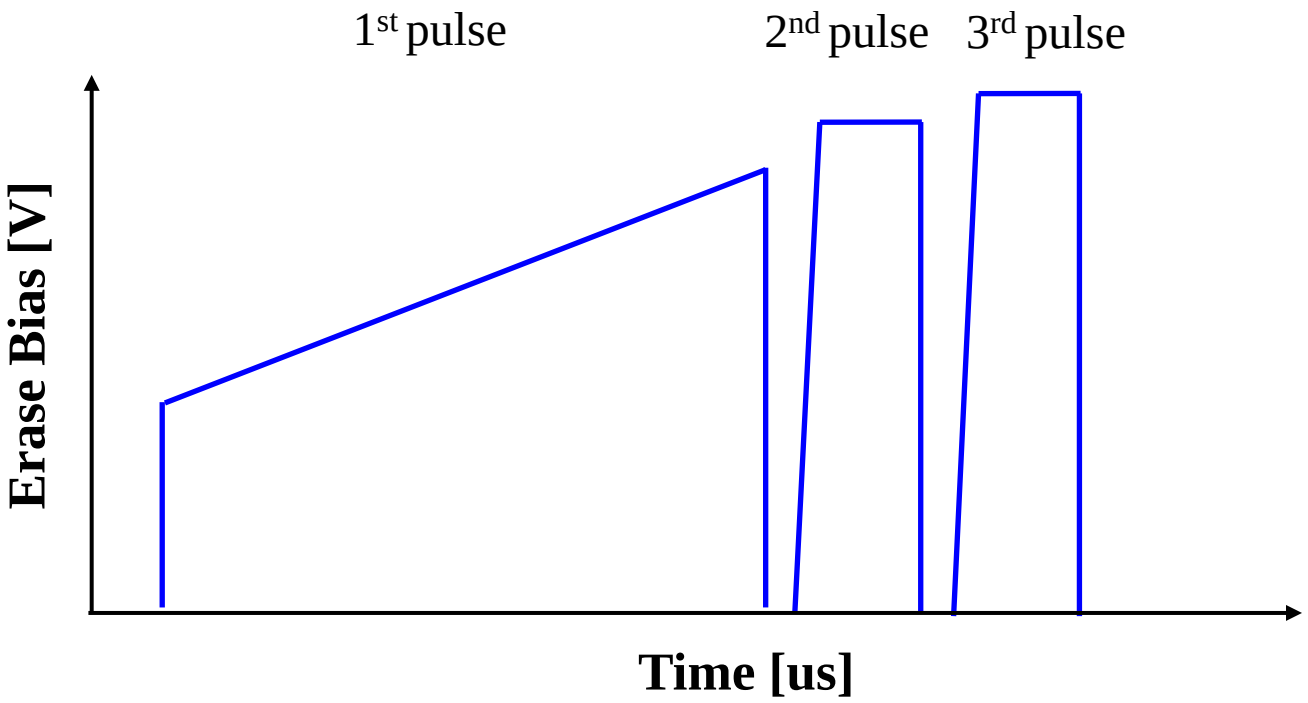
Erase Operation

- Erase Pulse Control
- Intelligent ISPE
- Variable Erase Verify

Erase Pulse Control

- Erase pulse shapes have been changed to enhance reliability and satisfy erase time requirement in erase pulse steps.

→ We could implement new erase operation that can reduce the FN stress and achieve fast erase operation simultaneously. The 1st erase pulse has graded slope and 2nd erase pulse has steep slope as in figure

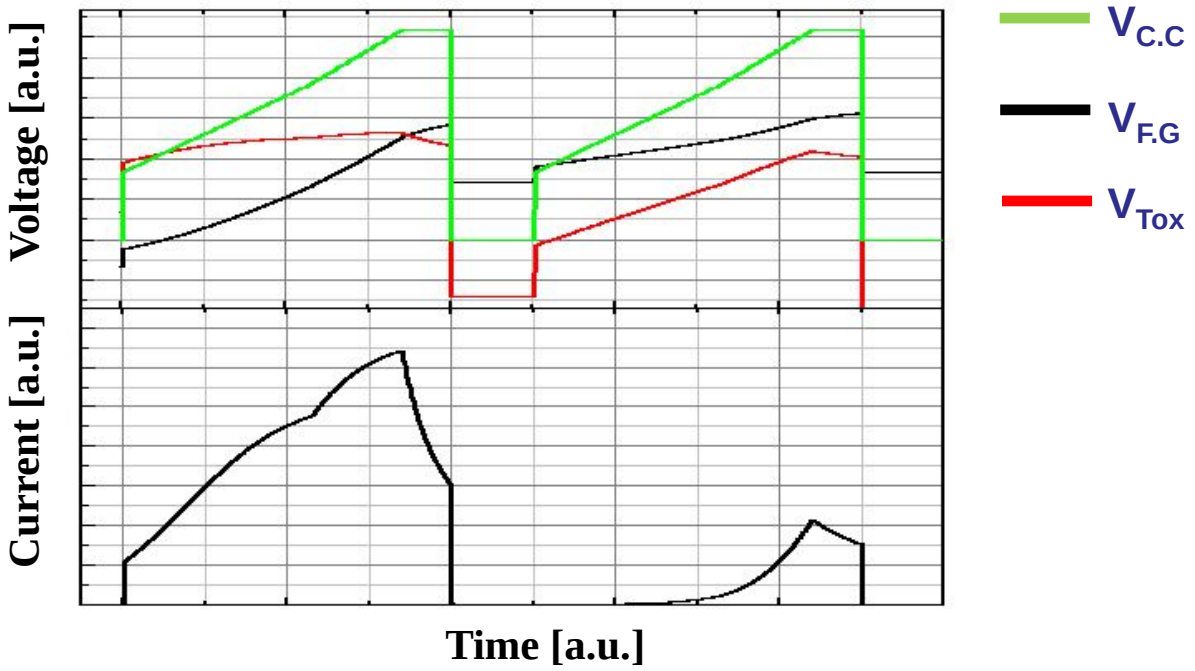


Erase Pulse and FN Current

- Larger FN current flows during 1st ISPE pulse step and its graded erase pulse slope relieve the FN stress in tunnel oxide. Since potential of floating gate rise after 1st ISPE pulse step, FN current decrease in low potential region of 2nd ISPE pulse.

→ Even if 2nd step pulse slope is changed into steep, it does not affect cell reliability.

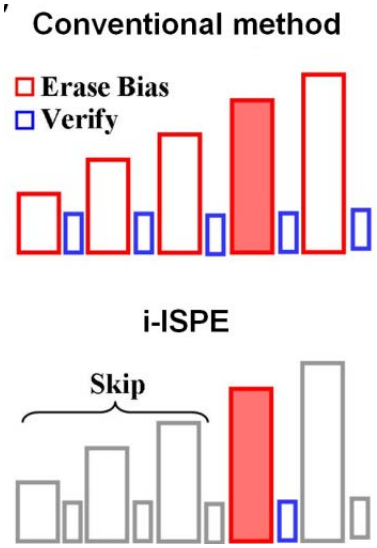
< Erase Pulse and FN current using HSPICE >



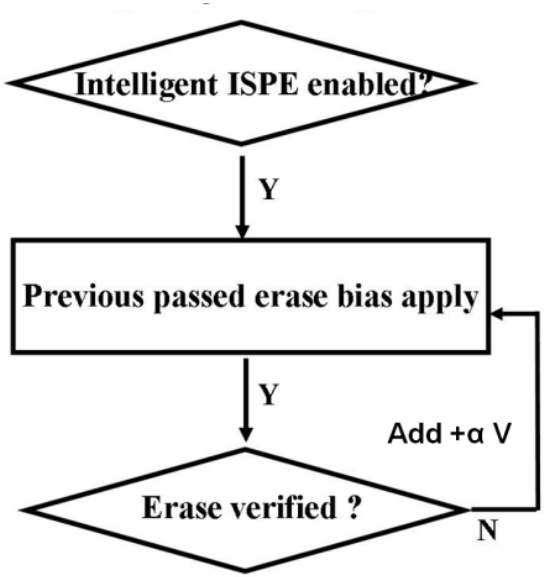
Intelligent ISPE Control (B.J. Park , 2012 FMS)

- Intelligent ISPE ; eliminating the redundant erase stress by using and applying the ISPE bias of previous EW cycles

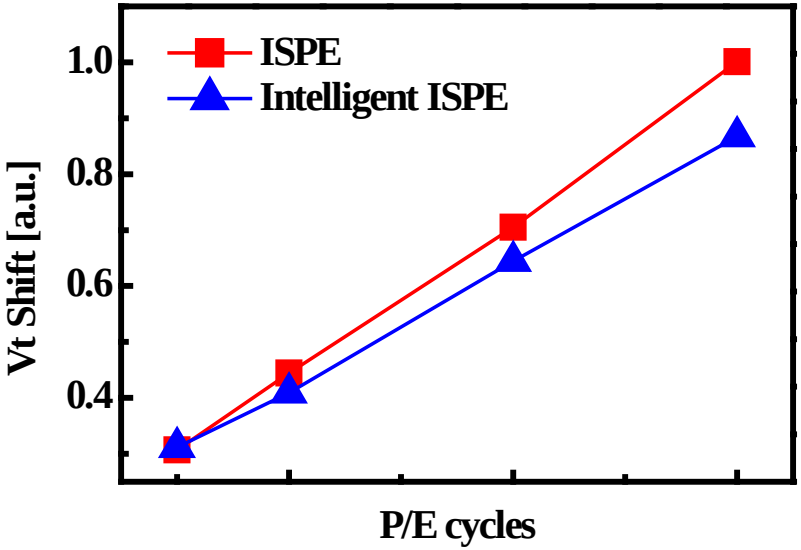
→ Erase operation can be finished within only one or two pulses even after P/E cycles.



(A) Schematics Diagram



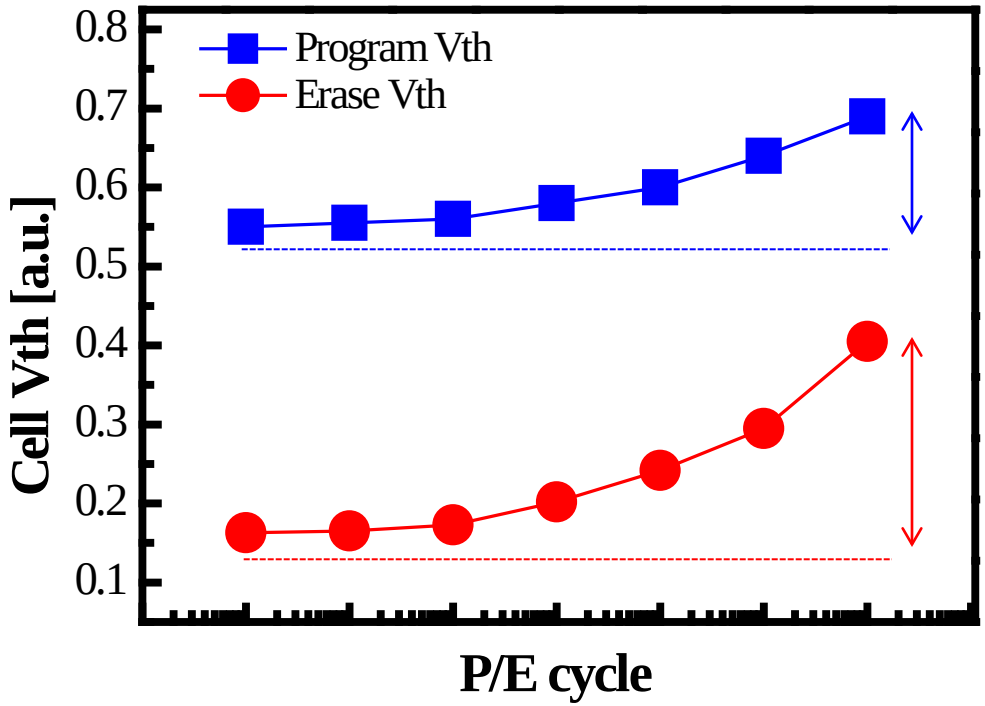
(B) State-Machine



(C) Vt shift comparison between conventional ISPE and I-ISPE

Variable Erase/Program Verify Level in P/E Cycle Nodes

- NAND Cell degradation characteristics can be beneficially used because erase verify, program verify and read level can be manipulated as P/E cycles. Especially, erase verify level should be delicately controlled since erase stress is the major factor for cell degradation.

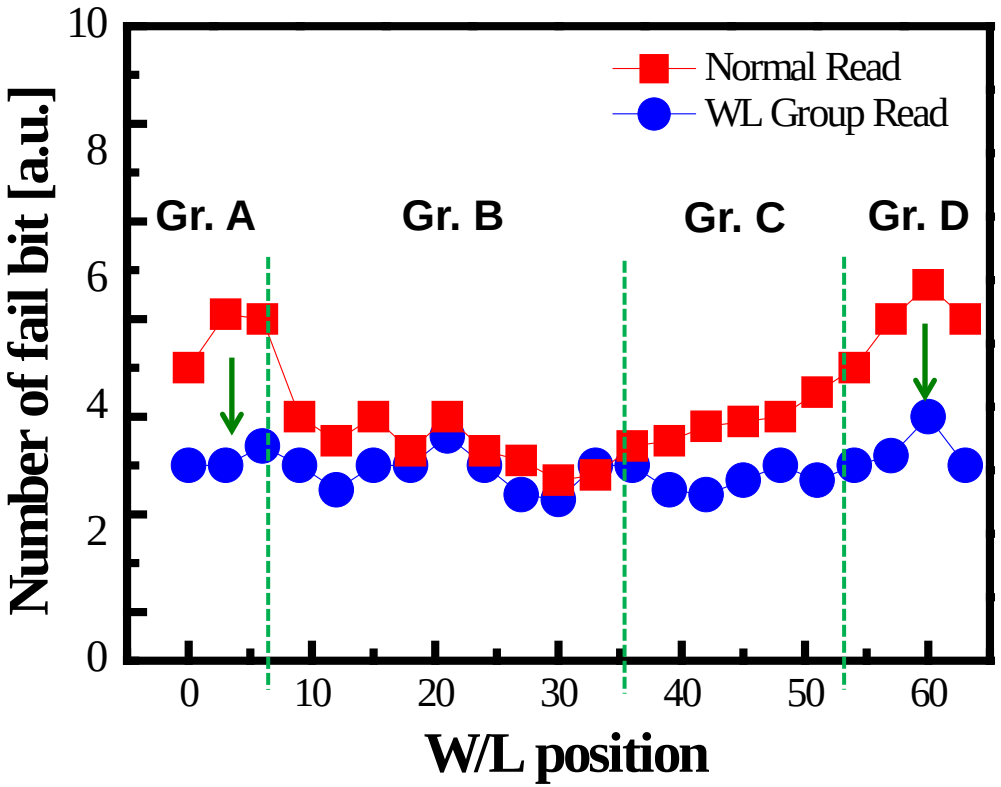


Read Operation

- Selected W/L Group Read
- Unselected W/L Group Read
- Read Scrub / Read Refresh

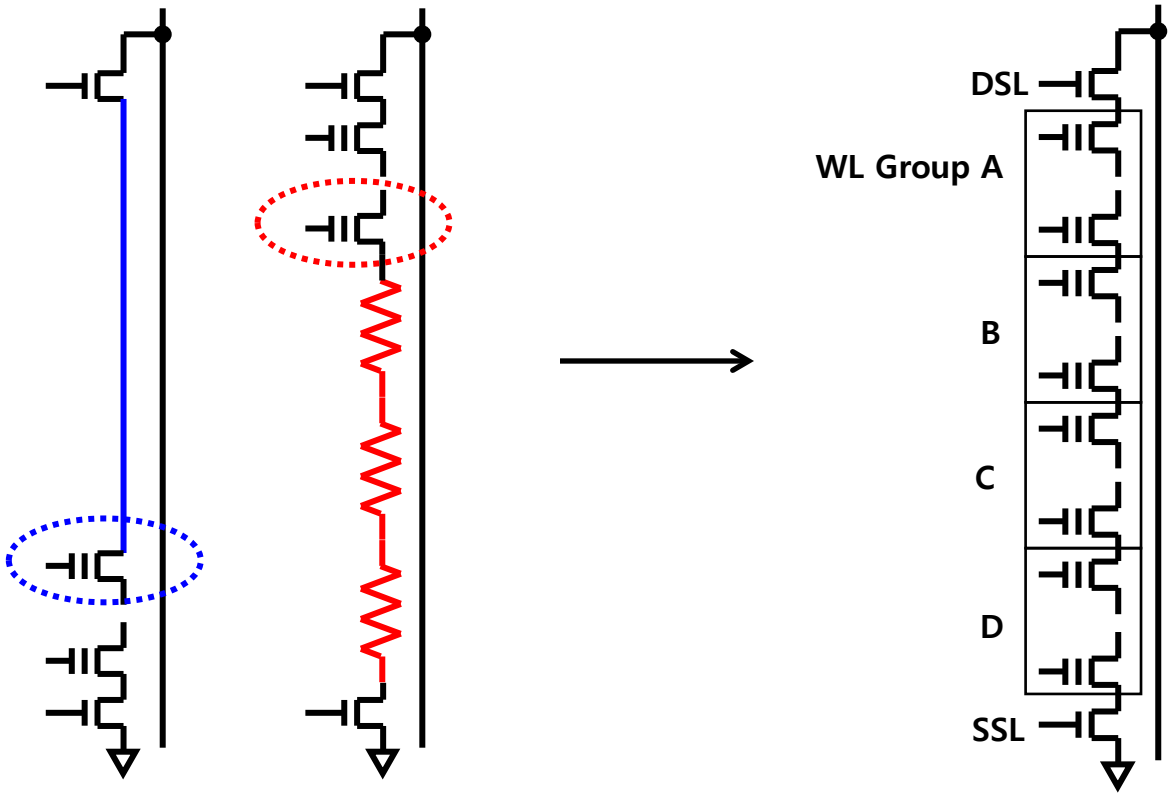
W/L Group Operation : Selected W/L

- As scale down, cell uniformity within a block is being worsened continuously. To overcome these ones, W/Ls are divided into several groups and different operation biases are applied for each W/L groups with controller assistance or NAND itself.



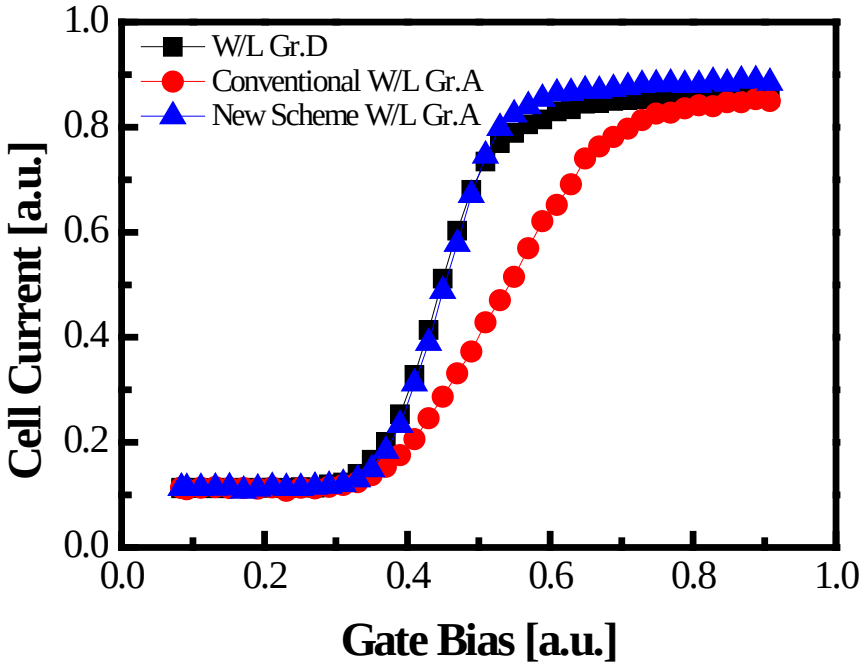
W/L Group Operation : Unselected W/L

- With increasing string size, series resistance of cells are also increased. As a result, string current is varied with W/L positions. We could use each different biases for each “W/L Groups” to compensate the variation of the string resistance.



W/L Group Operation : Cell Current

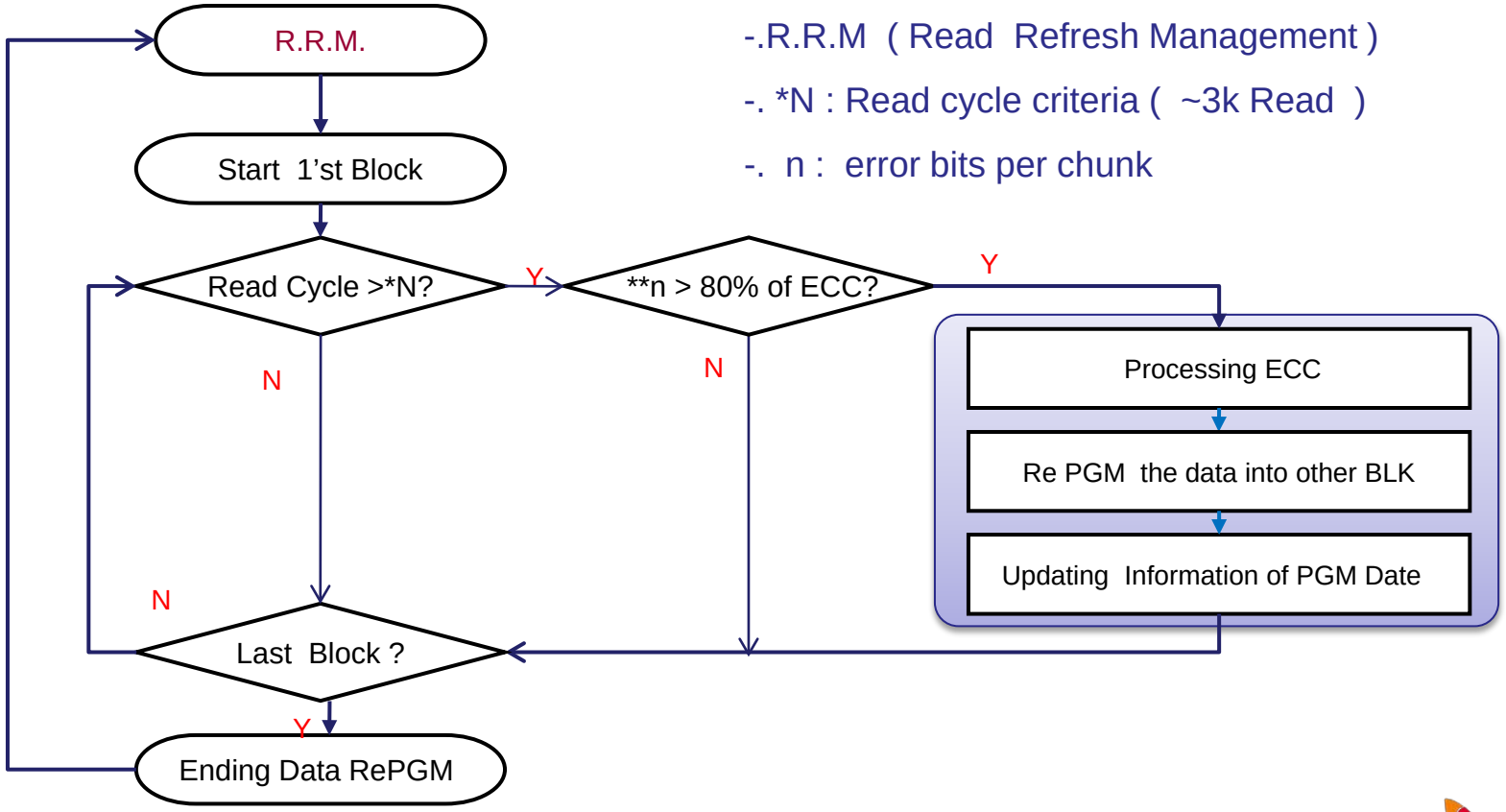
- By using the W/L group scheme, we can make the cell current of “Gr. A”similar to that of “Gr. D”.



Selected W/L	Unselected W/L	Value
W/L Group A	VPASS_A	VPASS_D + α
W/L Group D	VPASS_D	VPASS_D

Read Scrub / Read Refresh

- Read Scrub is used for detecting retention and read disturbance.
- Controller could trace read count using R.R.M., which re-program the block if the number of fail bits is more than 80% of ECC coverage.



-.R.R.M (Read Refresh Management)

-. *N : Read cycle criteria (~3k Read)

-. n : error bits per chunk

Conclusions

- We introduced the controller assisted algorithms that can improve the reliability by utilizing the cell characteristics change.
- In program operation, controller assisted algorithms ISPP was proposed to improve reliability with proper performance.
- In erase operation, Erase pulse control and intelligent ISPE are proposed to reduce the erase stress and enhance erase performance.
- In read operation, bias conditions for each W/L groups are separately controlled to overcome cell uniformity within a block.