Overcoming the Challenges of 10nm-class NAND Flash Memory

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Forward Looking Statement

During our meeting today we will be making forward-looking statements.

Any statement that refers to expectations, projections or other characterizations of future events or circumstances is a forward-looking statement, including those relating to market **demand**, market growth, industry trends, expenses, future memory technology, and technology transitions and future products.

Actual results may differ materially from those expressed in these forward-looking statements due to the factors detailed under the caption “Risk Factors” and elsewhere in the documents we file from time-to-time with the SEC, including our annual and quarterly reports.

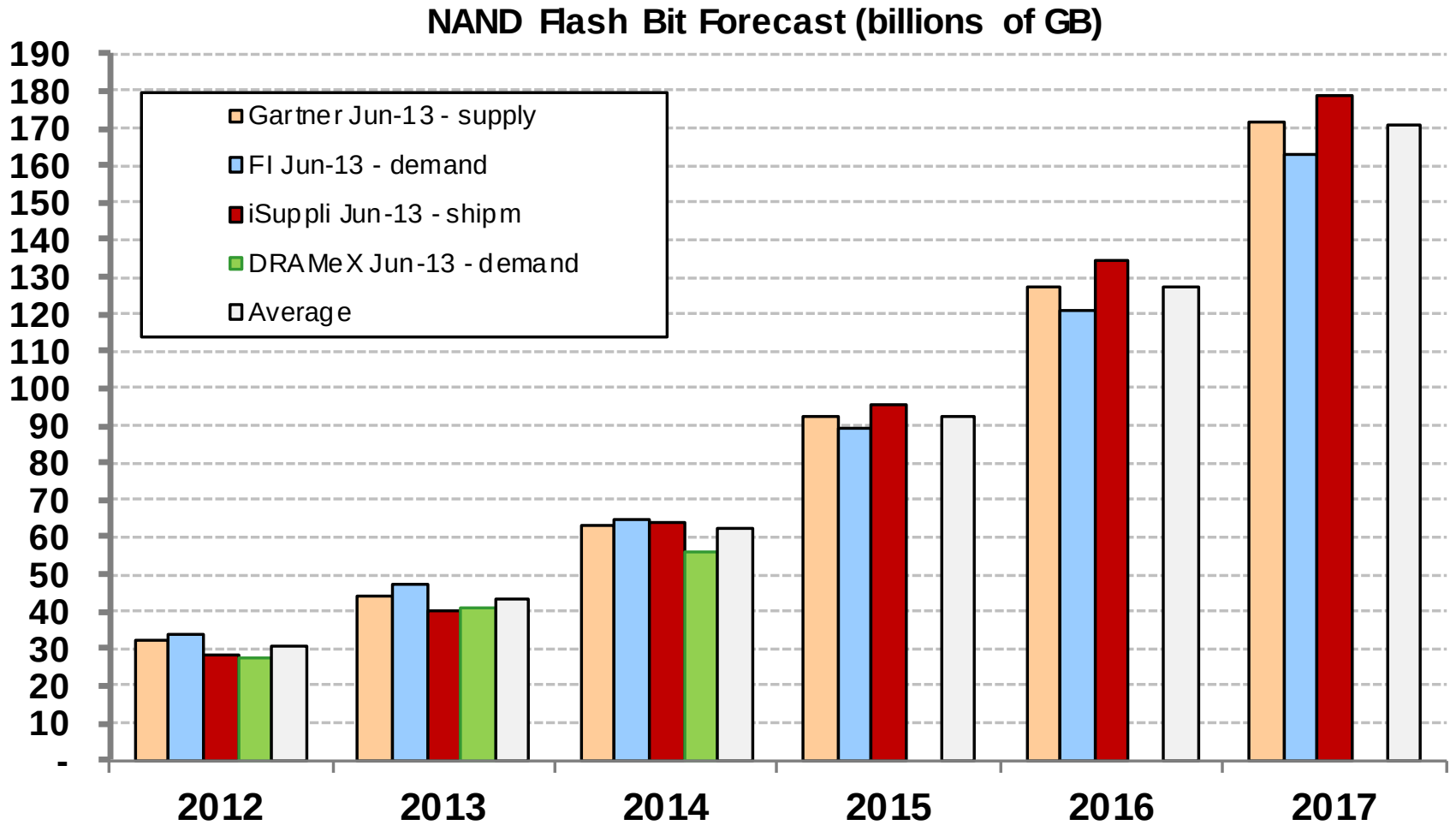
We undertake no obligation to update these forward-looking statements, which speak only as of the date hereof.

Outline

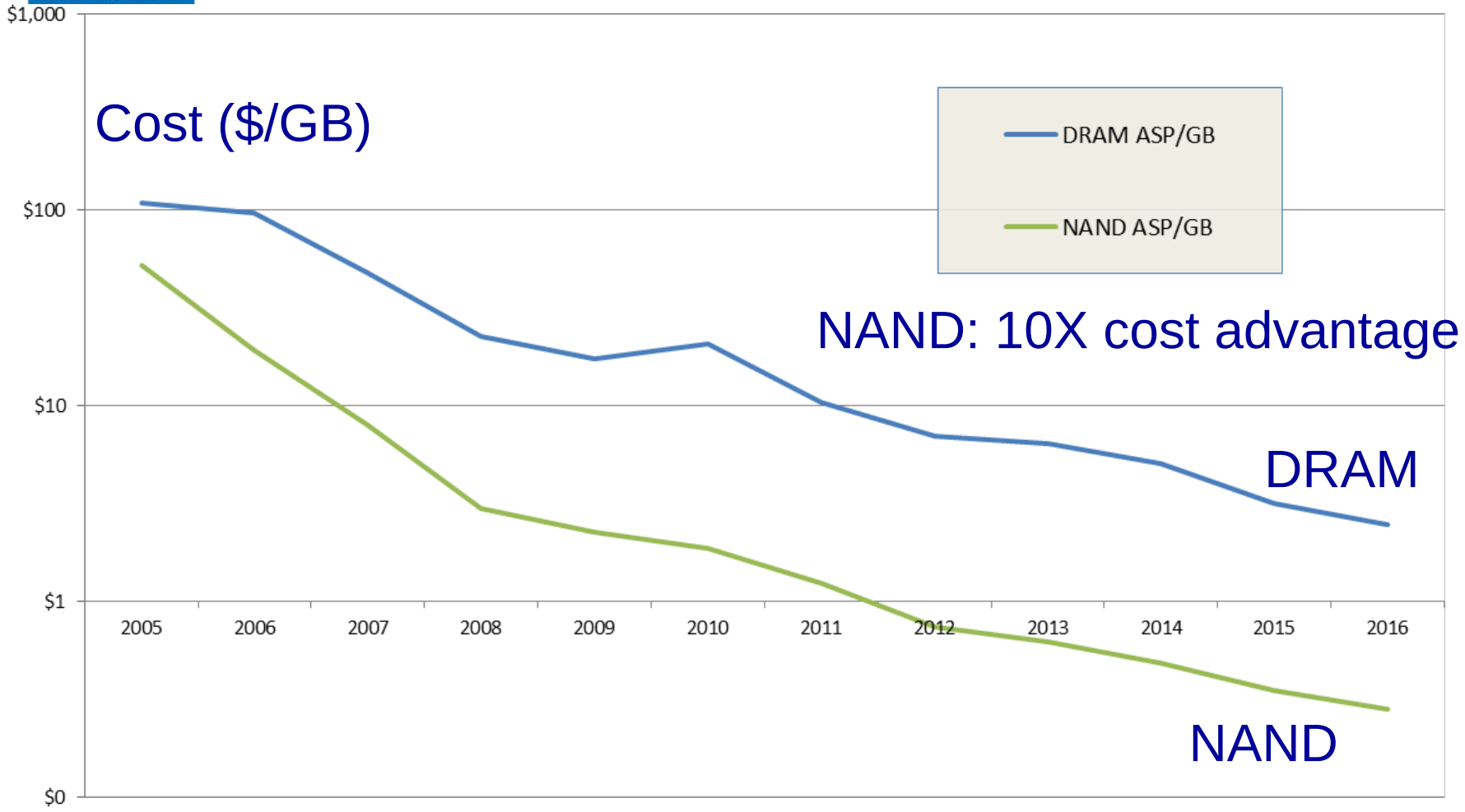
- Demand for Flash Memory
- Challenges and Developments in 10-nm Class NAND
- Future Development
- Final Notes

Demand for NAND Flash Memory

Applications Driving NAND Demands

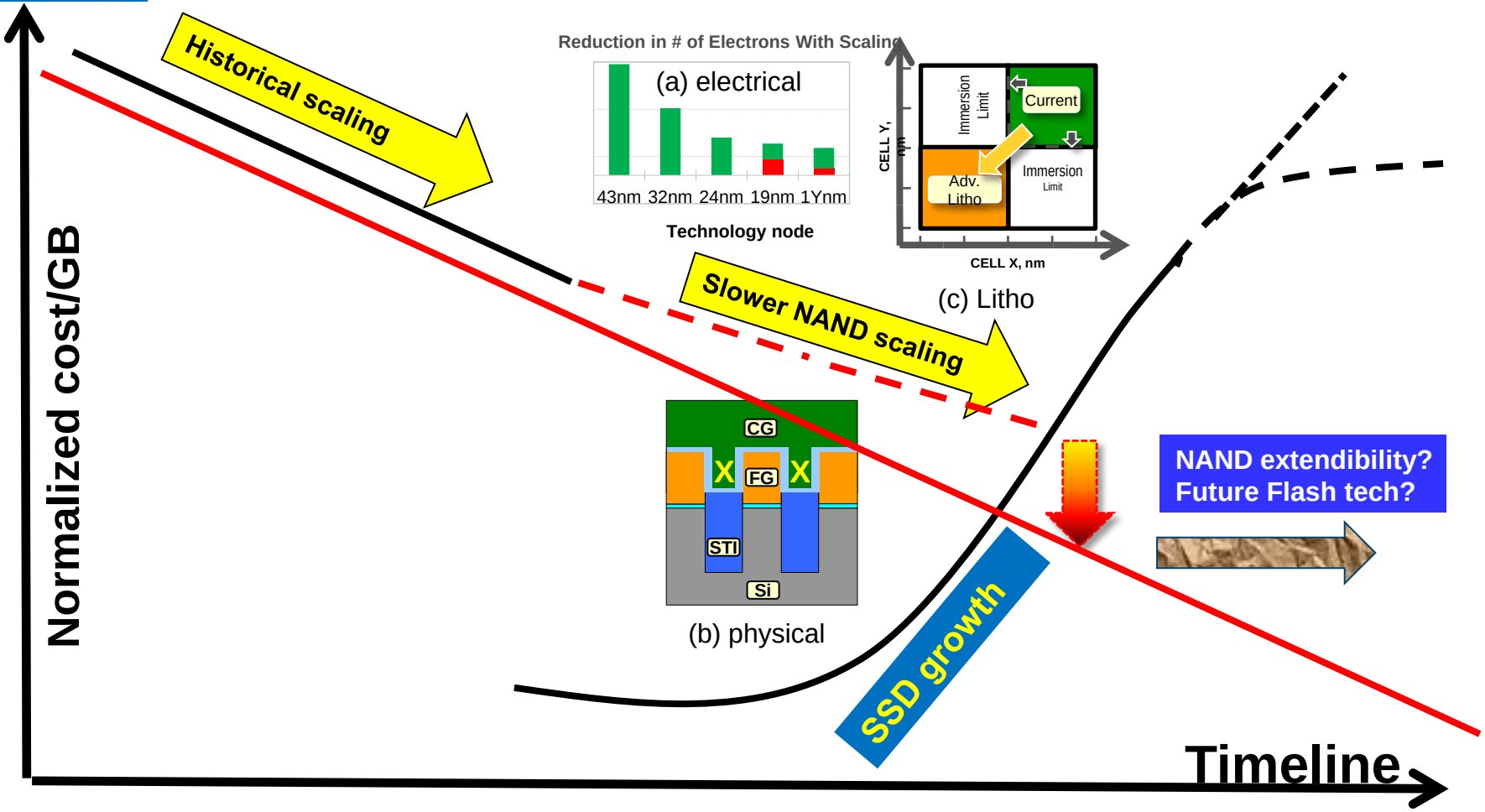


NAND vs. DRAM Cost Delta: New Opportunities



Source: Gartner Forecast

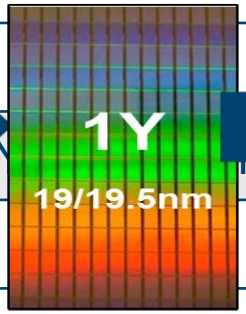
Flash Scaling Trends



- Slower NAND scaling due to more complex process and fundamental changes in lithography
- Electrical/physical limits of NAND, higher density, and $/GB scaling will require 3D approaches

SanDisk Technology Strategy

2D NAND

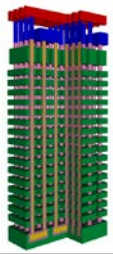


Note: Diagram not to scale

1Z-nm → ??

3D BiCS

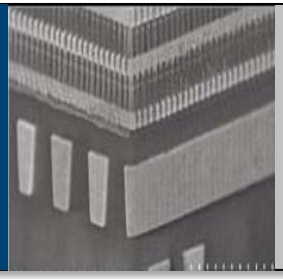
Bit Cost Scalable NAND



- Efficient and Scalable 3D NAND Architecture
- Easy system adoption due to similarity to 2D NAND

3D ReRAM

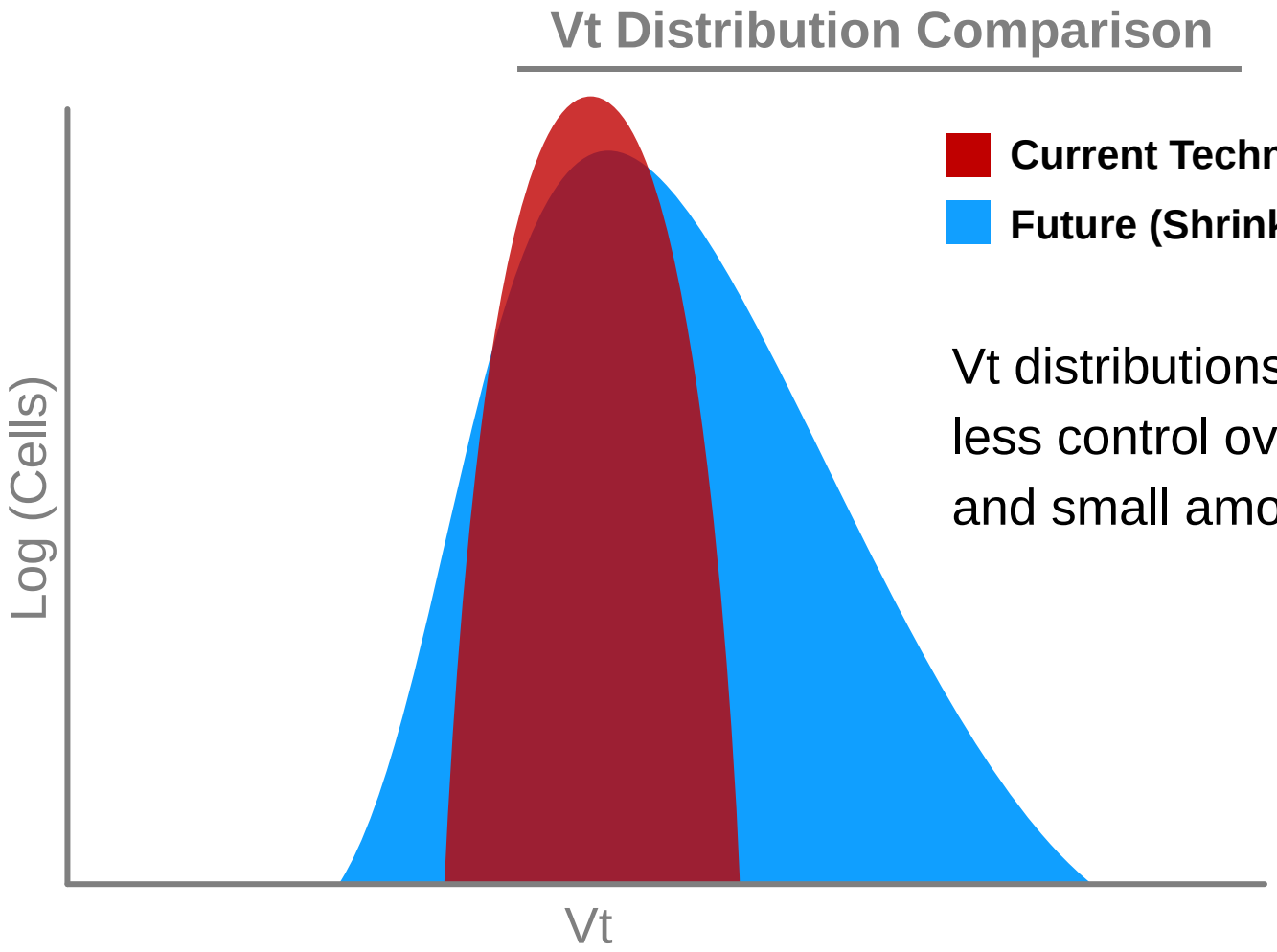
3D Resistive RAM



- 32 Gb Test Chip Successfully Made on 24nm node
- Potential to Scale Below 10nm

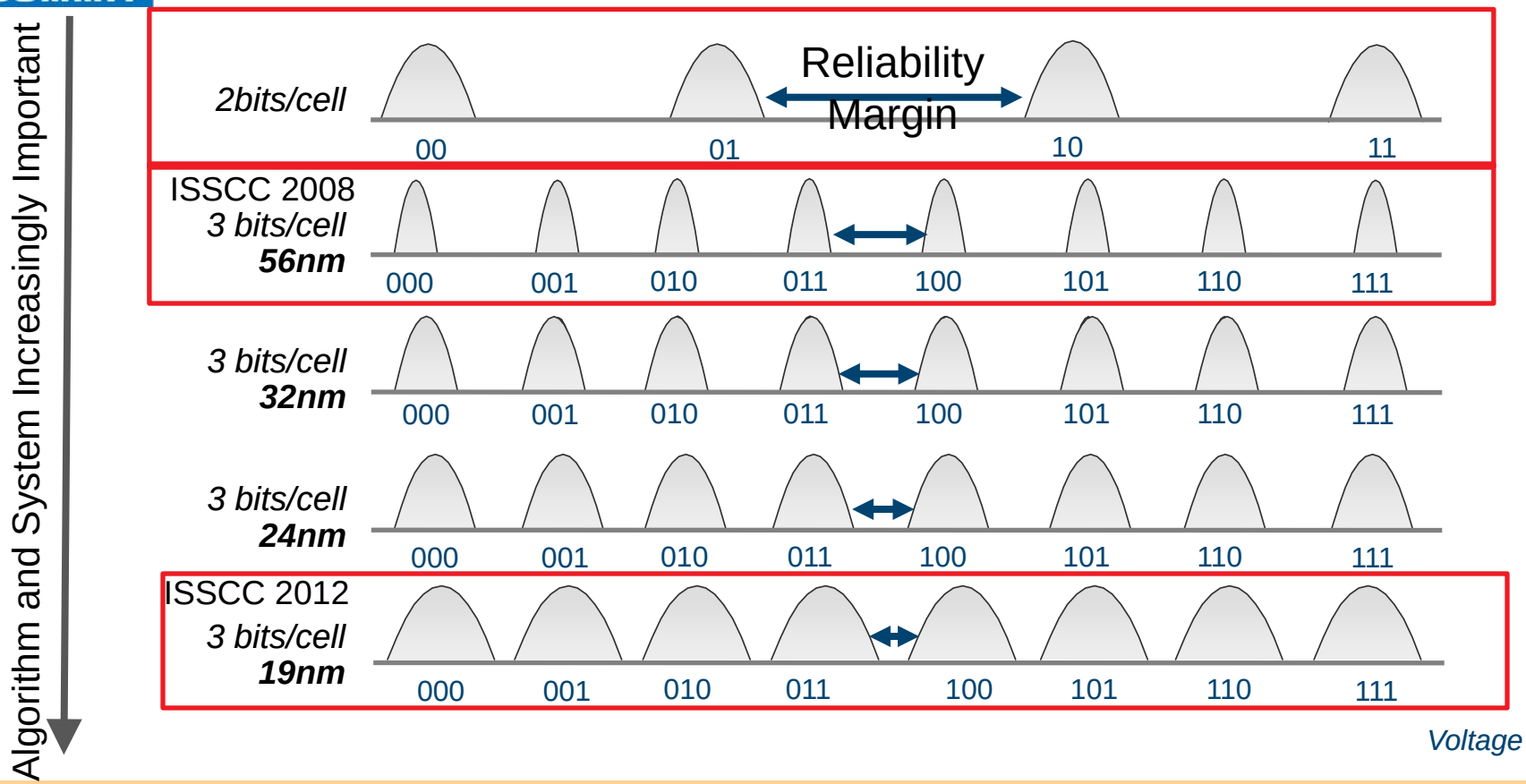
Challenges and Developments in 10-nm Class NAND

The Effect of Scale Down (Technology Shrink)



Vt distributions wider because of less control over the cell uniformity and small amount electrons in FG.

Reliability with Physical Scaling & 3Bits/cell

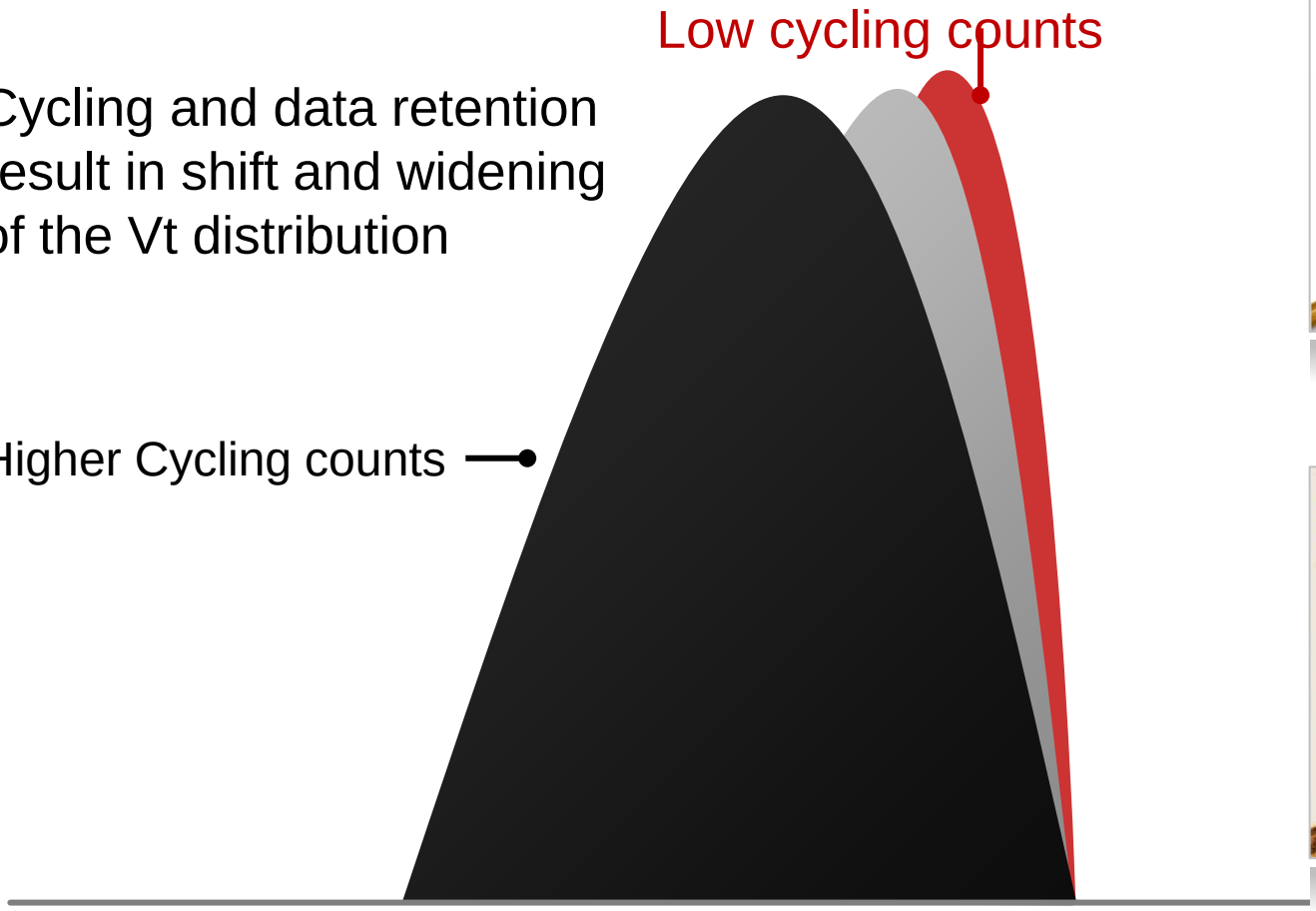


- 3 bits per cell continue in 1Ynm and 1Znm
- More applications will use 3 bits per cell for cost reduction

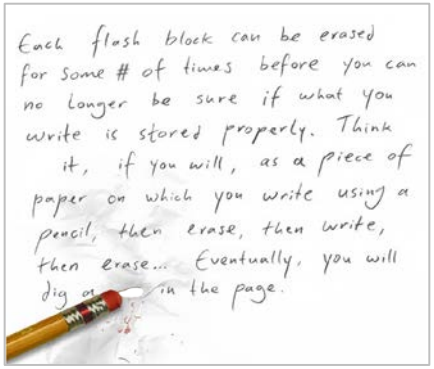
The Effect of Cycling + Data Retention

VT Shift after Data Retention

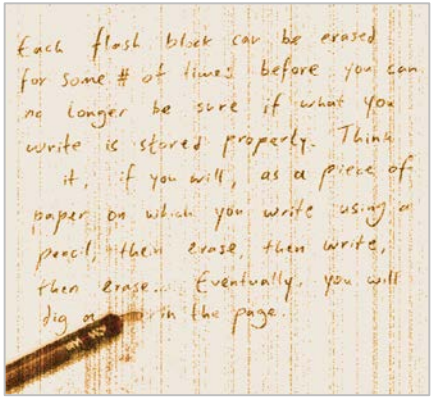
Cycling and data retention result in shift and widening of the Vt distribution



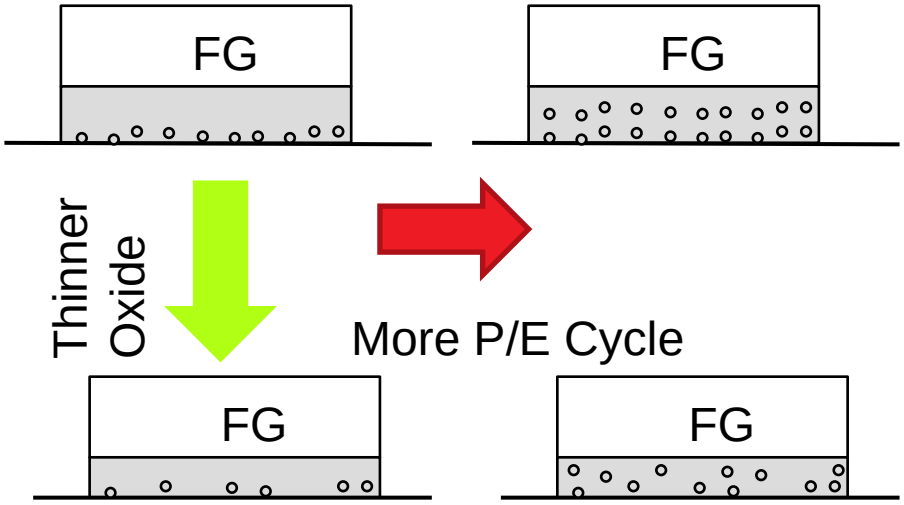
Cycling

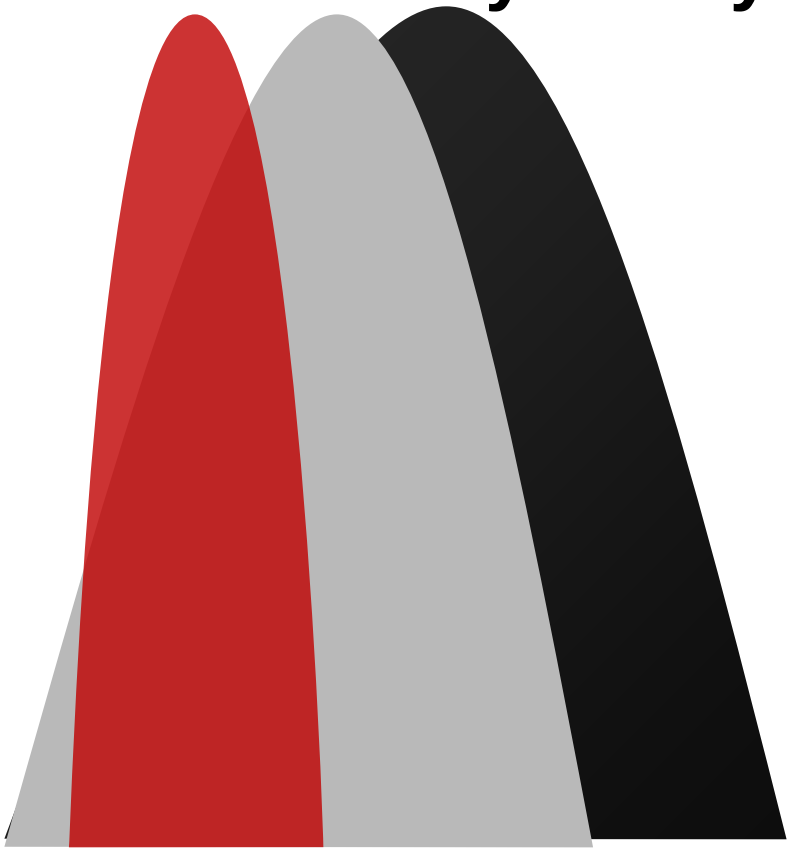


Data Retention



Factors Affecting Flash Memory P/E cycle

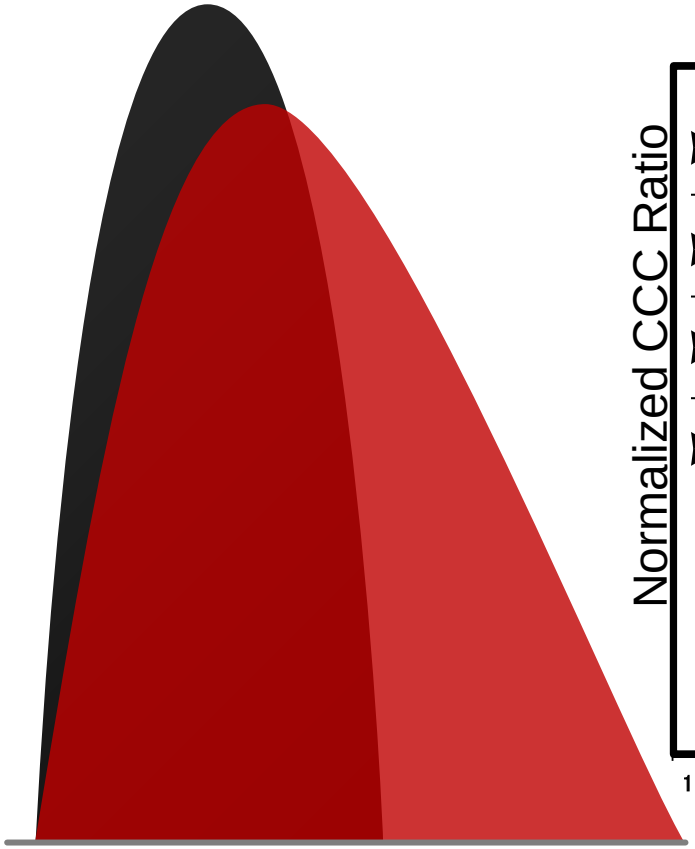


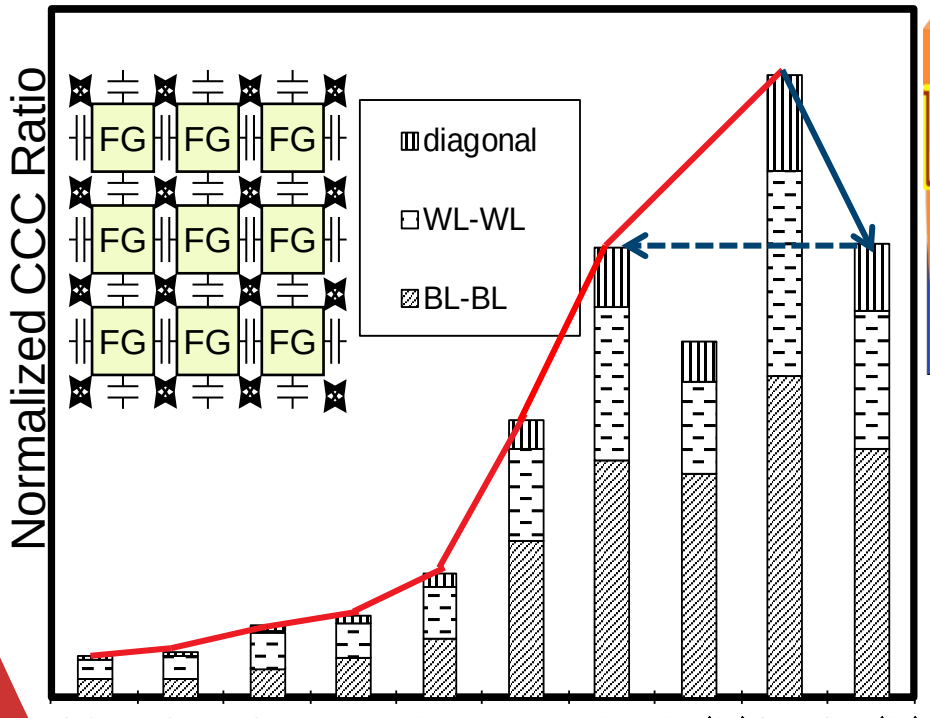


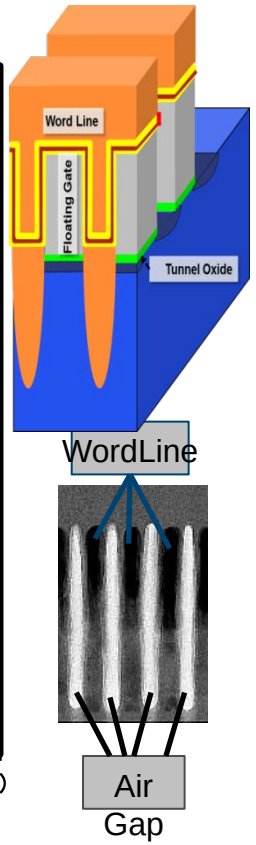
- Limited endurance in Flash Memory is due to Tunnel-Oxide Degradation and trap generation
- Thinner Oxide can help → less data retention
- Heating to get the traps out?

The Effect of Cell to Cell Interferences

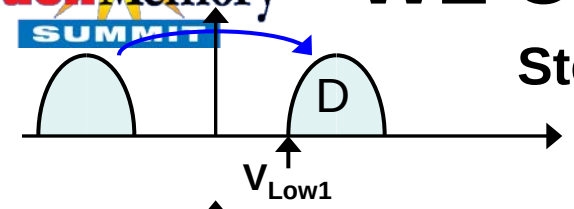
Interferences and noise cause the Vt Distribution to shift and widen



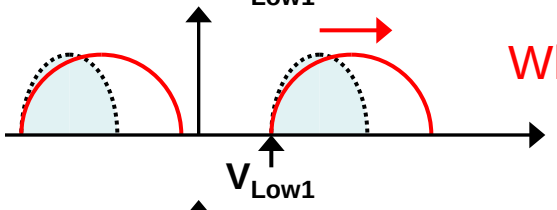




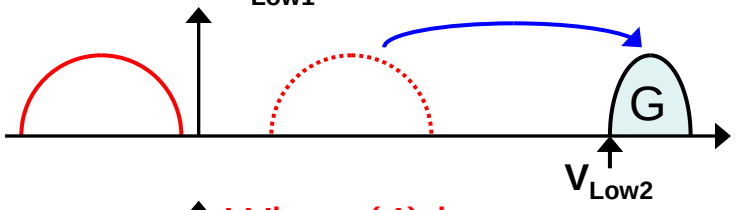
Overcome Cell to Cell Coupling – WL Order



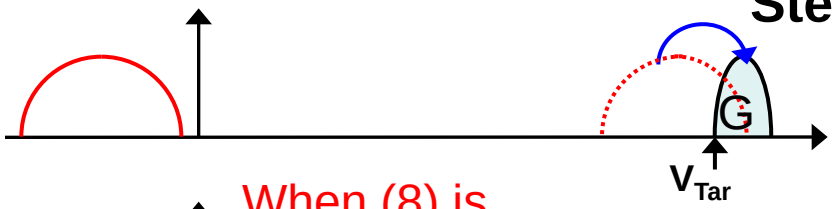
Step1: 2 states Program



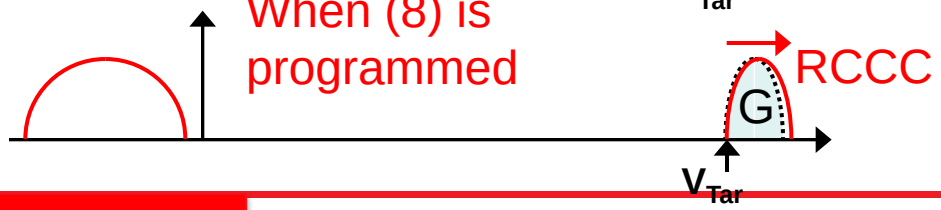
When (1) is programmed

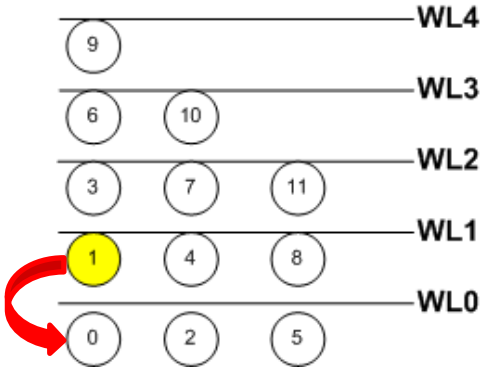


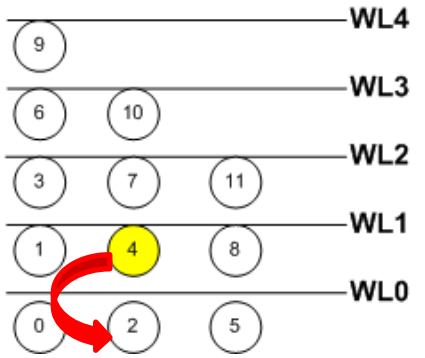
Step2: Coarse Program

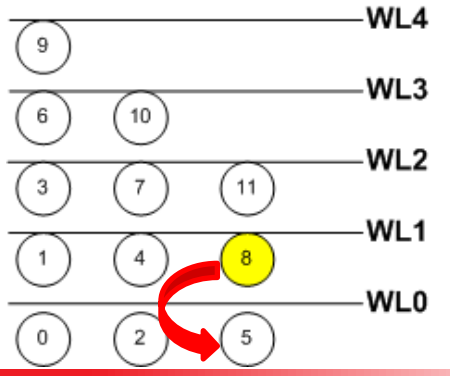


Step3: Fine Prog





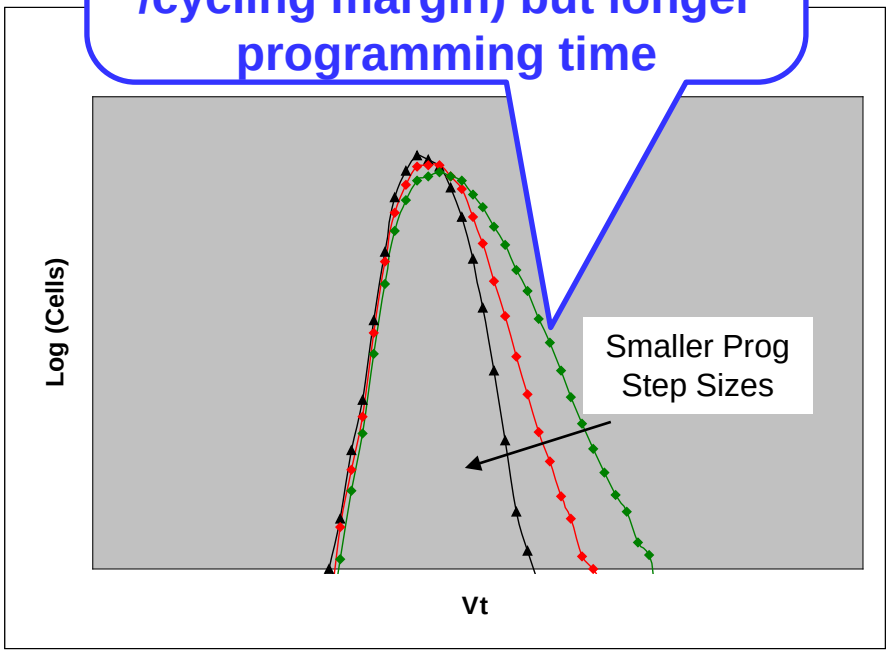


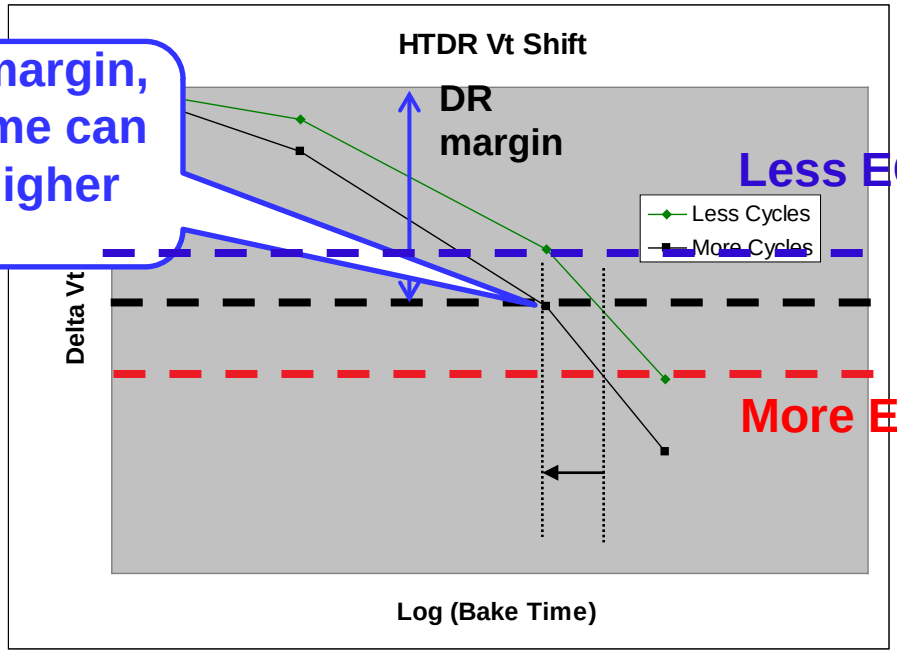


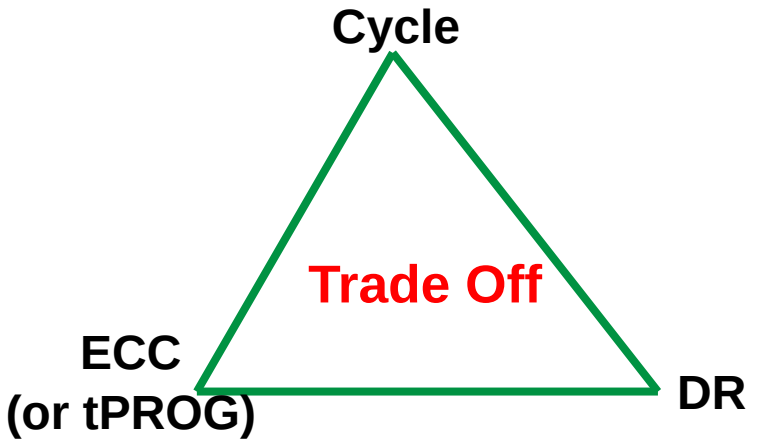
P/E Cycle/Data Retention/ Performance Tradeoff

For the same DR margin, reduction in DR time can be traded in for higher endurance

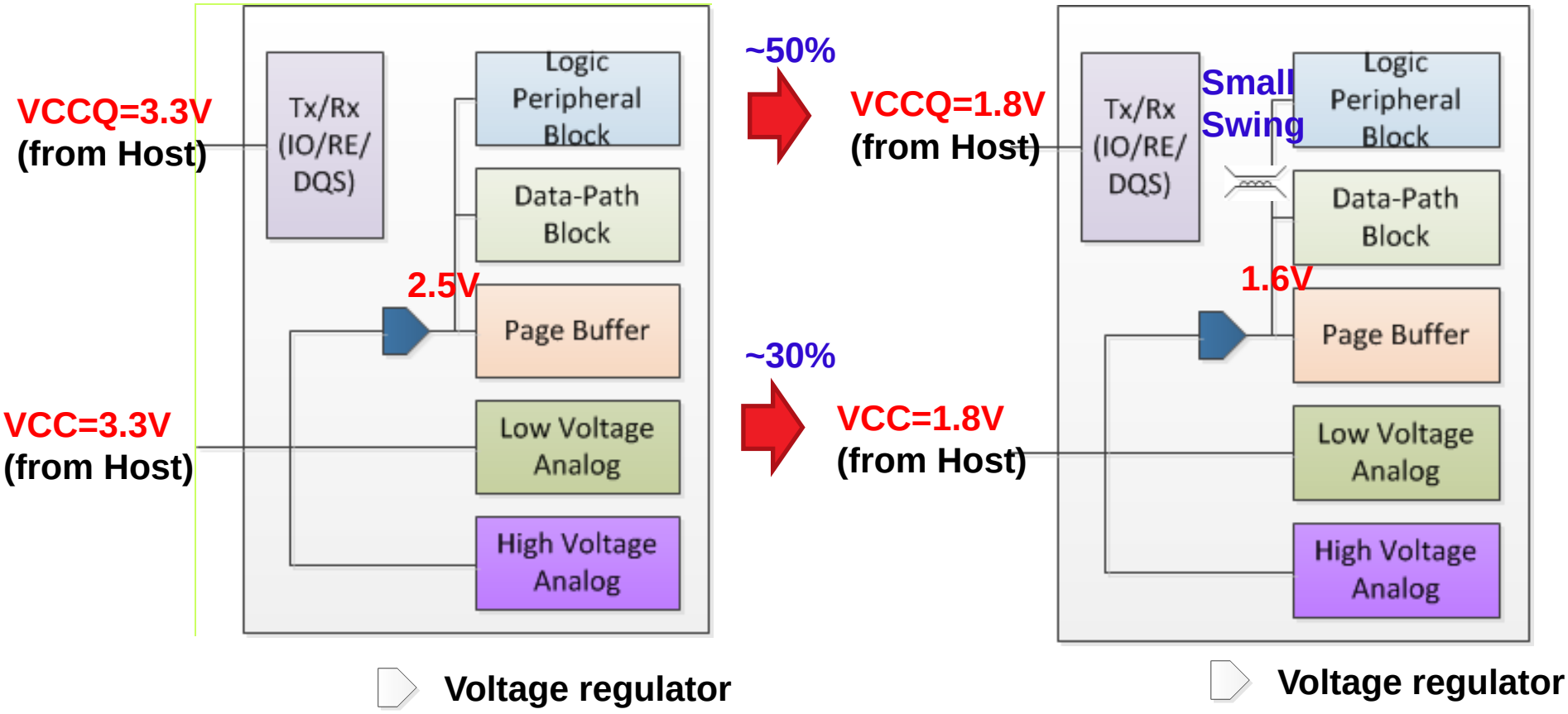
Smaller program voltage step size: narrower distributions (for more DR /cycling margin) but longer programming time







Energy Reduction – Lower Supply Voltage



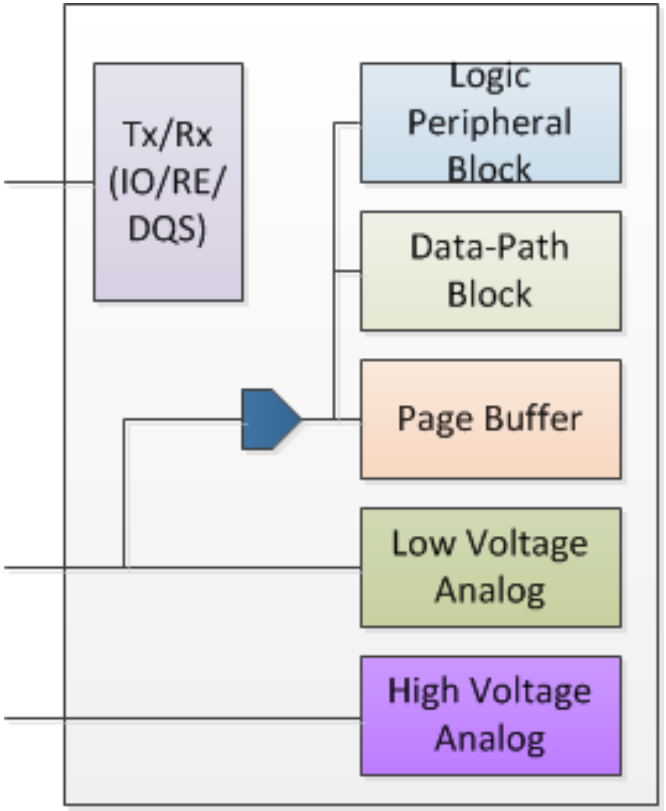
- Power Supply get lower for energy reduction

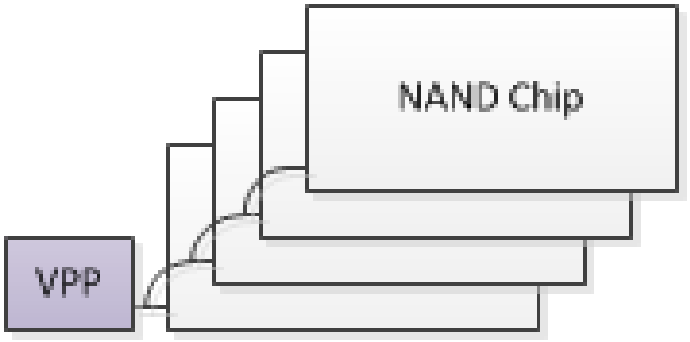
Energy Reduction – External Pump Supply

VCCQ=1.8V
(from Host)

VCC=1.8V
(from Host)

VPP=12V-24V
(pump chip)

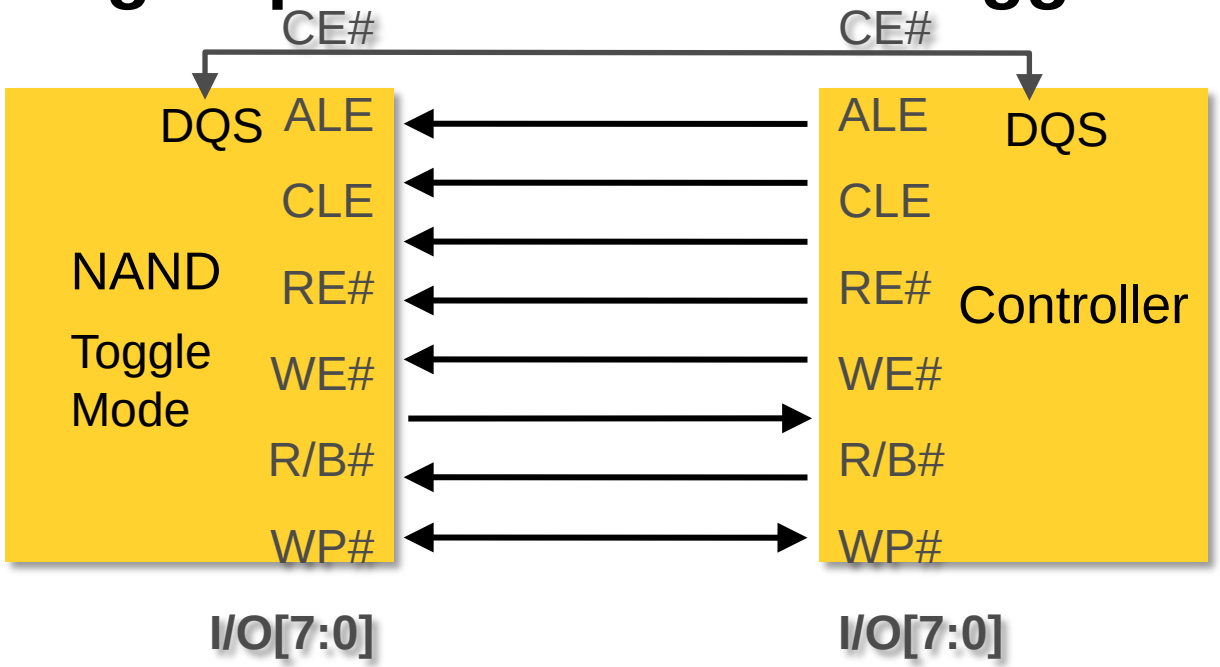




The JEDEC standard NAND Flash Interface 0.62. VPP=12V

- High Voltage generation may cost more power with lower VCC supply
- External pump device could be more efficient

High Speed IO Interface Toggle Mod



50MB/s	200MB/s	400MB/s	533MB/s	800MB/s ?
All NAND	2xnm	1x-1ynm	1znm	**3D NAND**

- Interface Speed impact on System performance
- 800MB/s need new transistors (extra process cost)

Future Development

3D NAND--Alternatives to 2D NAND

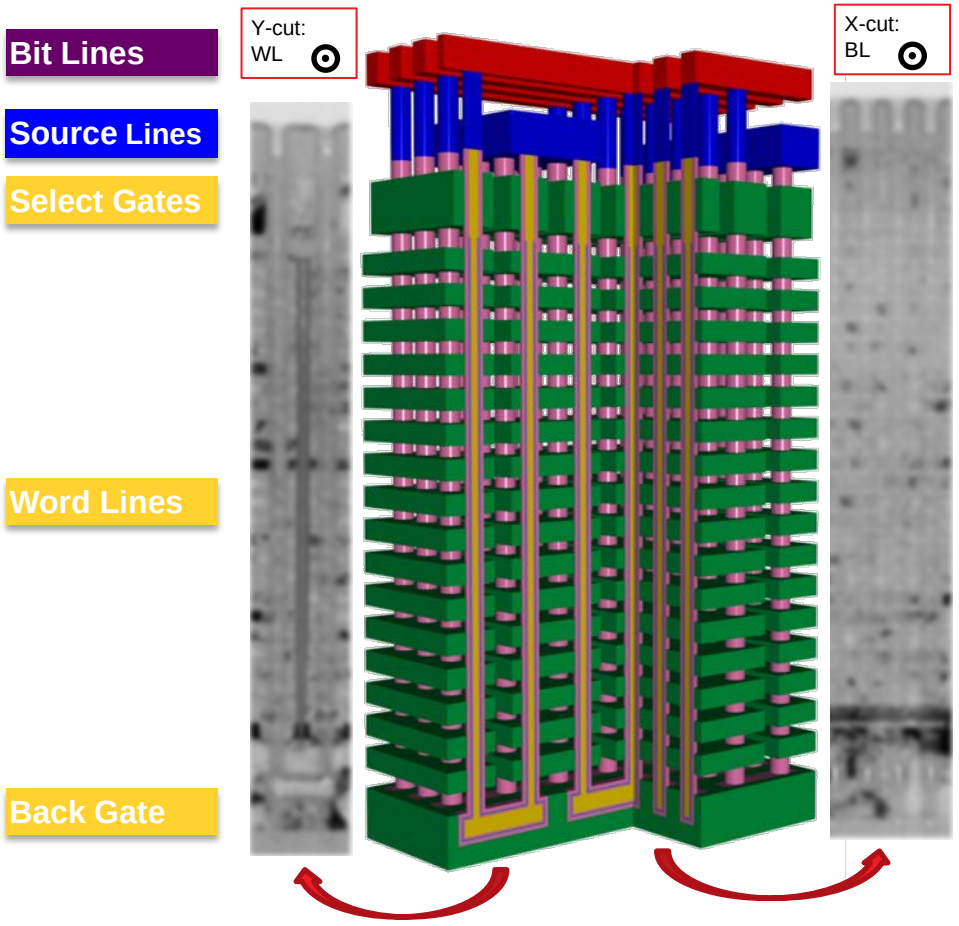
3D NAND Technology

BiCS

- Doesn't require EUV
- Regular optical tools for less stringent HP
- Large cell for better reliability

Yield Challenge

- **High aspect Ratio**
- **Multiple stack patterning**
- **Defect in 3-D structure**

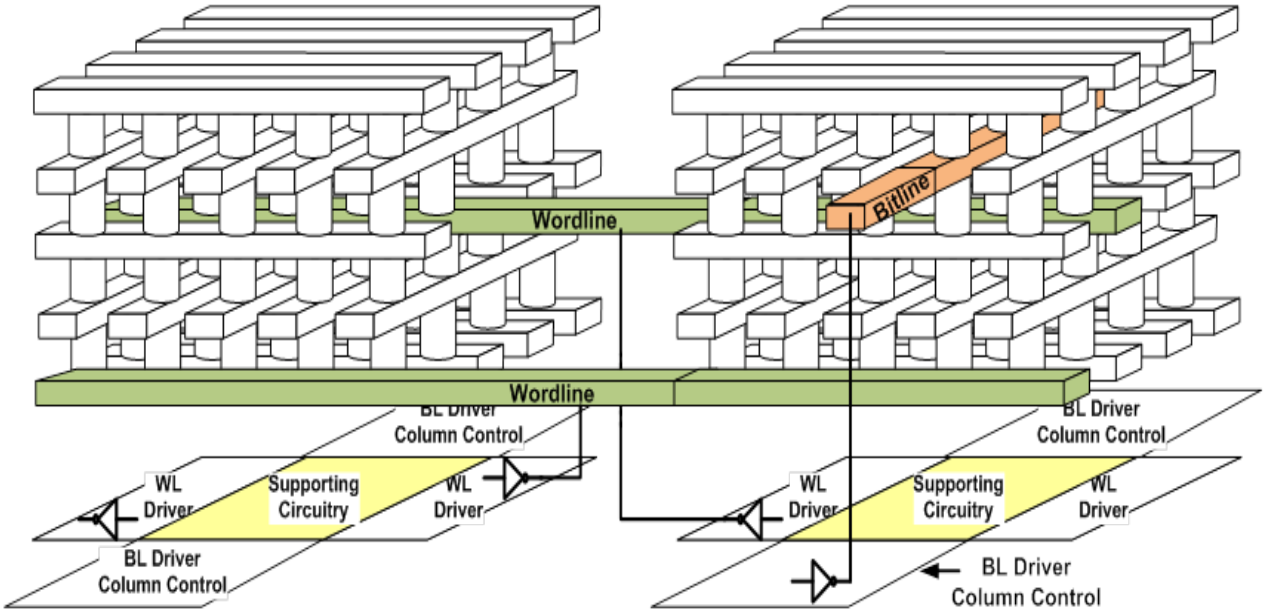


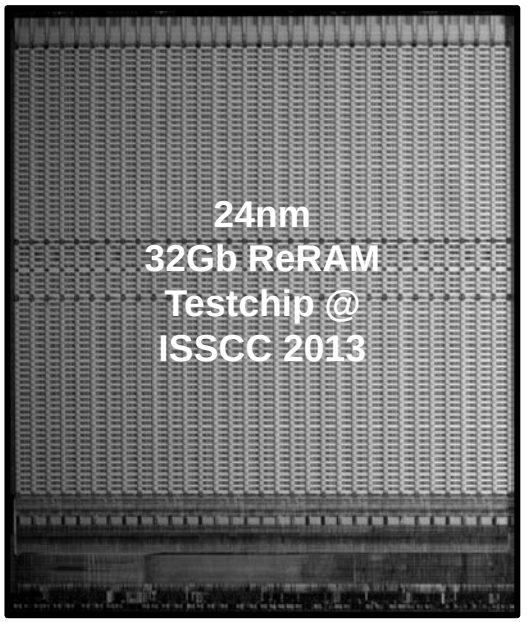
Note: Diagram not to scale

BiCS offers Cost cutting and overcome 2-D NAND scaling issues

3D ReRAM

- SanDisk R&D making steady progress in 3D ReRAM
- 3D ReRAM R&D Paper Presented at ISSCC 2013





3D ReRAM may scale to below 10nm node

Final Notes

Overcome the Challenges of 10nm–class NAND Flash

- Advanced system management
  - Intelligent memory managements and algorithm
  - Trade off performance, data retention and endurance
- Enhanced system performance
  - High speed IO interface
  - Reduced energy consumption to allow massive parallel operations
- Advanced New Technologies on the Horizon
  - 3D NAND & ReRAM

The Flash industry needs breakthroughs to take advantage of the explosive storage demand in the digital age

Flash Memory continues to be the storage king