SSDs with Error-Prediction LDPC (EP-LDPC) and Error-Recovery Schemes

Shuhei Tanakamaru[1,2],
Yuki Yanagihara[2], and Ken Takeuchi[1]
[1]Chuo University
[2]University of Tokyo

Outline

- Introduction
- Error Prediction (EP) LDPC scheme
  - Measurement results
- Error Recovery (ER) scheme
  - Program disturb error recovery pulse (PDRP)
  - Data retention error recovery pulse (DRRP)
- Summary & Conclusion

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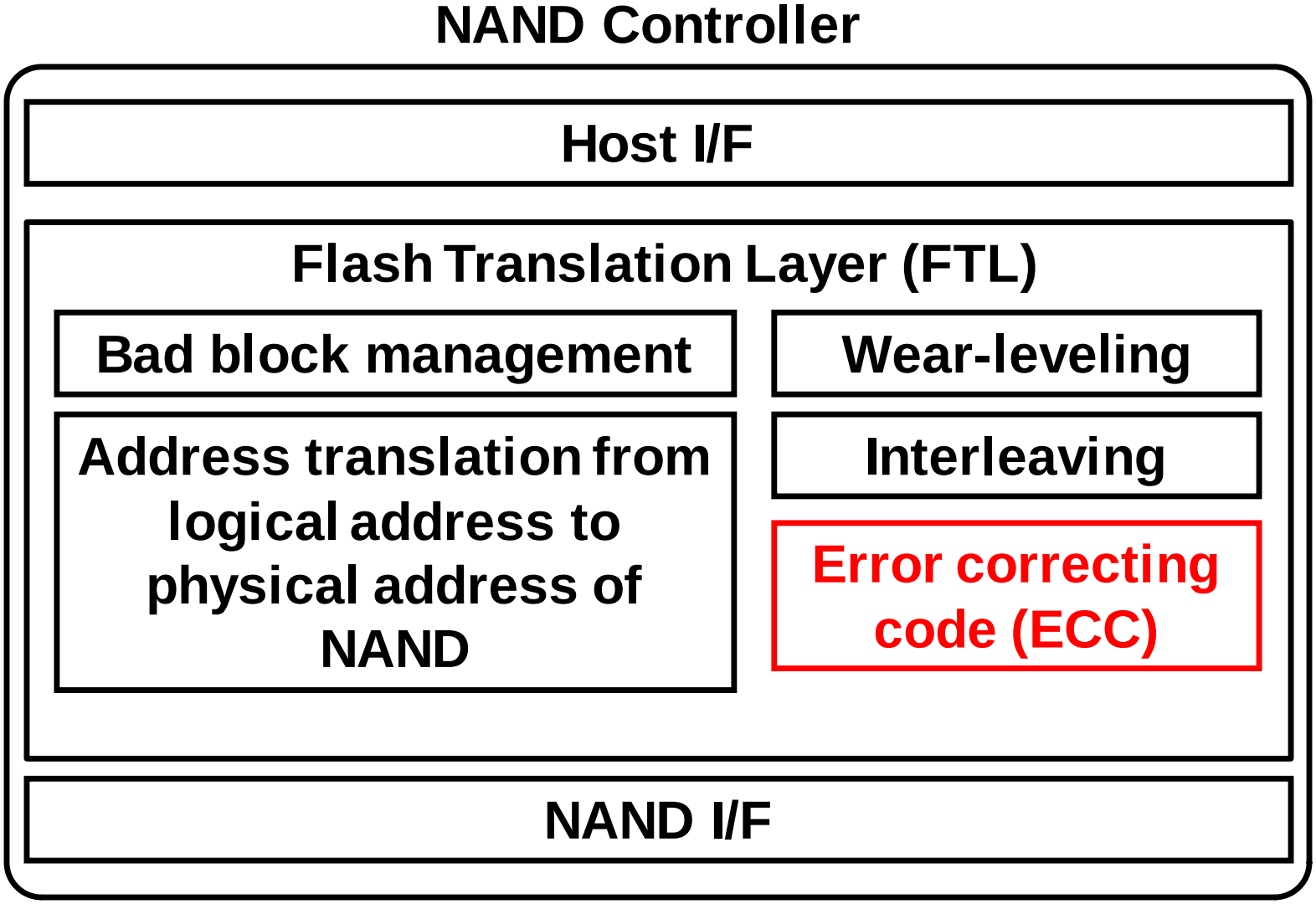
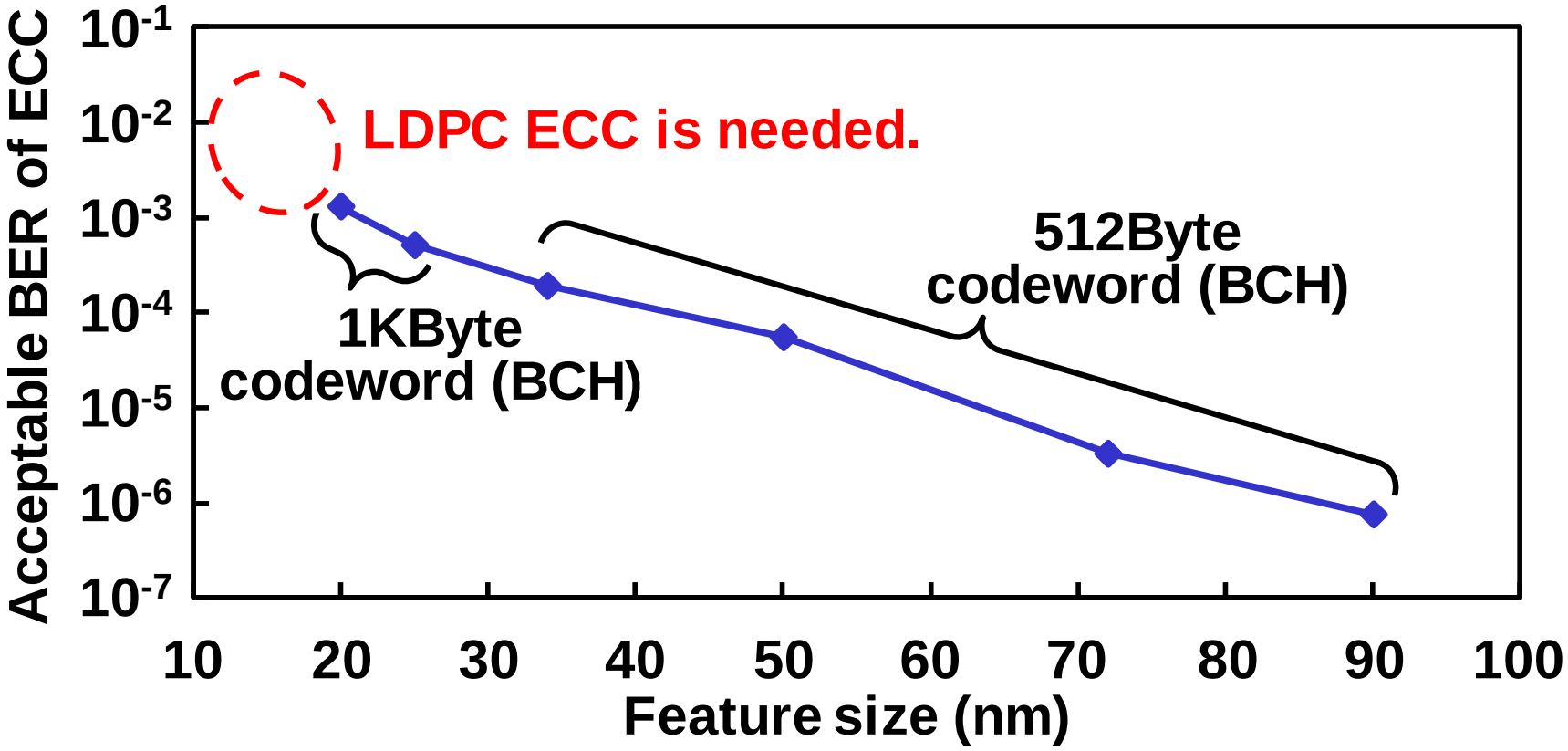
NAND Controller Architecture



K. Takeuchi, *JSSC*, pp.1227-1234, 2009.

NAND Controller Architecture

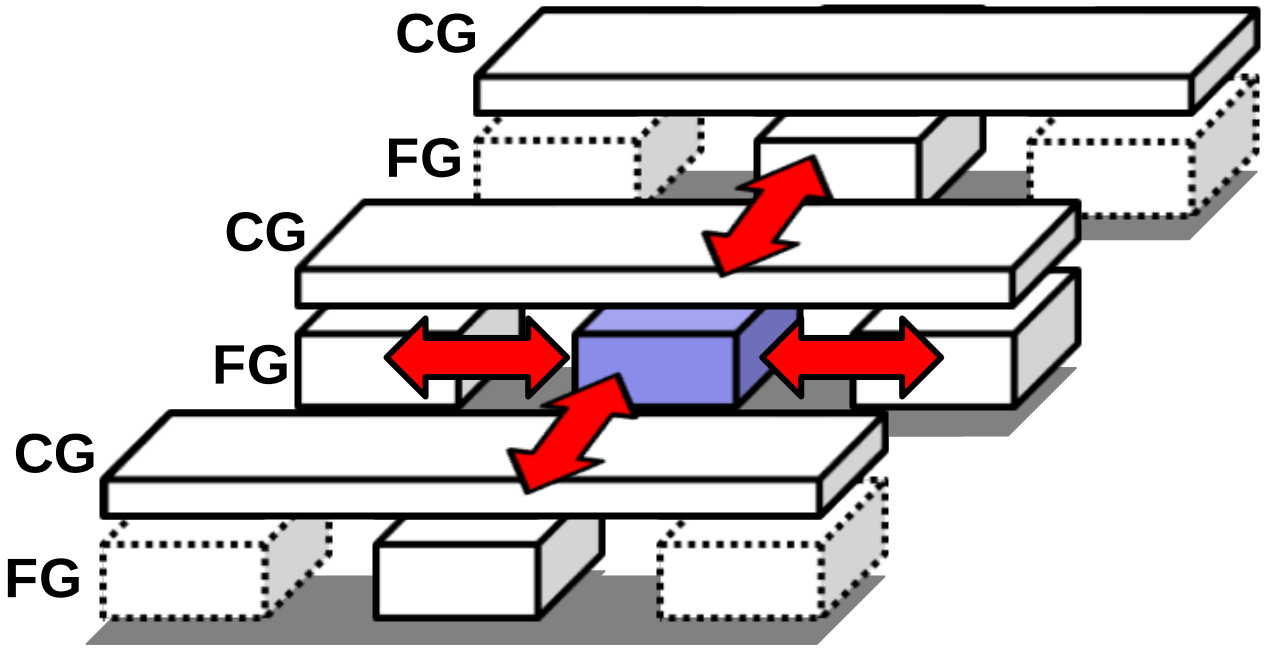
- Stronger ECC is required in the scaled NAND.
- Low-density-parity-check (LDPC) ECC is needed.



K. Prall et al., *IEDM*, pp. 102-105, 2010.
R. Motwani et al., *Flash Memory Summit*, 2011.

Inter-cell Coupling

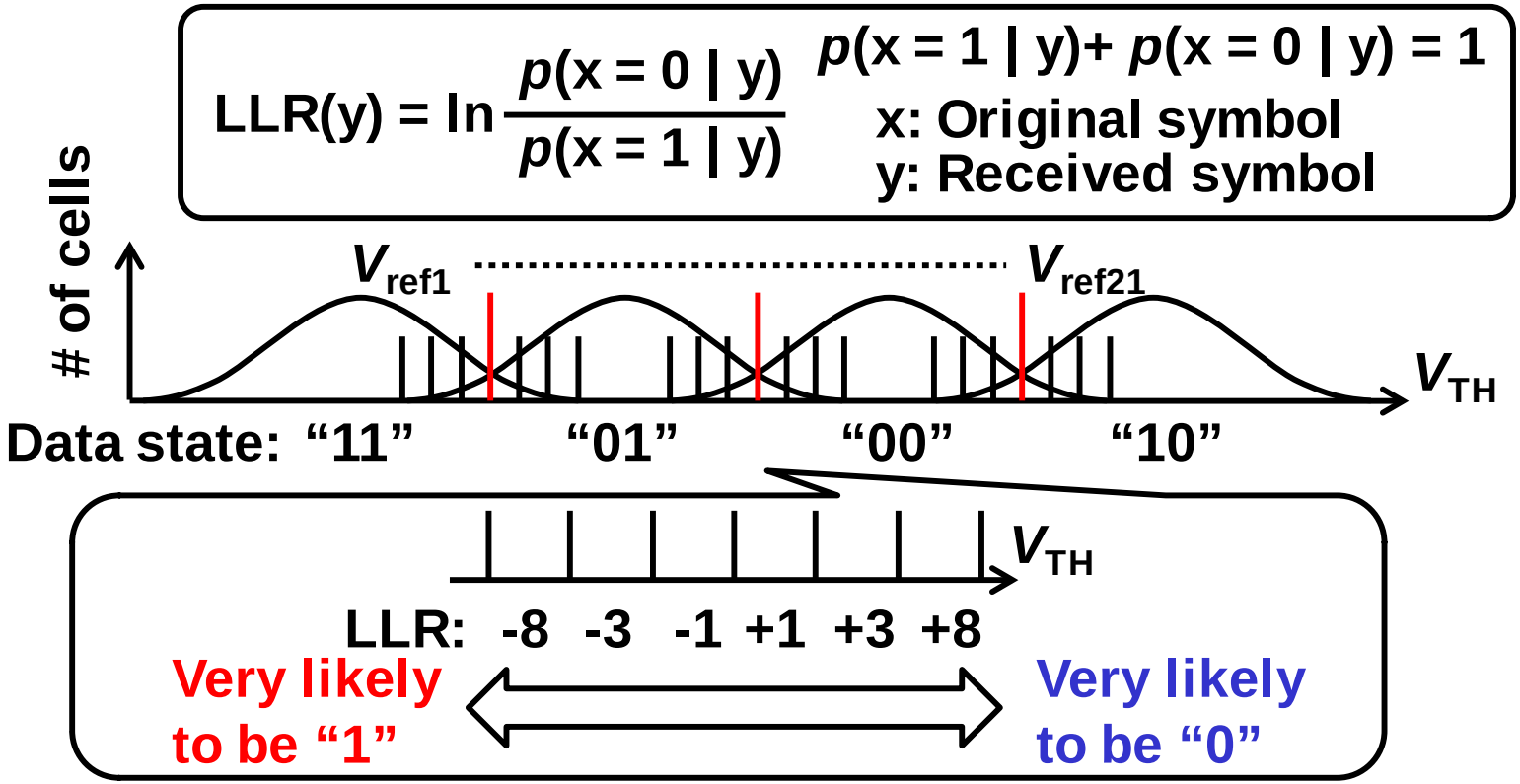
- Floating gate (FG)-FG capacitive coupling significantly degrades memory cell reliability as the design rules shrink.
- Direct field effect to channel is also observed.



J-D. Lee *et al.*, *EDL*, pp. 264-266, 2002.
M. Park *et al.*, *EDL*, pp. 174-177, 2009.

Problem of Soft Decoding LDPC ECC

- Log-likelihood ratio is input to LDPC decoder.
- Increased number of V_{ref} result in large seq. read cycle.



R. Motwani *et al.*, *Flash Memory Summit*, 2011.

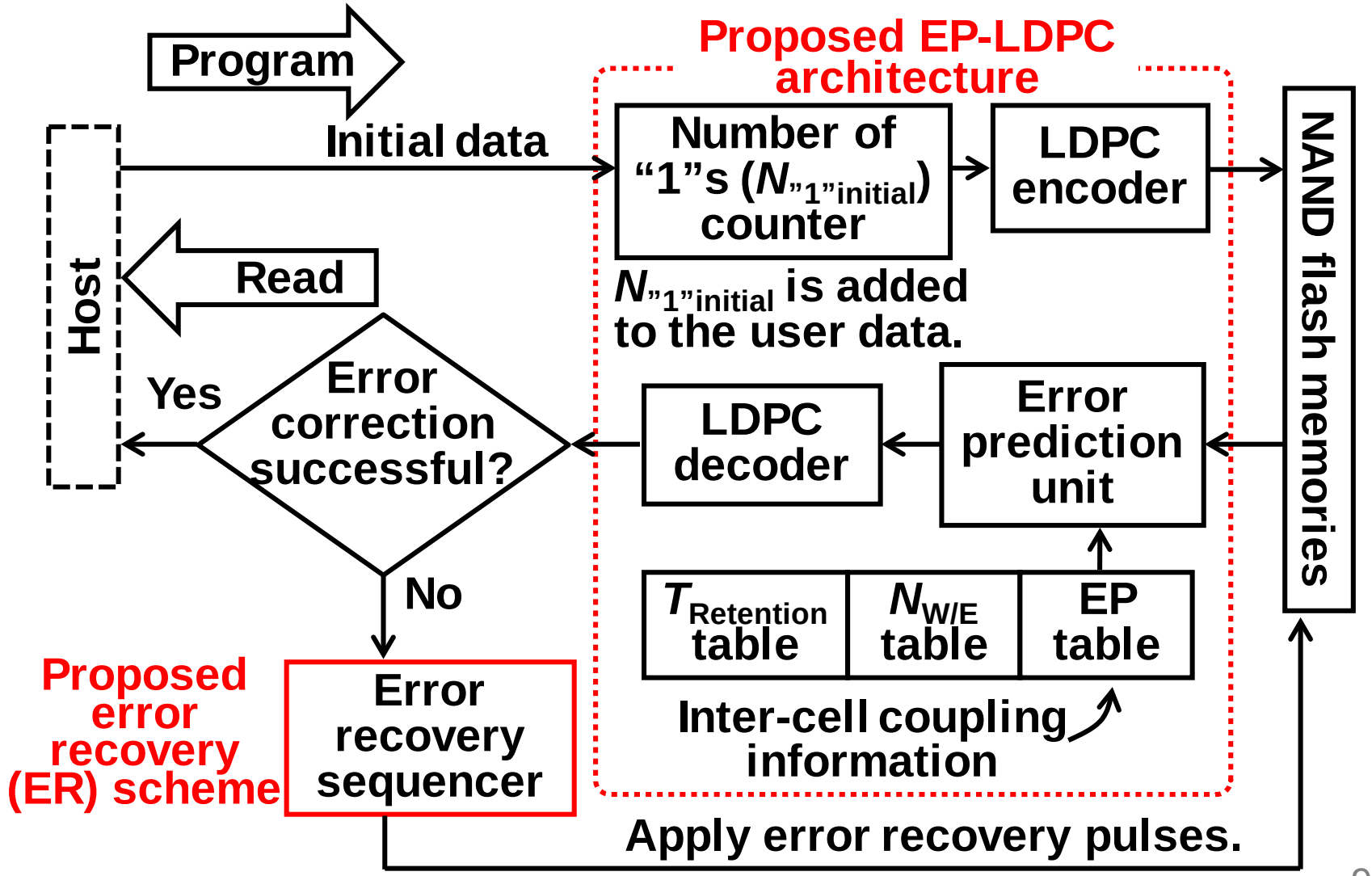
C. Kim *et al.*, *Symp. VLSI Circ.*, pp. 196-197, 2011.

Objectives of This Work

- To propose an error prediction (EP) LDPC ECC scheme without sequential read cycle increase to realize high reliability.

- To propose error recovery (ER) scheme to further enhance reliability.

Proposed SSD Architecture



S. Tanakamaru *et al.*, *ISSCC*, pp. 424-425, 2012.

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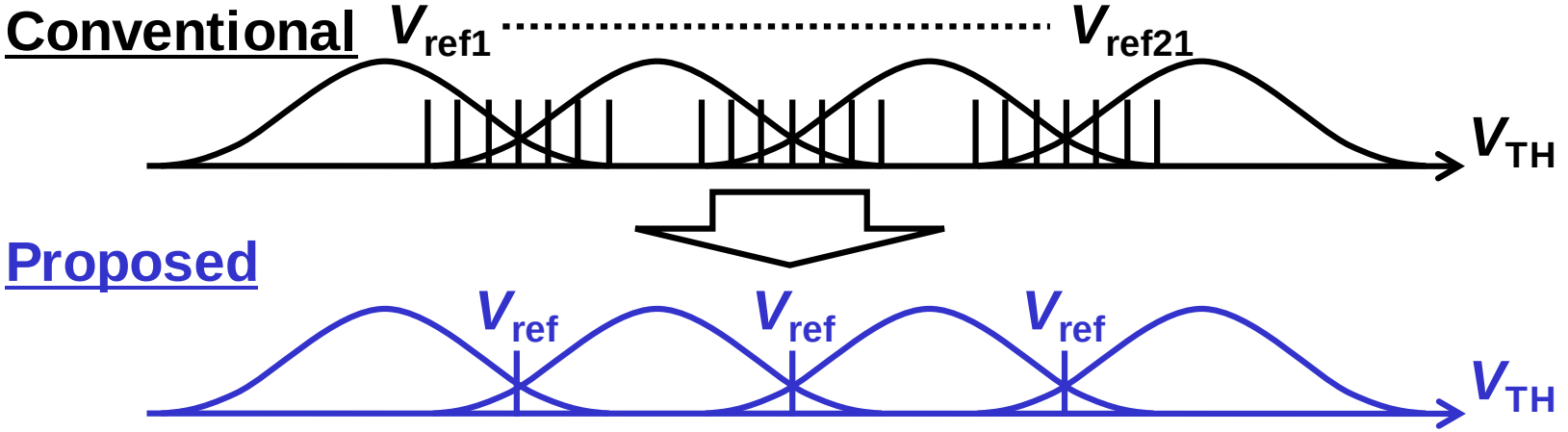
Concept of the Proposed EP-LDPC



Likelihood of data "0"

$$LLR(0) = \log \frac{1-BER_{Est}}{BER_{Est}}$$

Likelihood of data "1"

$$LLR(1) = \log \frac{BER_{Est}}{1-BER_{Est}}$$

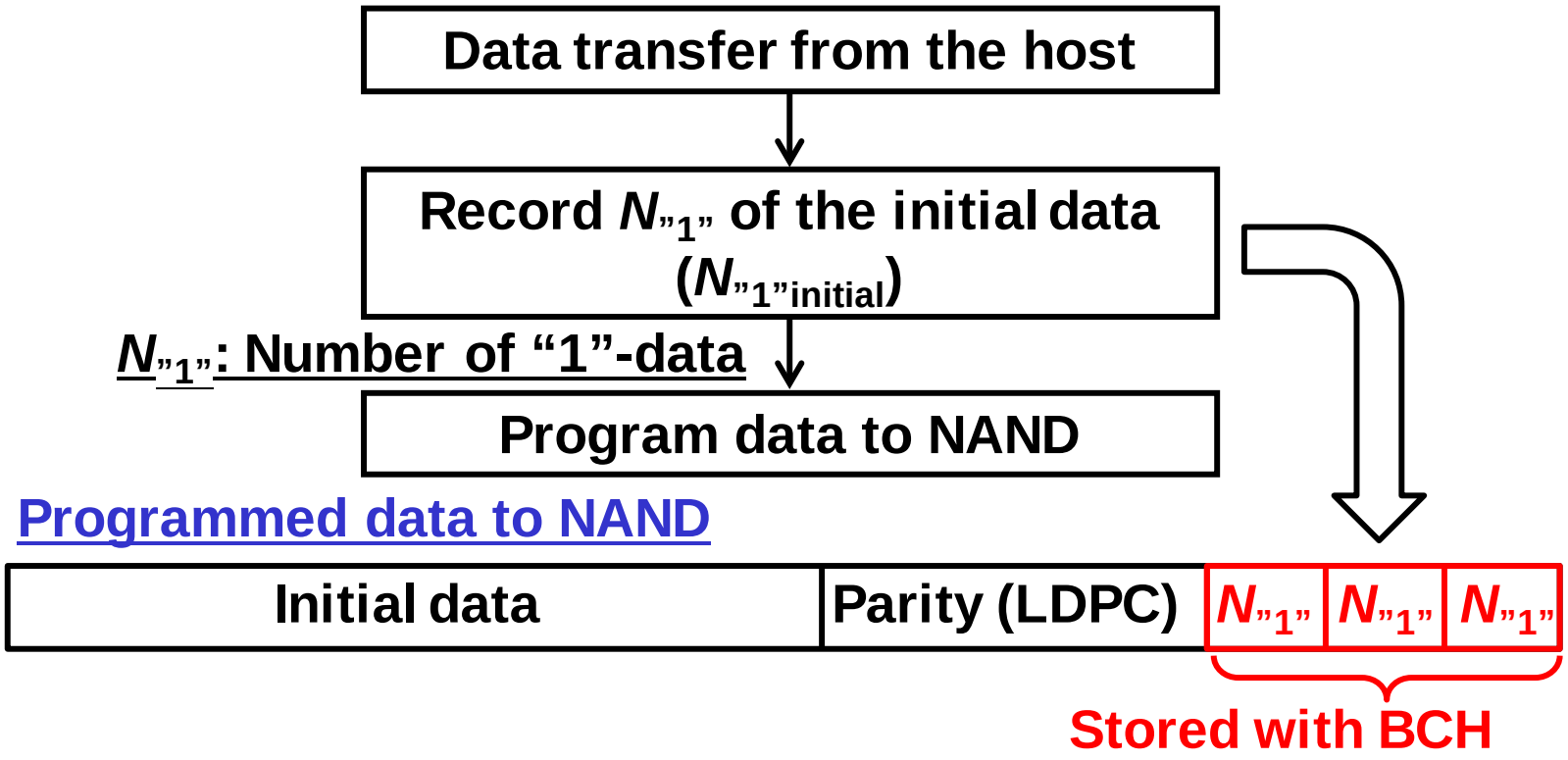
BER_{Est}: Estimated BER with the error prediction sequence

- **V_{TH} information (x3)**
- **Inter-cell coupling information**
- **Write/erase cycles ($N_{W/E}$)**
- **Retention time ($T_{Retention}$)**

} **Less sequential read cycles**

Program Sequence of the EP LDPC

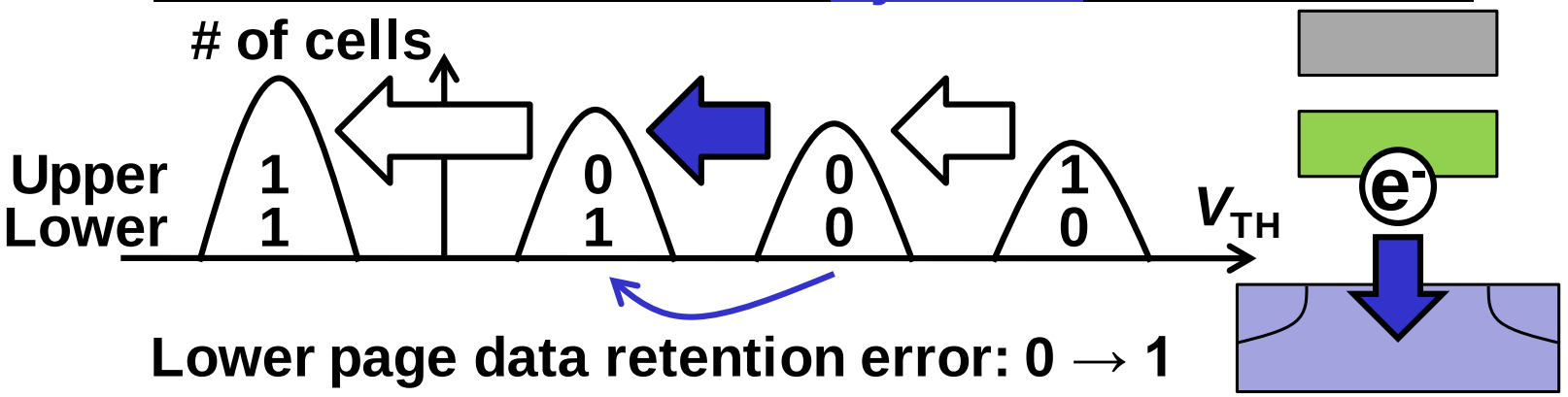
- To estimate BER of the lower pages, $N_{"1"}$ is counted and added to the program data.
- $N_{"1"}$ is protected by triplicated BCH ECC.



Overall BER Estimation

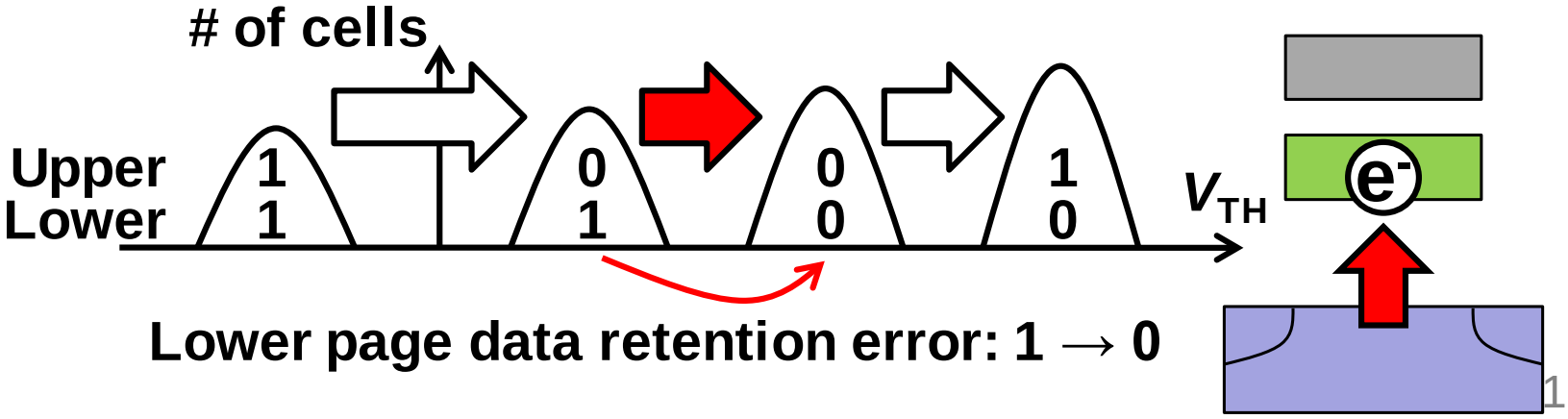
$$BER_{Lower} = |N_{"1"measured} - N_{"1"initial}| / (\text{Page size})$$

Data Retention Error: Ejection of electrons



Lower page data retention error: 0 → 1

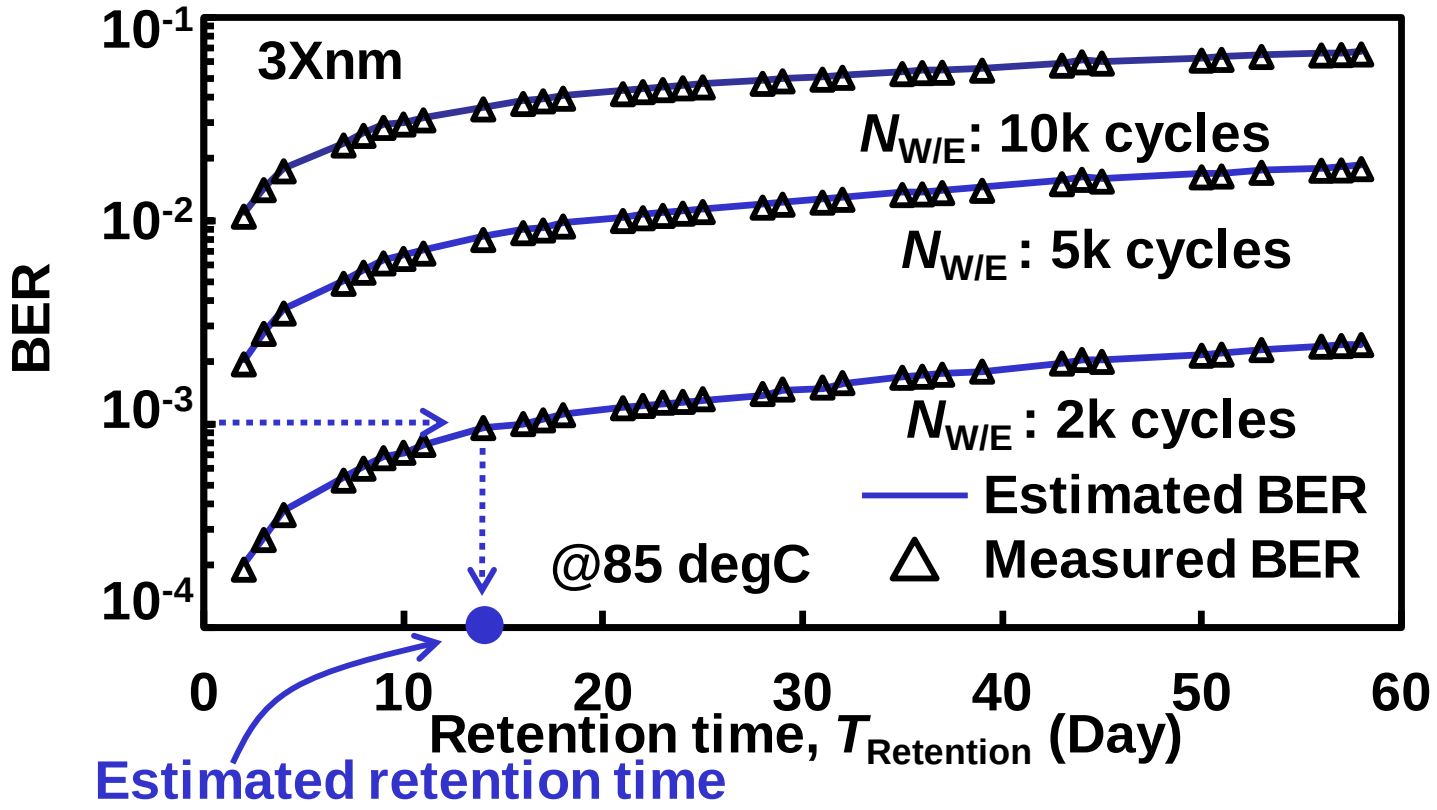
Program Disturb Error: Injection of electrons



Lower page data retention error: 1 → 0

BER & Retention Time Estimation

- BER is estimated from the difference of the number of “1”-data.
- Retention time is estimated from the table (BER vs. retention time).



Pre-recorded Tables (1)

$T_{Retention}$ table

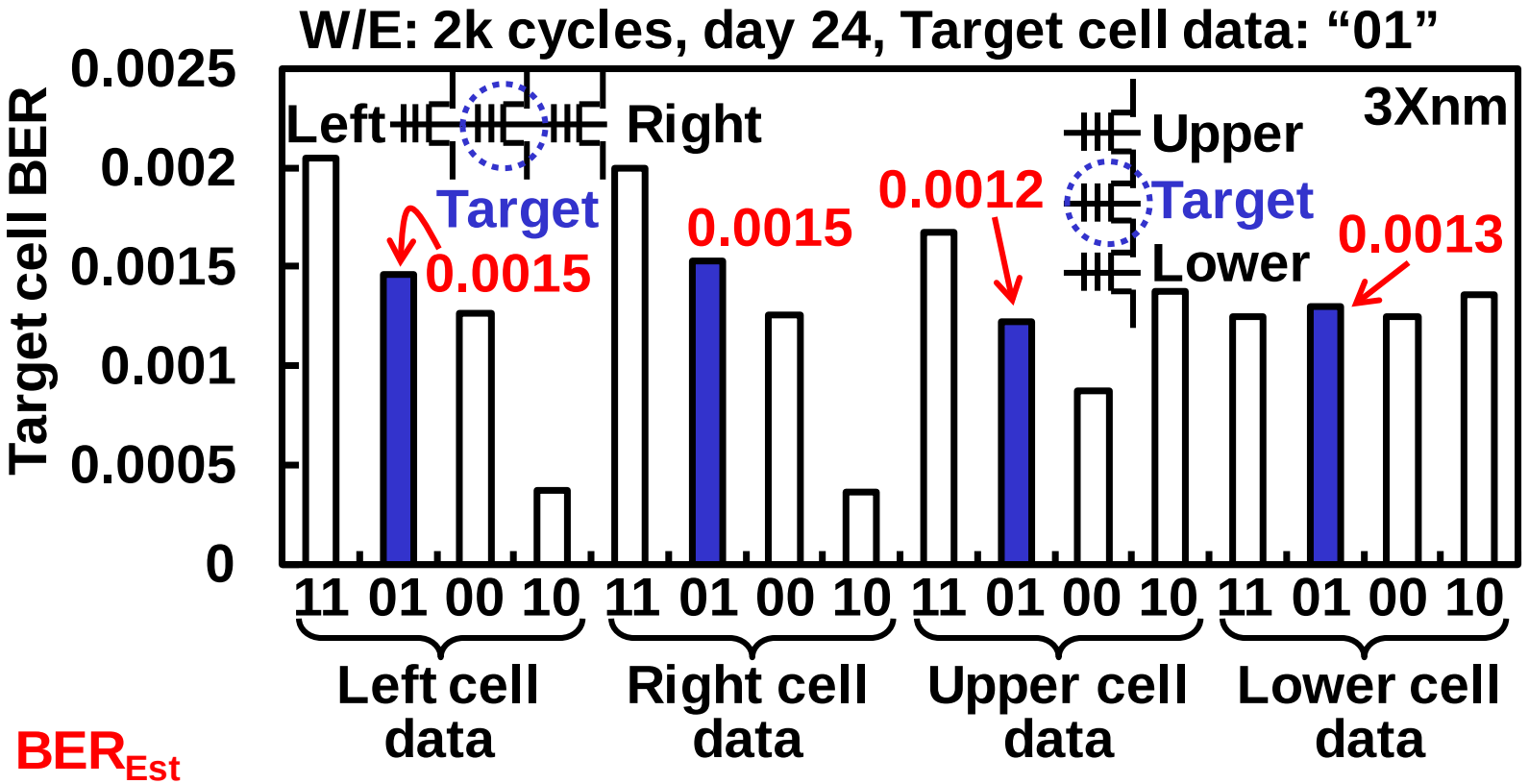
Retention time \ W/E cycles	$N_{W/E}$ 0	$N_{W/E}$ 1k	.....	$N_{W/E}$ 10k
Day 0	BER_{0_0}	BER_{0_1}	.....	BER_{0_10}
Day 1	BER_{1_0}	BER_{1_1}	.....	BER_{1_10}
.....	.....	.....	.....	.....
Day 100	BER_{100_0}	BER_{100_1}	.....	BER_{100_10}

$N_{W/E}$ table (Also used for wear-leveling)

Block number	0	1	.....	65536
$N_{W/E}$	$N_{W/E0}$	$N_{W/E1}$	.....	$N_{W/E65536}$

Error Prediction

- Error prediction is performed with EP table.

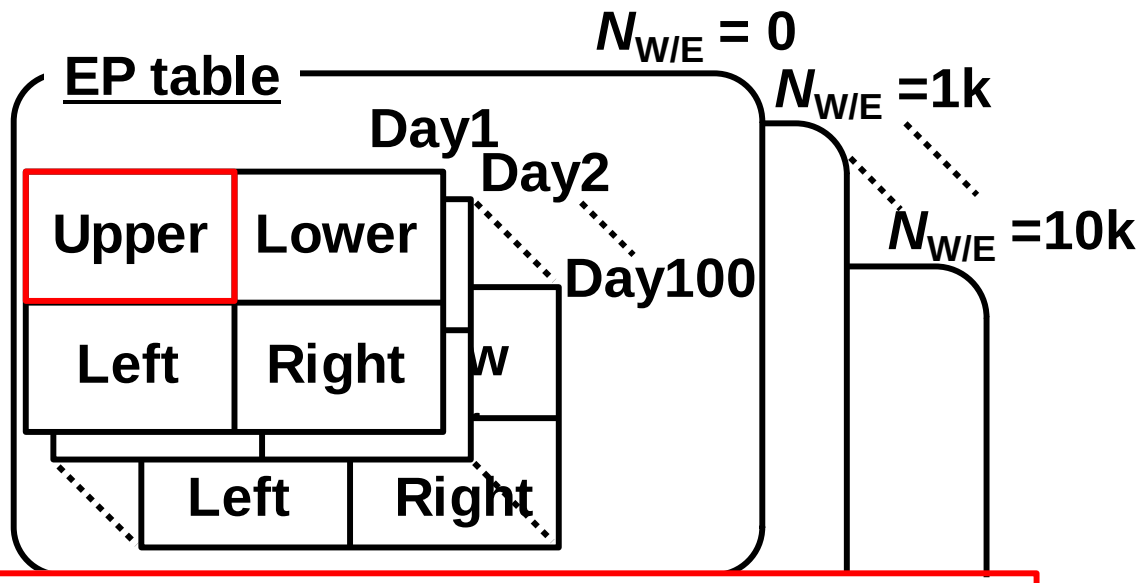


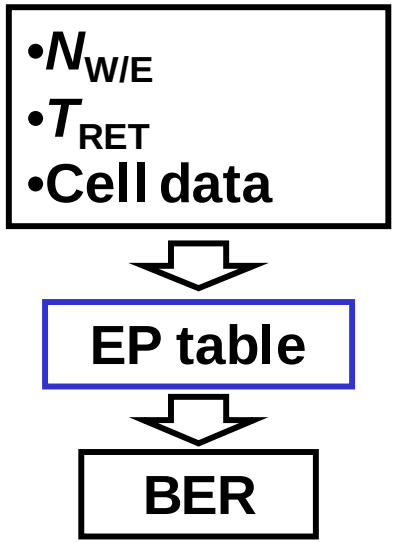
BER_{Est}

~ $(BER_{Left\_"01"} + BER_{Right\_"01"} + BER_{Upper\_"01"} + BER_{Lower\_"01"}) / 4$

= (0.0015 + 0.0015 + 0.0012 + 0.0013) / 4 = 0.0014

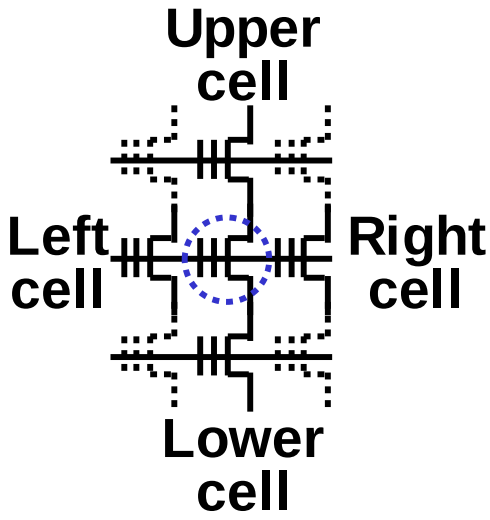
Pre-recorded Tables (2)





Upper cell data

Target cell data	"11"	"01"	"00"	"10"
"11"	BER_1	BER_5	BER_9	BER_{13}
"01"	BER_2	BER_6	BER_{10}	BER_{14}
"00"	BER_3	BER_7	BER_{11}	BER_{15}
"10"	BER_4	BER_8	BER_{12}	BER_{16}



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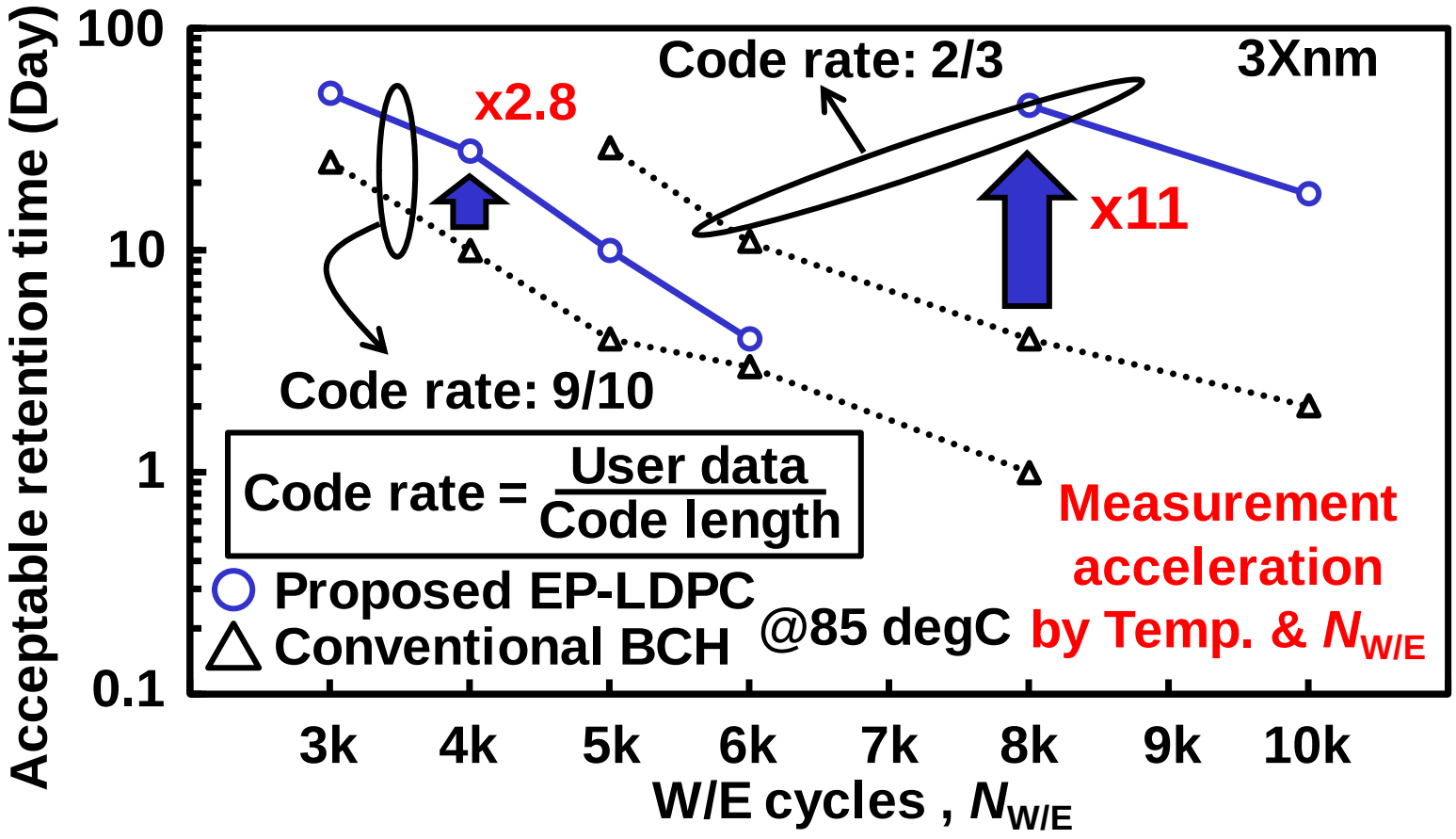
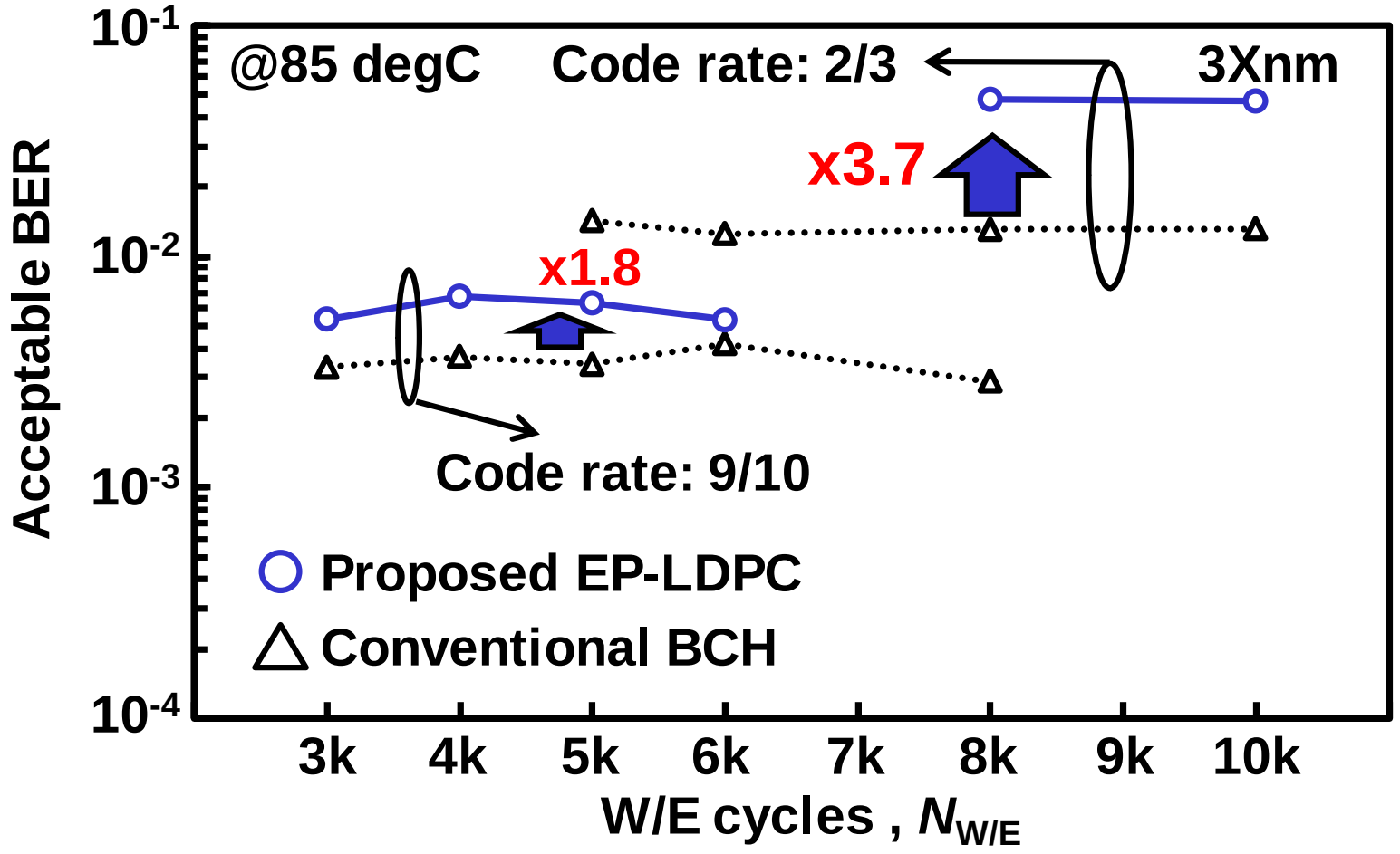
Acceptable Retention Time Extension

- Acceptable retention time is measured with 2 code rates (9/10, 2/3) and ECCs (BCH, EP-LDPC).



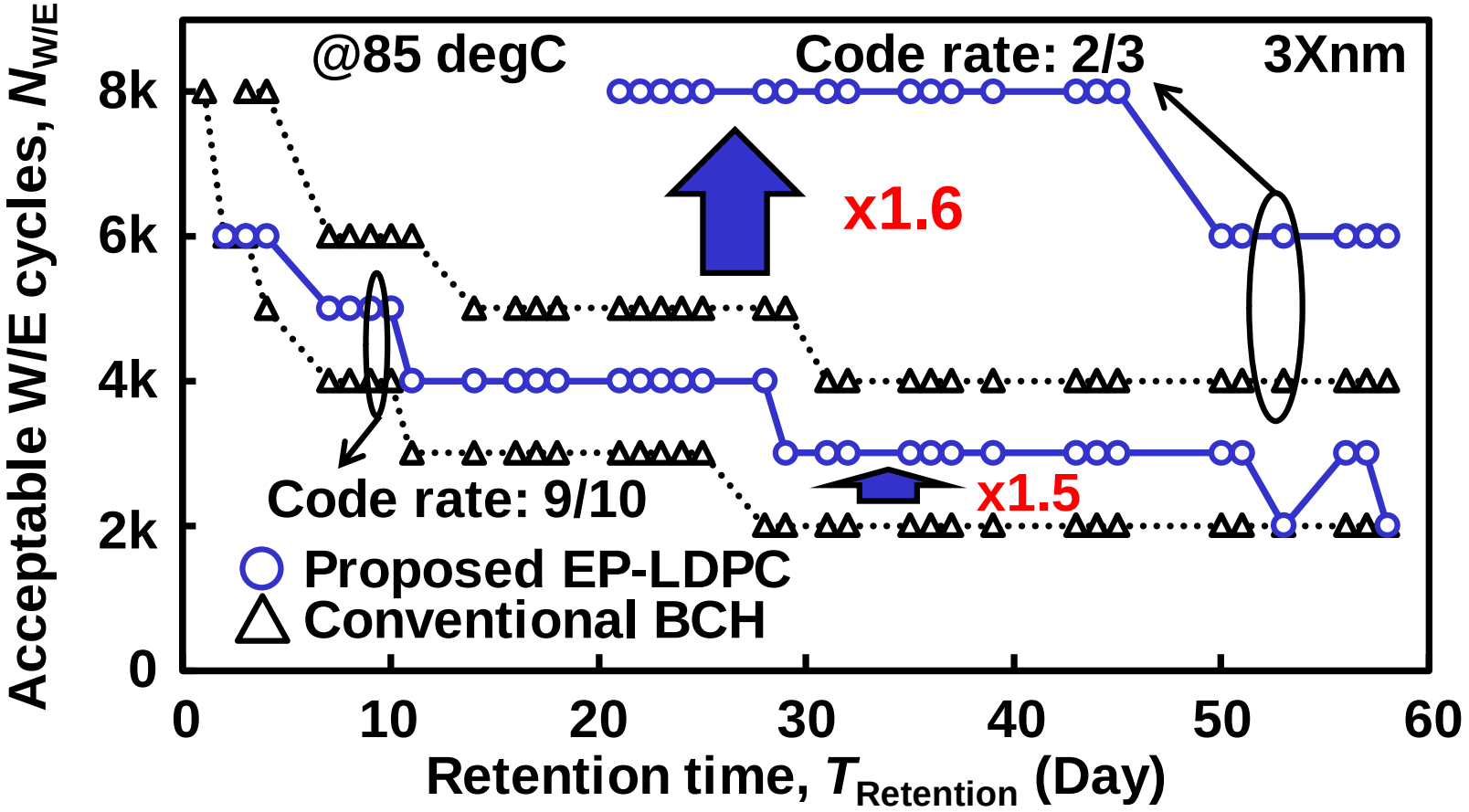
Improvement of Acceptable BER

- Acceptable BER is measured with 2 code rates (9/10, 2/3) and ECCs (BCH, EP-LDPC).



Improvement of Acceptable W/E Cycles

- Acceptable W/E cycles is measured with 2 code rates (9/10, 2/3) and ECCs (BCH, EP-LDPC).



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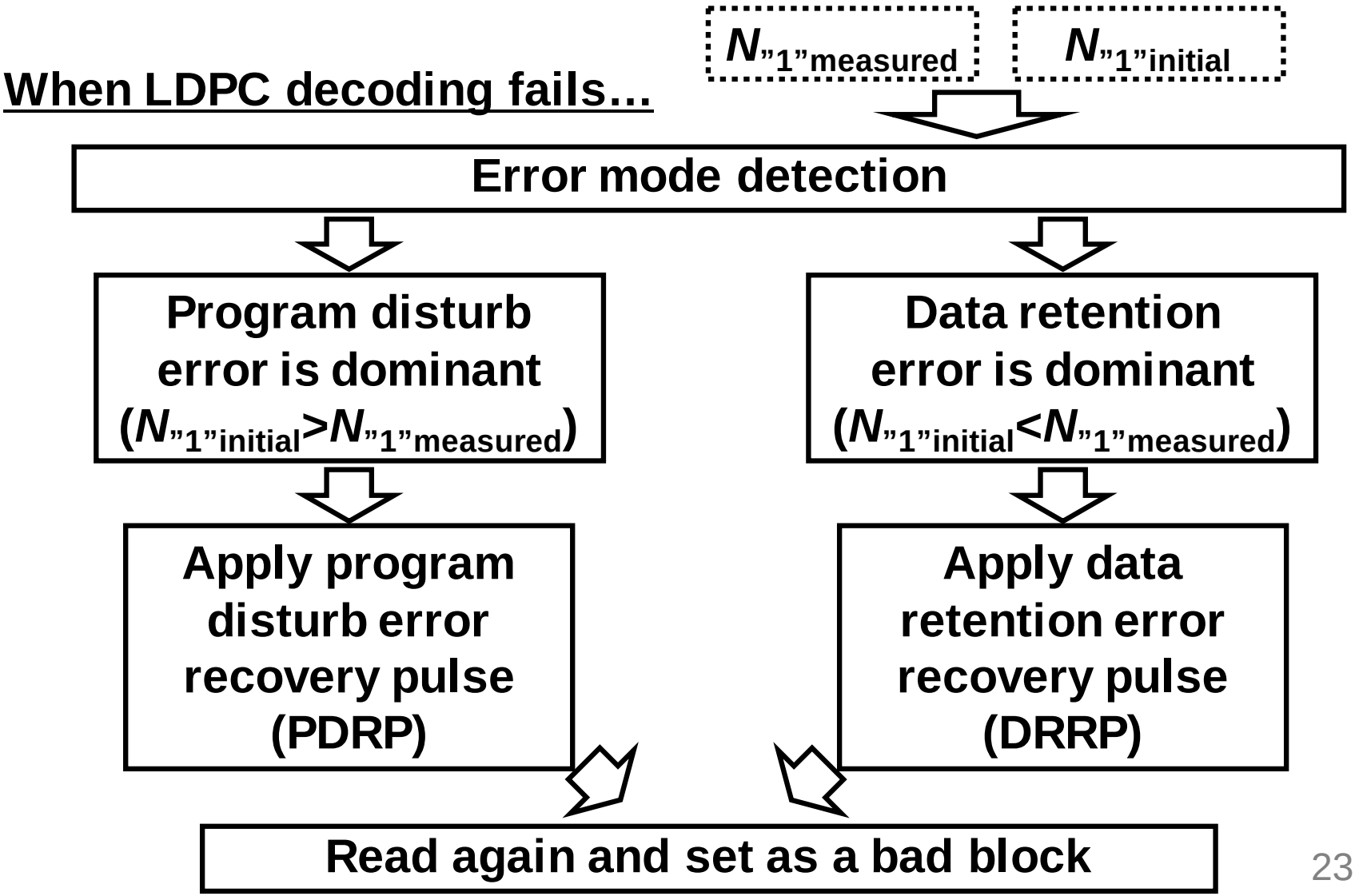
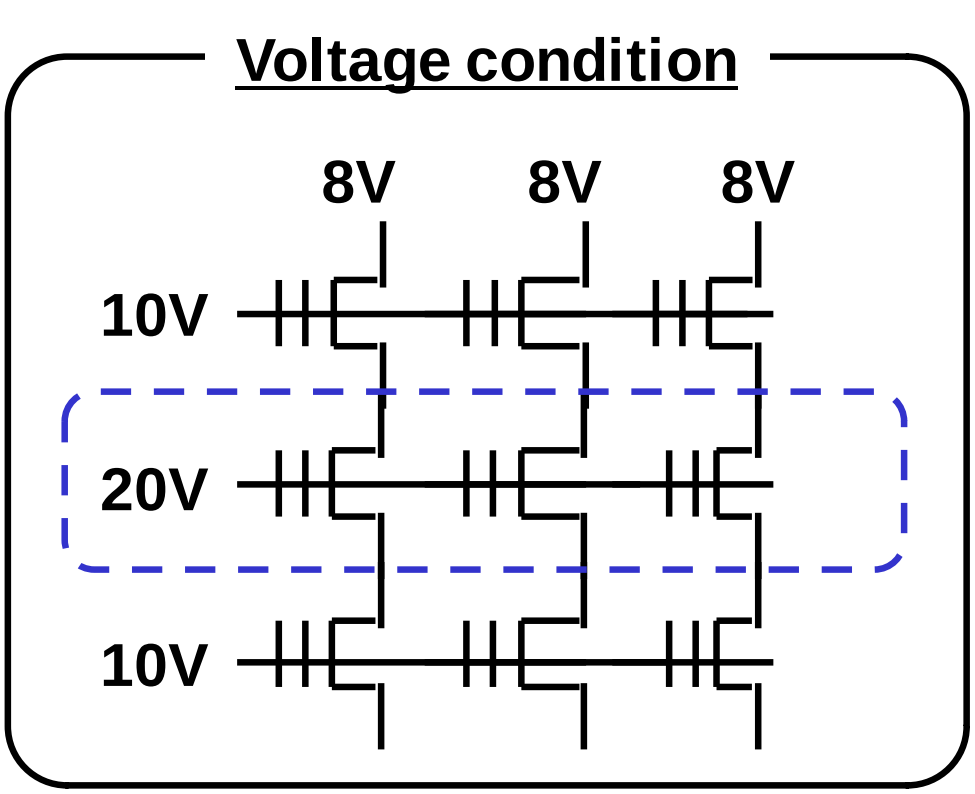
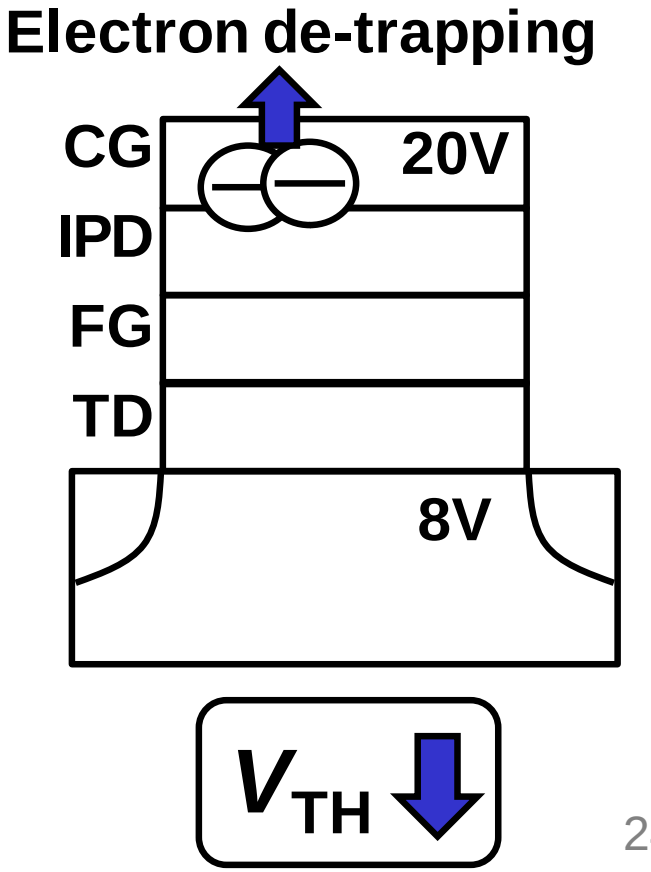
Flow of Error Recovery Scheme



Program Disturb Error Recovery Pulse (PDRP)

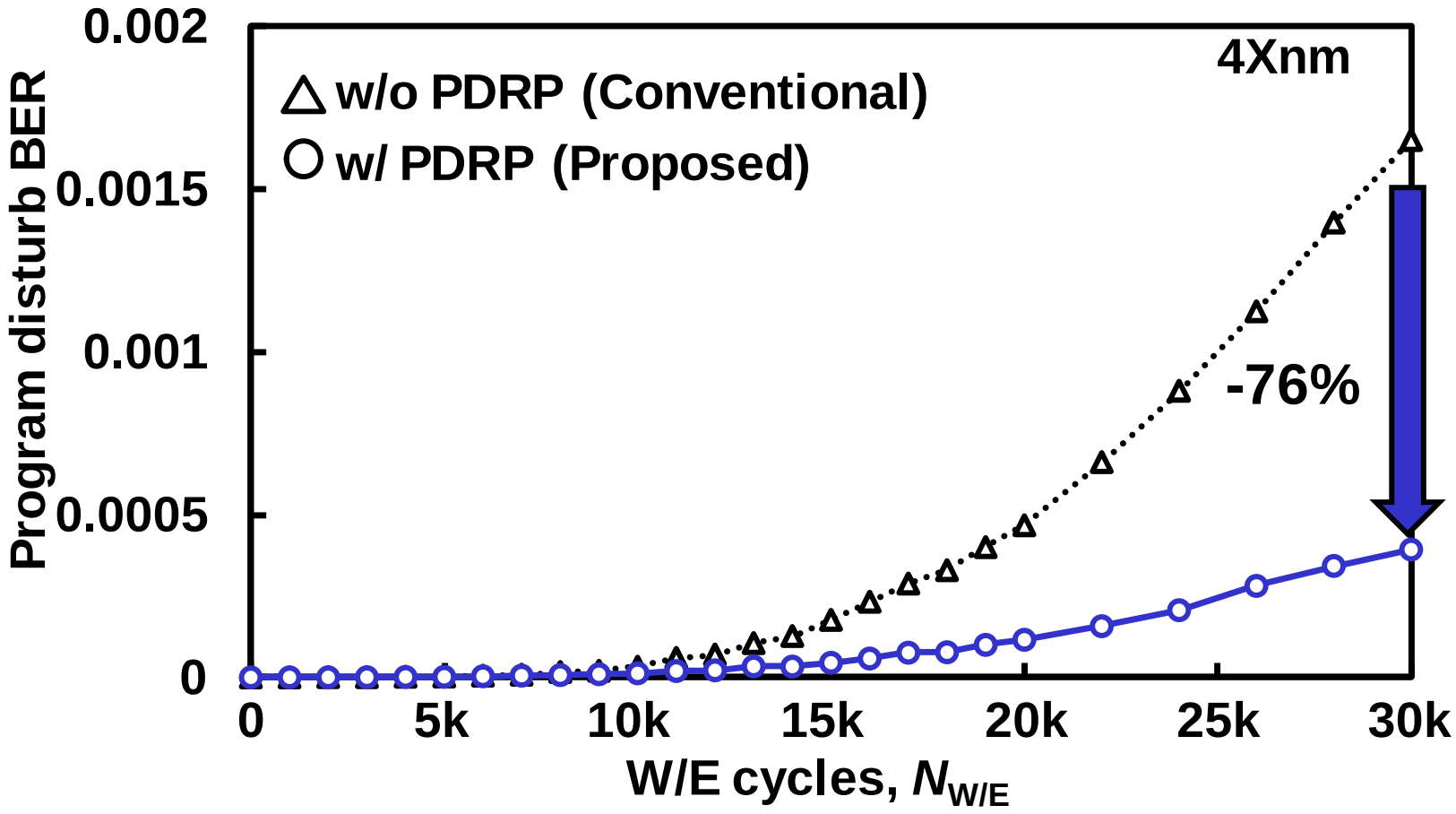
- Electrons at the interface between control gate (CG) and inter-poly dielectric (PD) are de-trapped with PDRP.





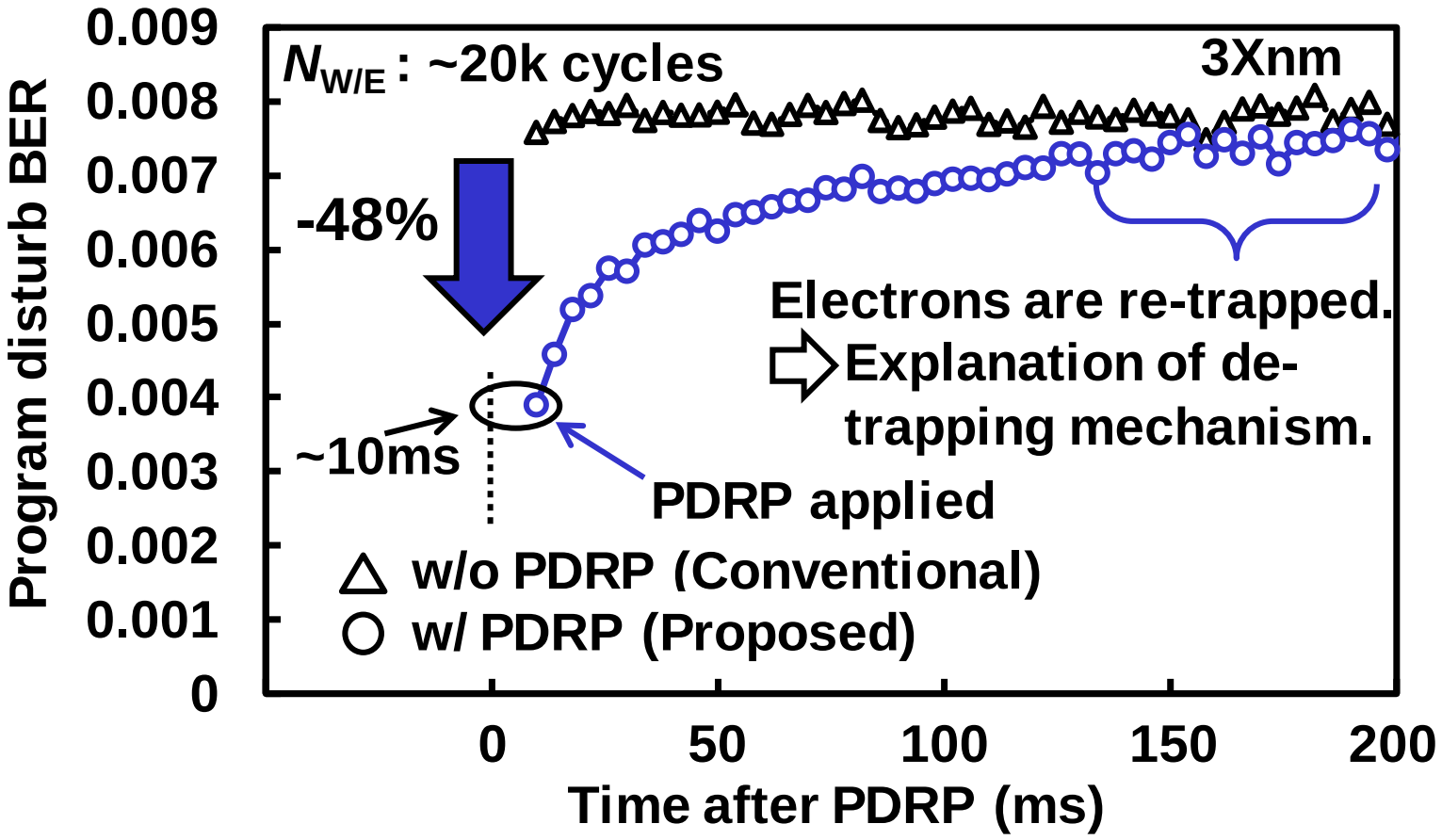
Measurement results of PDRP

- Program disturb BER is reduced by 76% by PDRP.
- The recovered data is read about 10ms after PDRP.



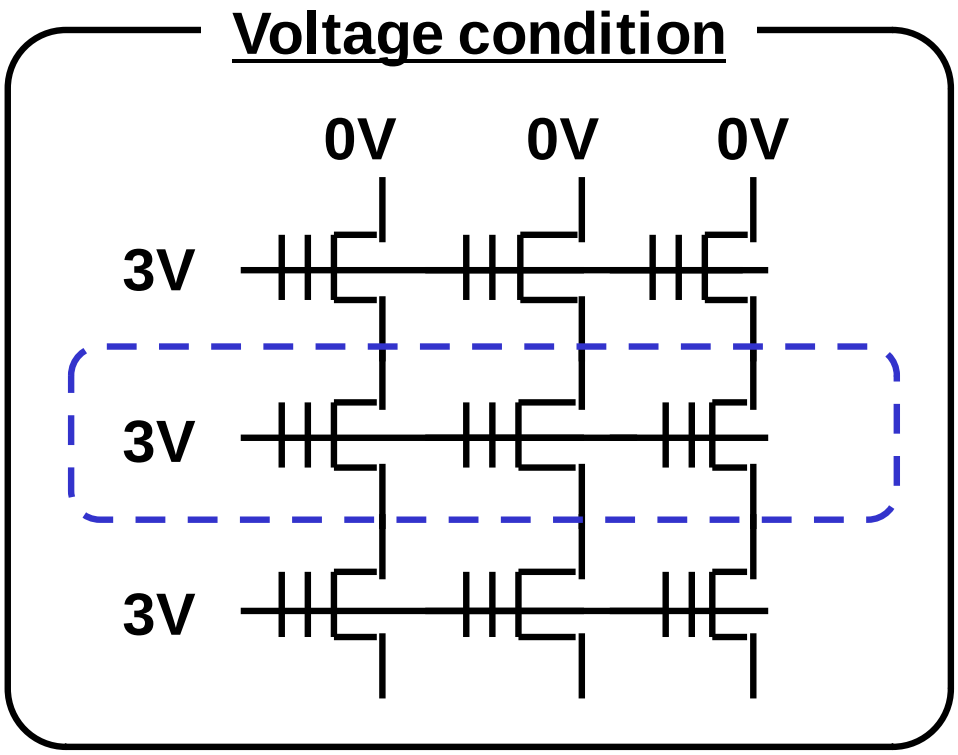
Transient Behavior after PDRP

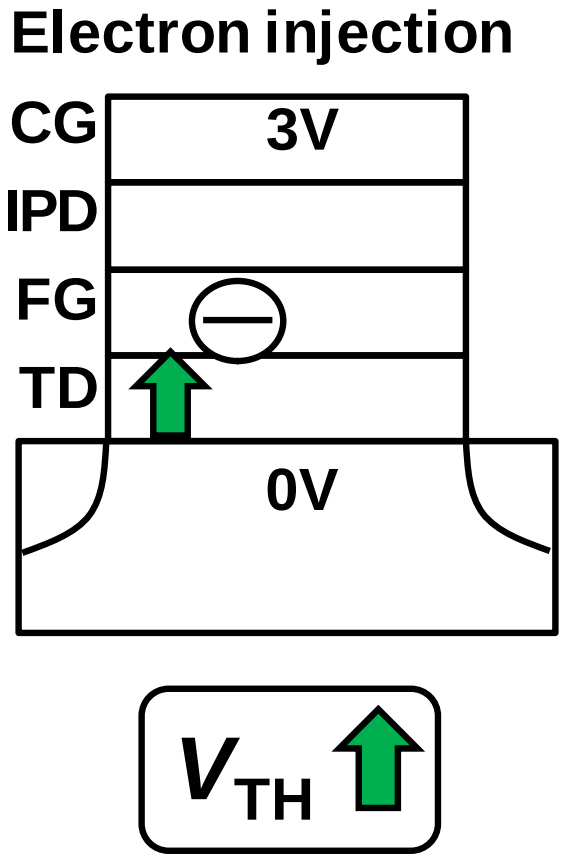
- BER with PDRP converges to the BER without PDRP.



Data Retention Error Recovery Pulse (DRRP)

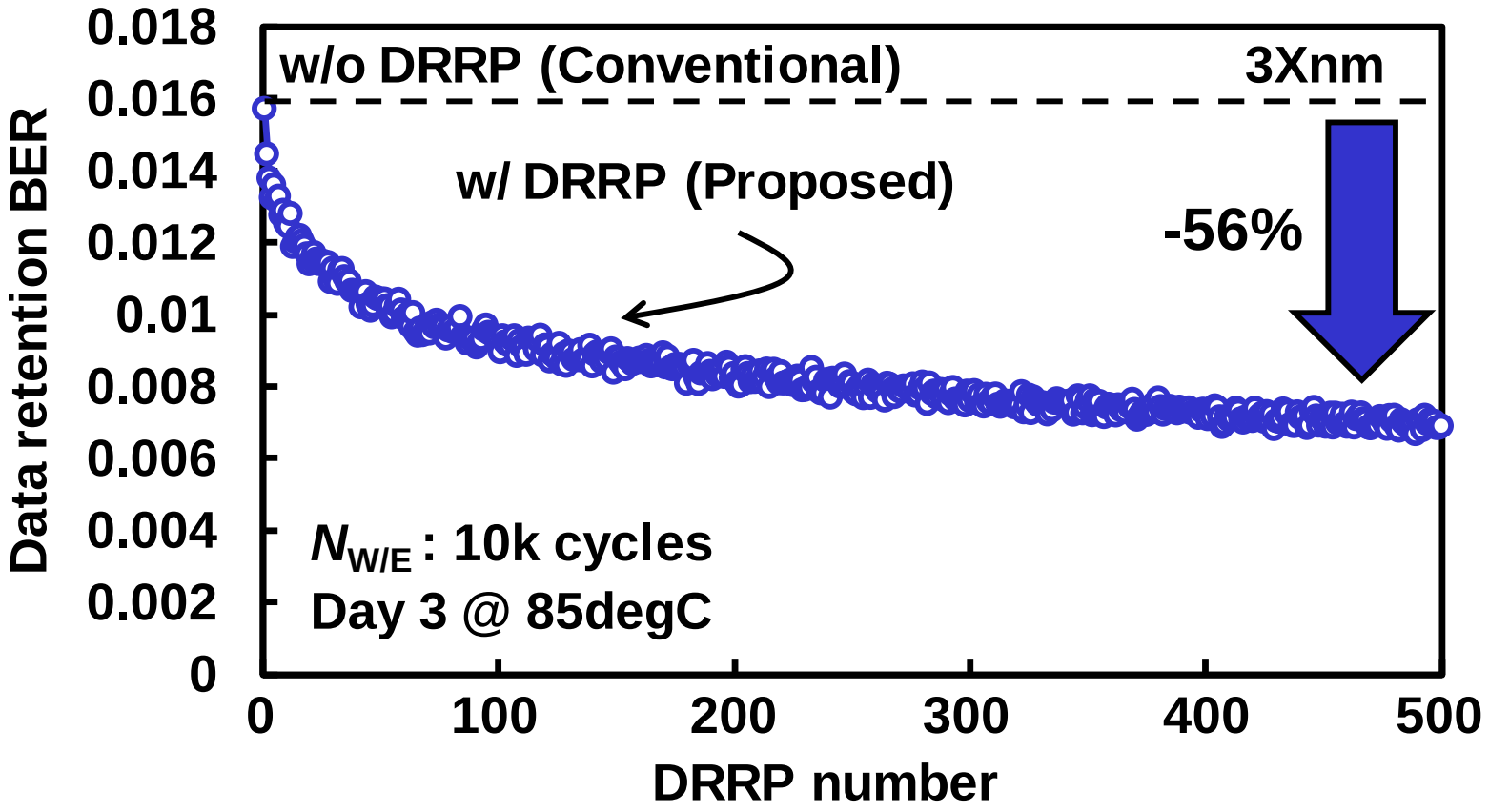
- Electrons are injected to the floating gate with DRRP.





Measurement results of DRRP

- Data retention BER is reduced by 56% by 500-times DRRP.



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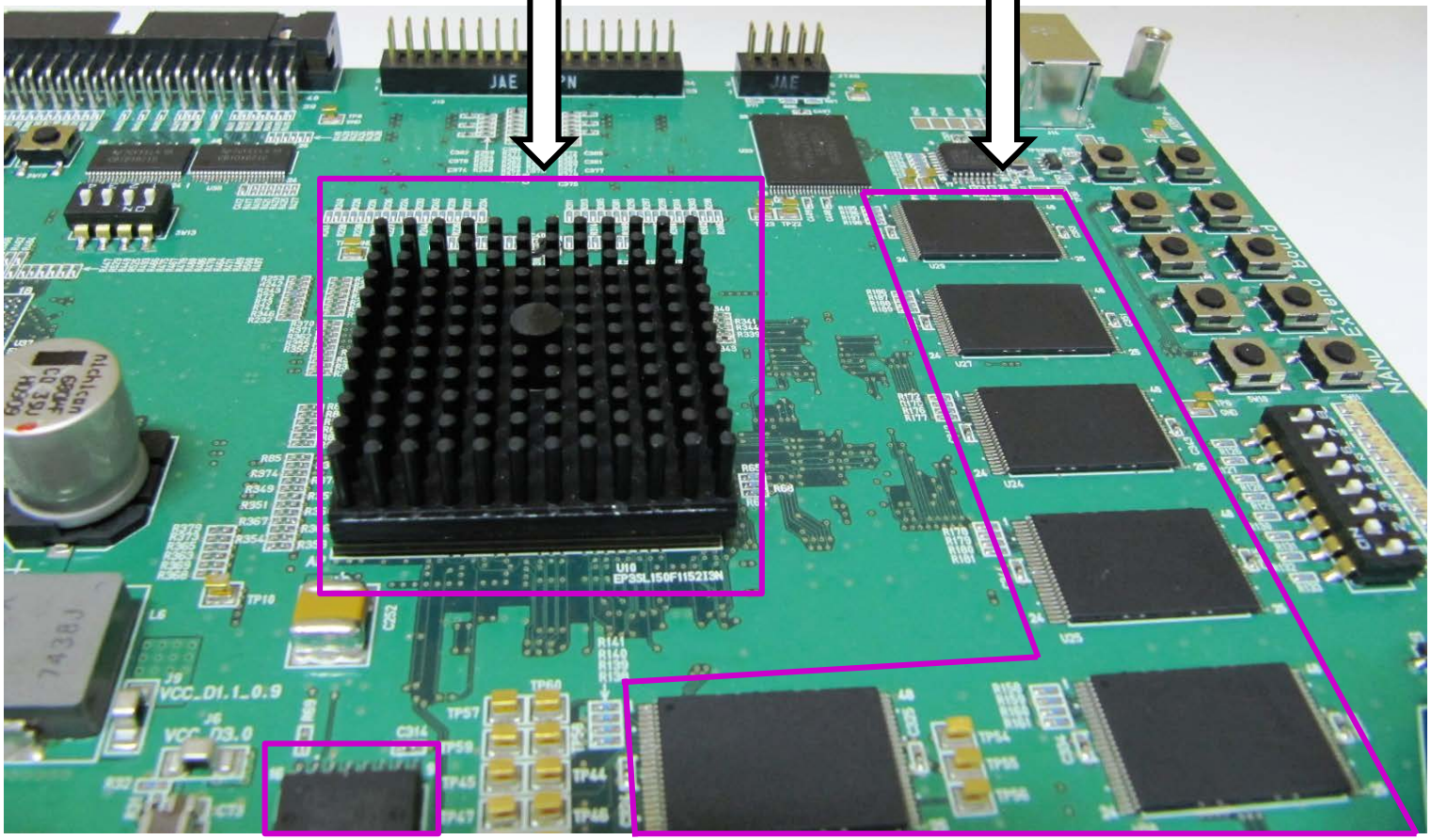
SSD Photograph



S. Tanakamaru *et al.*, *ISSCC*, pp. 204-205, 2011.

Summary of Key Features (1)

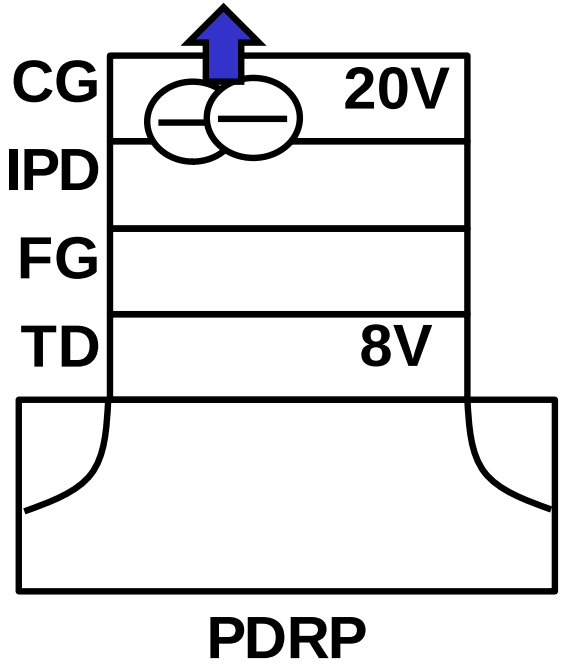
	BCH	LDPC (Soft decoding)	EP-LDPC
Considered information	V_{TH}	V_{TH} Inter-cell coupling	V_{TH} Inter-cell coupling W/E cycles Retention time
Sequential read cycles	x1	x7	x1
Acceptable retention time	4 days	-	45 days (>x10)

G. Dong *et al.*, *TCAS I*, pp. 429-439, 2009.

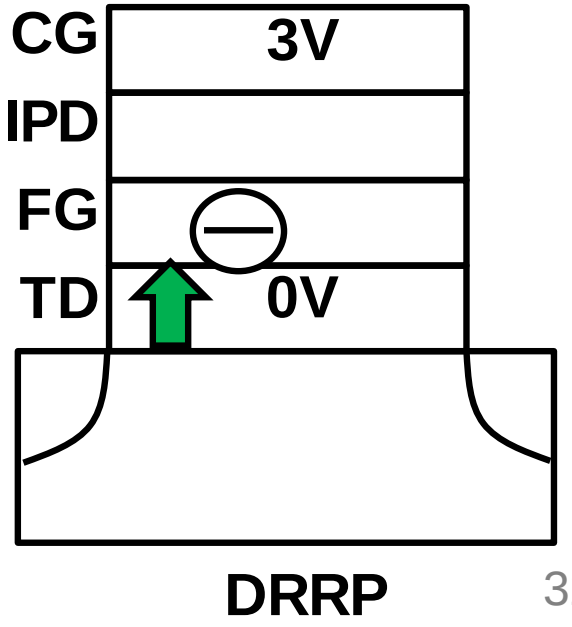
C. Kim *et al.*, *Symp. VLSI Circ.*, pp. 196-197, 2011.

Summary of Key Features (2)

	Conventional SSD	Proposed SSD
Program disturb error recovery	None	PDRP (-76%)
Data retention error recovery	None	DRRP (-56%)



PDRP



DRRP

Conclusion

- Highly reliable solid-state drive (SSD) is proposed with two key techniques.
- Error-prediction (EP) LDPC architecture is proposed.
- By estimating the BER of each memory cell with the pre-recorded tables, acceptable retention time increases by over 10-times.
- Error-recovery (ER) scheme is proposed.
- Bit error is reduced by 76% with error-recovery pulses.

Thank you for your attention

This work is partially supported by CREST/JST.