The Efficient LDPC DSP System for SSD

Jeff Yang

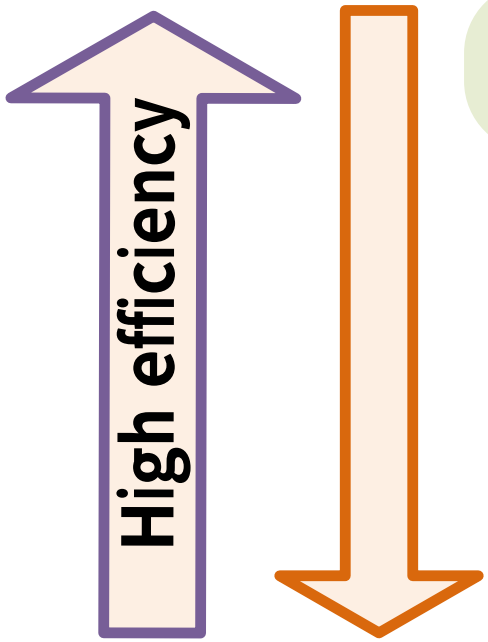
Principle Engineer

Silicon Motion

Agenda

- Error recovery flow
- LDPC design for NAND flash.
- High efficient Data-retention recovery.
- High efficient LDPC operation on embedded TLC.
- LDPC performance on real controller.
- Configurable ECC engine.

Error recovery flow

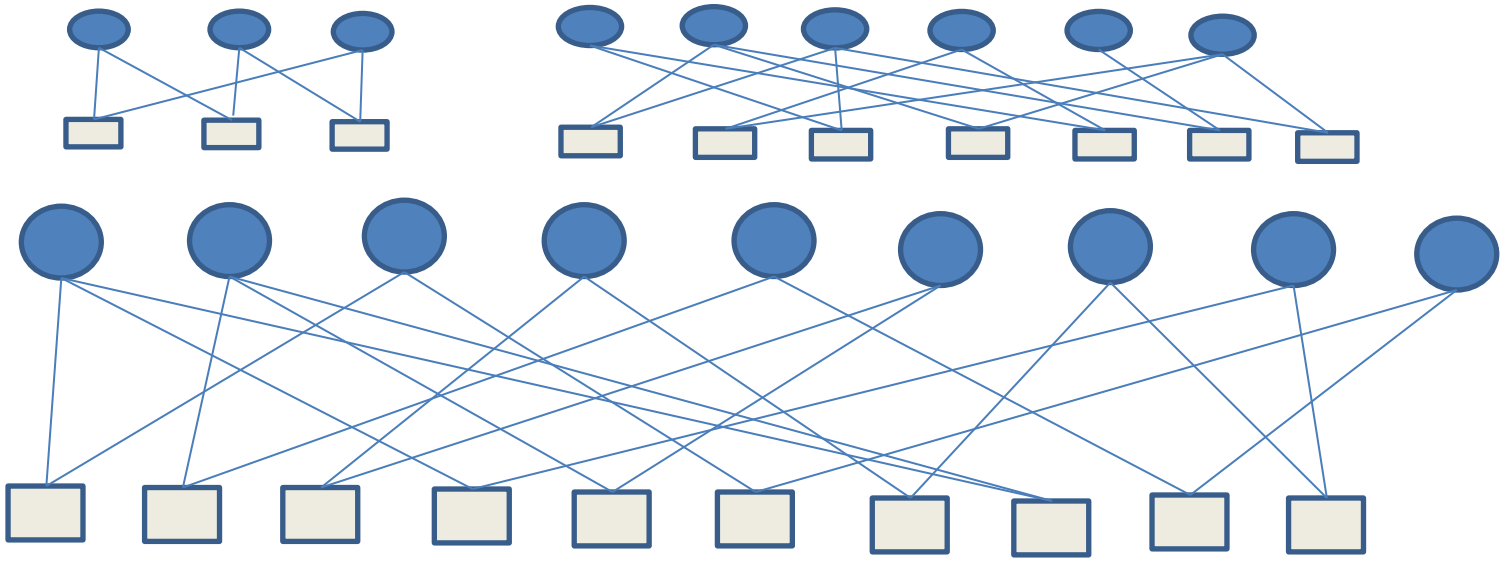


High complexity
Strong correction capability
Lower trigger rate

- Hard decoding
- Moving Read (Using read-retry table)
- Soft-decoding (Iterative decoding)
- Noise Cancellation
- RAID protection (addition parity)
- DISK Rescue

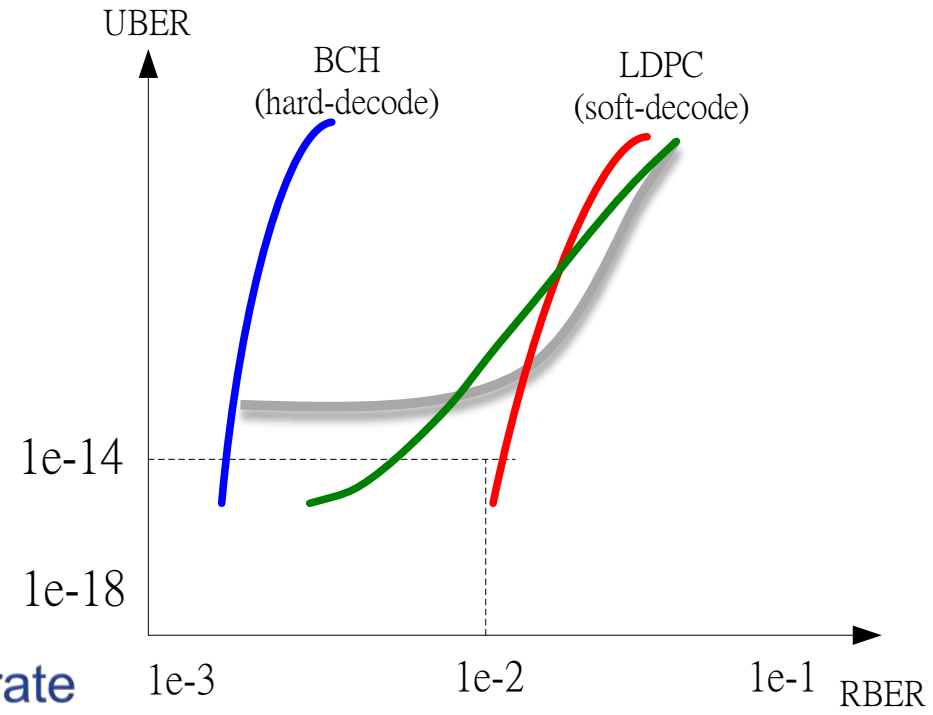
Trapping Set in LDPC Code

- The occurrence rate of noise in non-Gaussian part raises as the endurance-cycle increases.
- If a trapping set occurs in the non-Gaussian part, the error floor turns much worse beyond our imagination.
- Trapping Set Types



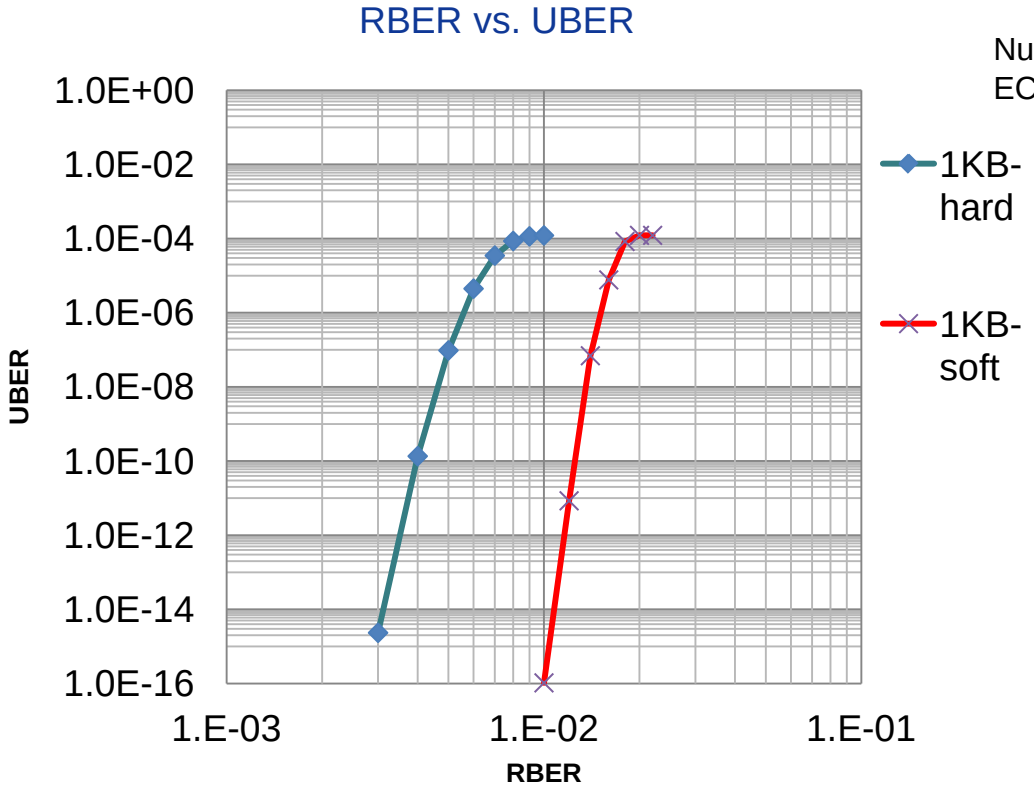
Optimized LDPC Design

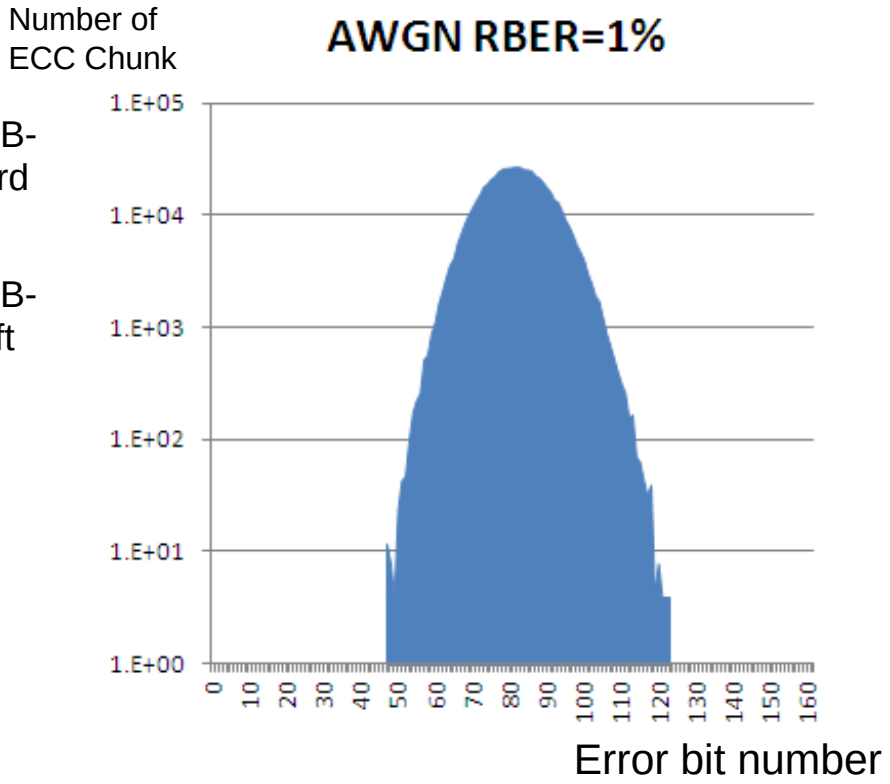
- Error floor
  - RBER decrease
  - UBER cannot become lower



- Solve the trapping set issue
  - Minimize trapping sets happen rate
  - Escape from the trapping set (under iterative decoding)
  - Concatenate with BCH coding is not the best way.
    - It consumes the capability of hard-decoding.
    - Lower column weight may help gain a better waterfall region, but it leads the error floor to become worse.

LDPC Correction Capability

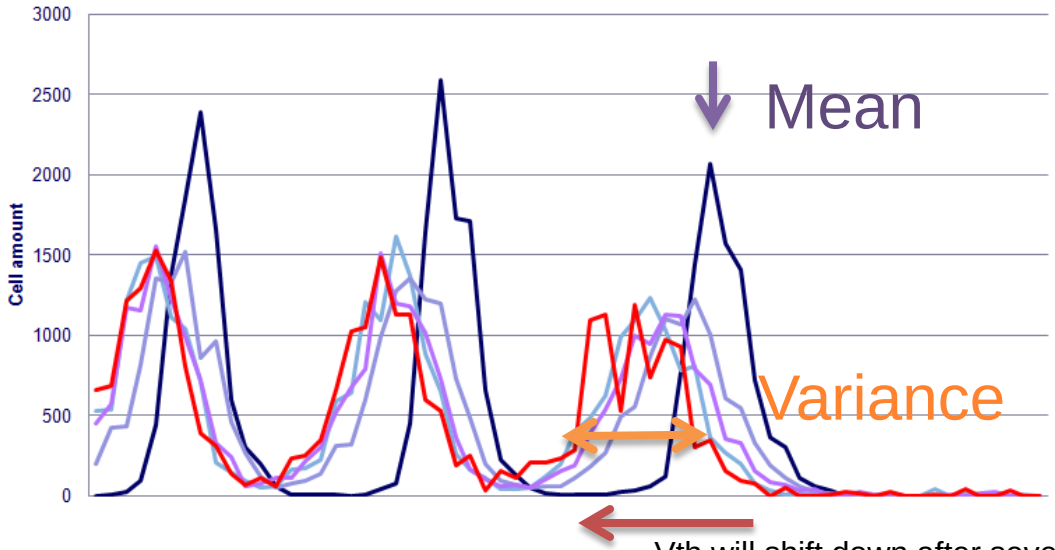




- AWGN RBER = 1e-2, UBER < 1e-15

- Soft-decoding can cover > 120-bit error
- The requirement (RBER = 1e-2) is similar to 120-bit error protection for TLC.

Efficient Retention Recovery



Vth will shift down after several hours baking
Mean value shift down, variance increase

Traditional Method

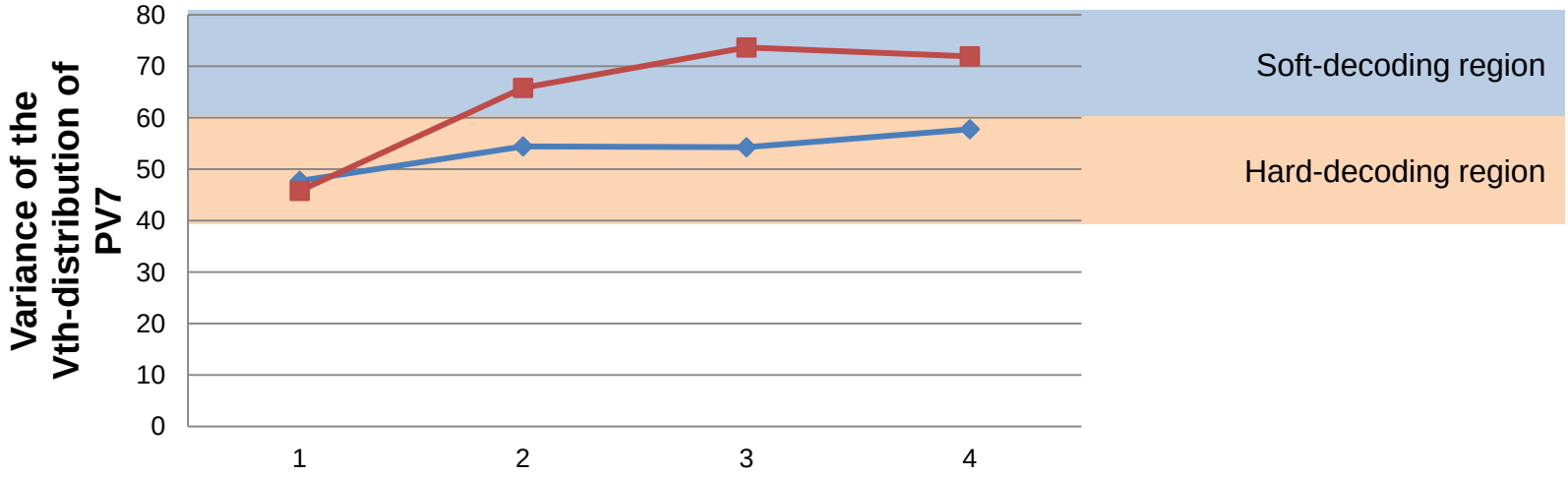
- When the host reads data, apply the complicated decoding.

New Method

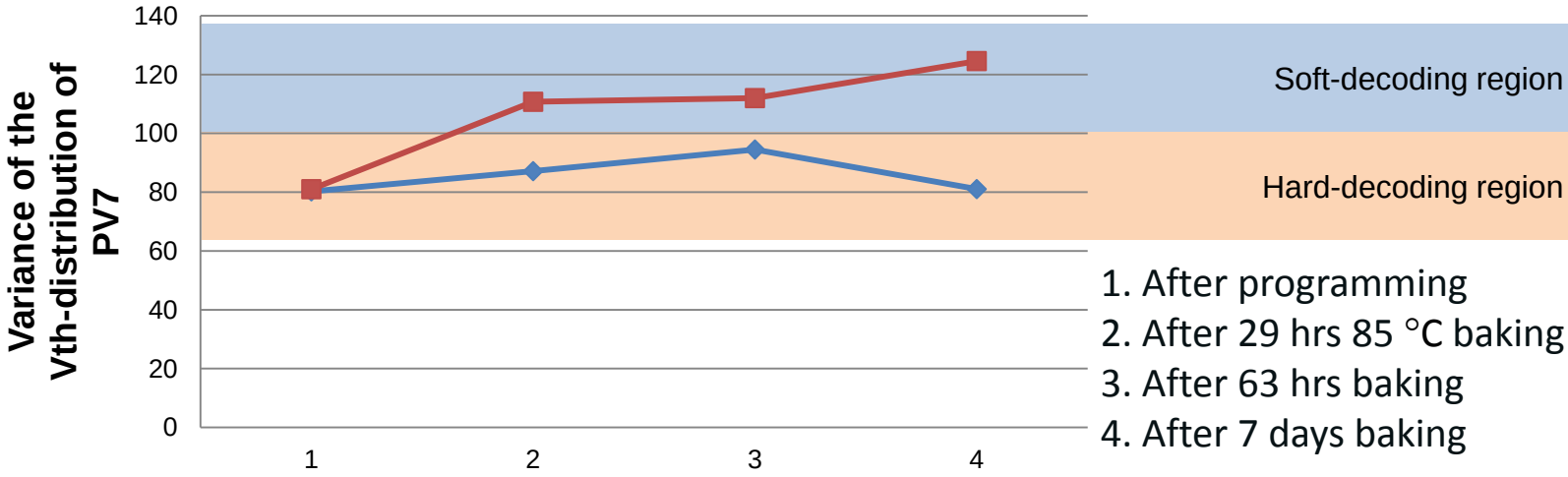
- Use DSP methodology to keep small variance in hard-decoding region, when the host want to read this data.

Superior Retention DSP on TLC

Flash A

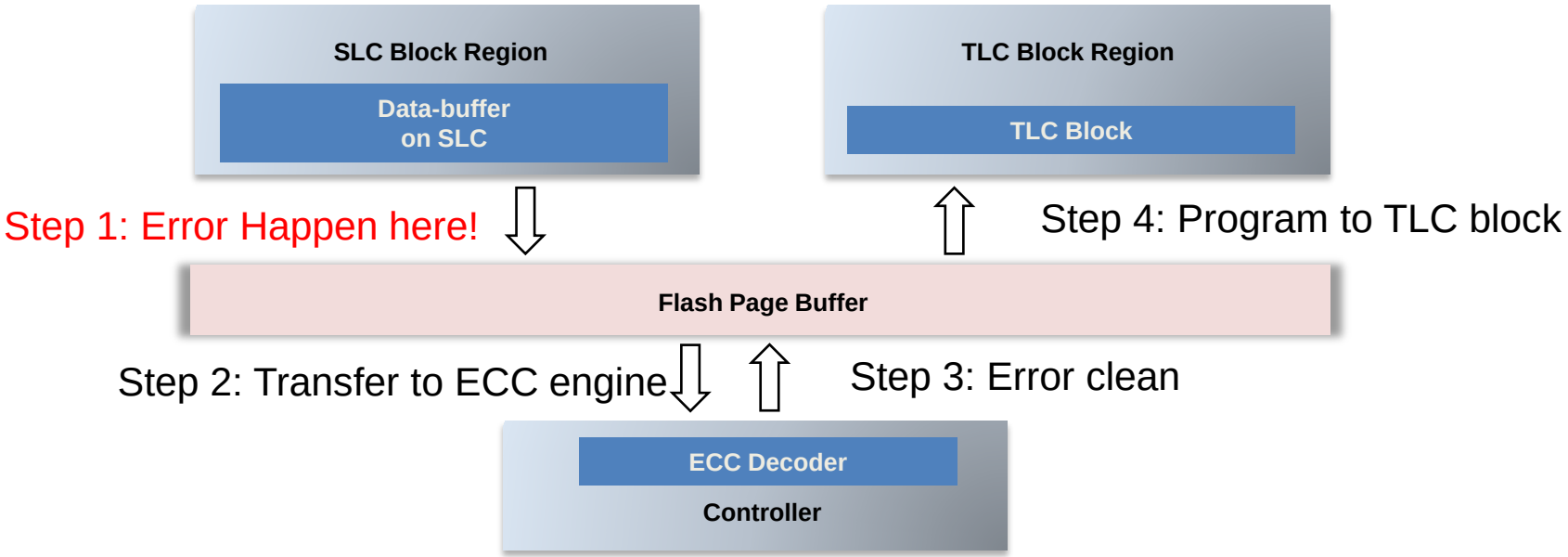


Flash B

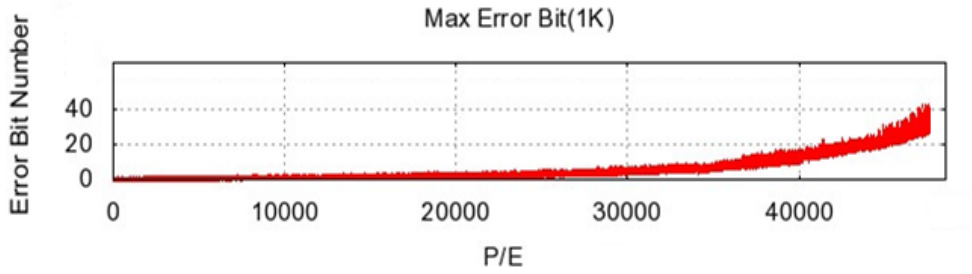


1. After programming
2. After 29 hrs 85 °C baking
3. After 63 hrs baking
4. After 7 days baking

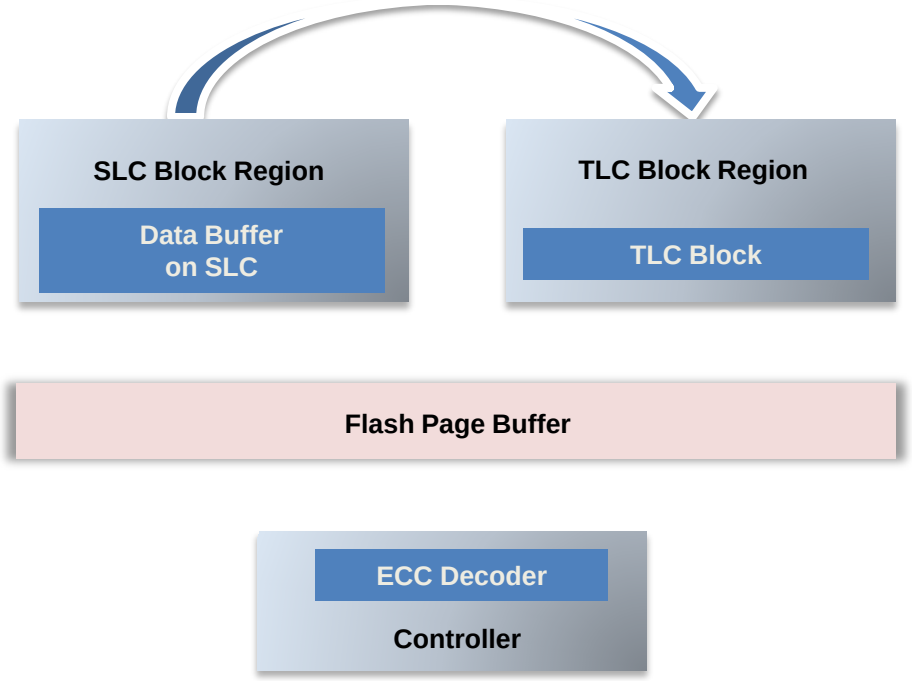
Traditional TLC Flash Operation



- SLC block Error-bit vs. Endurance



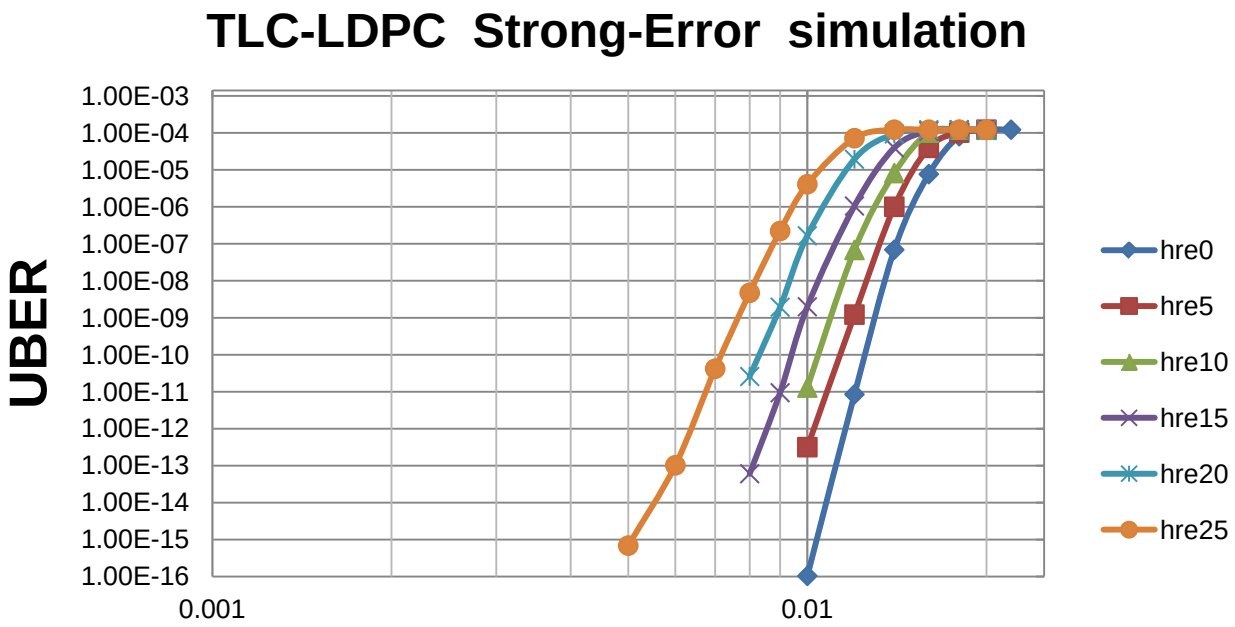
TLC Flash Operation



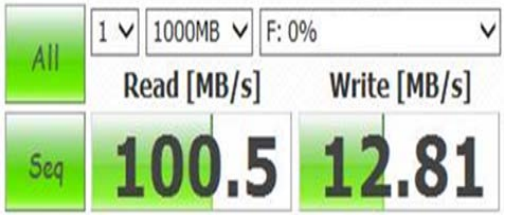
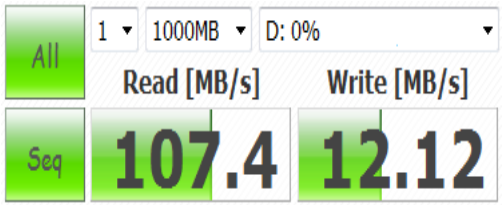
- Copying data from SLC to TLC is often used in flash operation.
- Copying data with checking latency
  - Data transfer time (2) + ECC decoding latency + Data transfer time (3)
- The system designer will need a LDPC engine with higher tolerance.

LDPC Solution

- Foggy and Fine Programming in TLC Flash
  - The immigrant error bits from SLC to TLC are the strong errors or highly reliable errors (HRE) in soft-decoding process..
  - The error floor will dominate the system reliability after long-term data retention.



LDPC Performance

USB3.0 controller	SM3263	SM3261
Process	110nm	110nm
ECC	LDPC	BCH
Sequential R/W performance		
Whole card Read-current	177mA	155mA
Controller Cost	150%	100%
Target RBER UBER=1e-15	300%	100%

- SM3263 UFD Controller (110nm Process)
- Test Environment
  - CPU: Intel core-I5
  - USB host: Ivy bridge
  - OS: Win8
  - 1xnm TLC 2-way
- LDPC Power Consumption
  - 10~20-bit error (hard): 28mA
  - 20~40-bit error (hard): 42mA
  - 40~68-bit error (hard): 70mA
  - 68-bit error (soft): 30mA

Configurable ECC engine

Configurable BCH Engine

- Protect 1 to 72 bits: 1-bit protection mode, 2 ~ 72-bit protection mode
- Run-time configuration

Configurable LDPC Engine

- Support 1KB data with different parity lengths: From 120Bytes to 68Bytes with 4Bytes step size.

Benefits of Configurable ECC Engine

One single controller is able to support all kinds of flash types for flash vendors.

Dynamic protection levels.

Summary

- The major concerns in TLC based SSD
  - Reliability.
  - Power.
- SMI provides very efficient LDPC decoder for TLC based SSD
  - The power increase slightly.
  - Correction capability increases 3 times comparing to BCH.
  - Adaptive Vth-tracking with joint Hard/soft decoding to improve the latency.
  - SLC to TLC direct-copy.
  - Good user experience, higher reliability.

THANK YOU!

Q & A

Disclaimer Notice
Although efforts were made to verify the completeness and accuracy of the information contained in this presentation, it is provided “as is” as of the date of this document and always subject to change.